Heidelberger VHDL Graduate Courses

The Heidelberg VHDL graduate course aims at students of the Heidelberg/Mannheim/Bergen/Oslo international research and training group and other interested students. It teaches the fundamentals of hardware design and VLSI design, using the hardware design language VHDL as example. The course is split into lectures and practical work, where the material, which is taught in the morning is practised immediately in the afternoon. Here own designs are developed, translated into hardware, using the appropriate tools and then exercised using the FPGA evaluation board UXIBO (http://sus.ti.uni-mannheim.de/Uxibo), which was developed in Mannheim. The lectures will take place in the KIP CIP Pool (http://www.kip.uni-heidelberg.de/cip/cip.html) and the practical work in the KIP hardware praktikum (http://www.kip.uni-heidelberg.de/ti/HWP/?lang=en). We will try to provide students, who already have knowledge of VHDL, whith appropriate advanced study and praktikum material.

The Course is organized during five days with the program below. All relevant Course material, reference designs, assignments can be found there. The lectures start at 9:00 in the morning and the practical course ends at 17:00 in the afternoon.

Introduction to VHDL and Synthesis

Saturday, September 17

Lectures

Introduction, Motivation

Hardware Design Layers

Examples of Target Technologies

Building blocks of digital circuits

Introduction to VHDL

VHDL signals and data types

VHDL operators

Exercises

Introduction

First designs in FPGA

Social Event

Sunday, September 18
Meeting 10:00 at the Kirchhoff Institute for Physics where a bus will take us first to Speyer.
Visit of the famous "Dom zu Speyer" which is the largest existing Roman church in the world.
"Technikmuseum Sinsheim" where you can have a closer look at more than 300 vintage cars, 200 Motorbikes, 40 Sportcars, the largest collection of Formular-1 cars, 60 planes and a walk through a CONCORDE or a TUPOLEV TU-144.
At 16:30 the bus will bring us back to Heidelberg, giving the Germans the possibility to go to the election and vote for a (even) better future.
After so much hard work there definitely the need for a relaxed barbecue in the garden of the Physikalisches Institut. 19:00! Don't miss it!!!
!!! CHANGE !!! Due to the weather forecast the barbeque will take place in the old library in the Albert Überle Straße. And it will start at 18:30!!!
More detailed information will be given on Saturday during the VHDL course.

Parallel and sequential Operators

Monday, September 19

Lectures
Parallel and sequential Operators Introduction and fundamentals
Parallel and sequential Operators Advanced features

Exercises
Parallel and sequential Operator designs

Finite State Machines in VHDL

Tuesday, September 20

Lectures
Finite State Machines in VHDL

Exercises
FSM Designs

VHDL synthesis and application of FPGAs

Wednesday, September 21

Lectures
VHDL synthesis
VHDL FPGA Designs
Commercial Applications of FPGAs
Exercises

Advanced FPGA Designs in VHDL

Miscellaneous

Miscellaneous Material

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