IRTG Fall School 2006, Heidelberg

Silicon Pixel Detectors

Peter Fischer

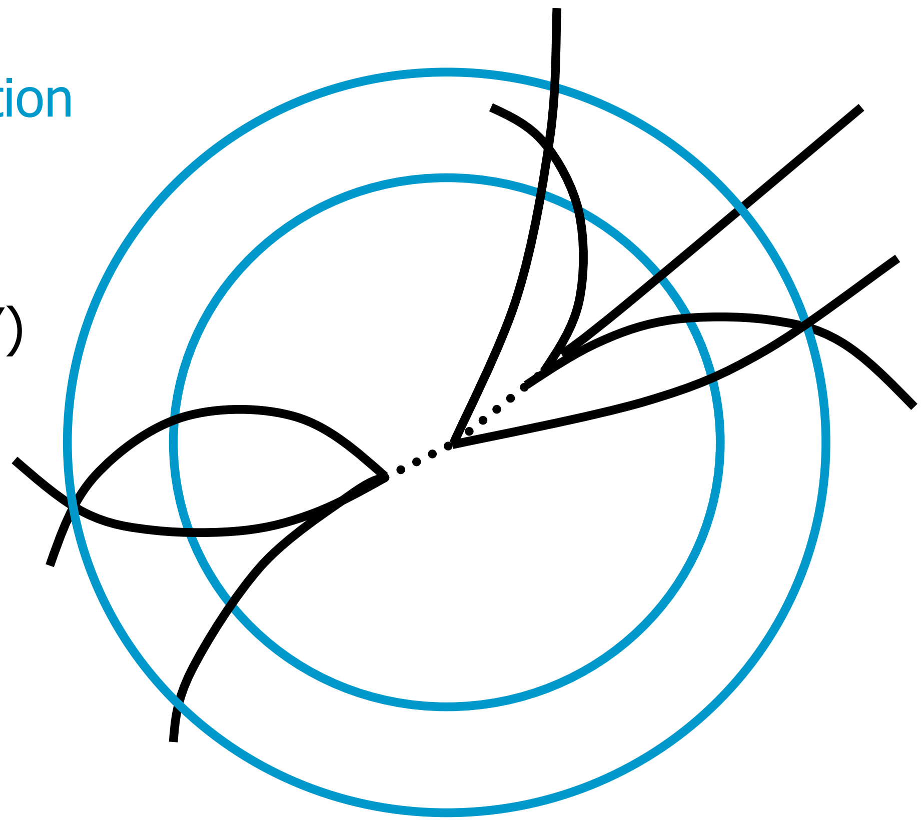
Universität Mannheim

Silicon Pixel Detectors – Today and Tomorrow

- Why pixels?
  - Requirements and challenges
- The ATLAS pixel detector
  - Modules, mechanics etc.
  - The sensor
  - The front end electronics
  - Some results / present status
- The next generation (for TESLA)
- Other applications of hybrid pixel detectors

Tracking in Particle Physics

- Goals:
  - Full event reconstruction, pattern recognition
  - Momentum measurement
  - Identification of short lived particles
    (e.g. B-Mesons for b-physics, Higgs, SUSY)

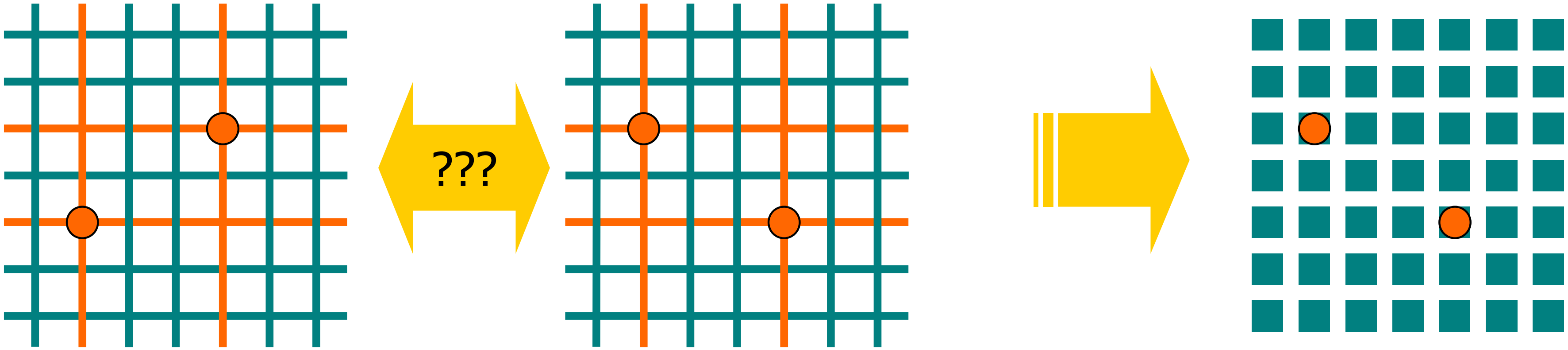


- Requirements for innermost layers:

- Small radius	few cm
- High resolution	$\sigma_{r\varphi}$ ~ 15 µm, σ_z ~ 1 mm
- Short radiation length	~ 1% X_0 per layer
- Accept high track density	several hits / crossing / cm^2 (jets!)

Why Pixels ?

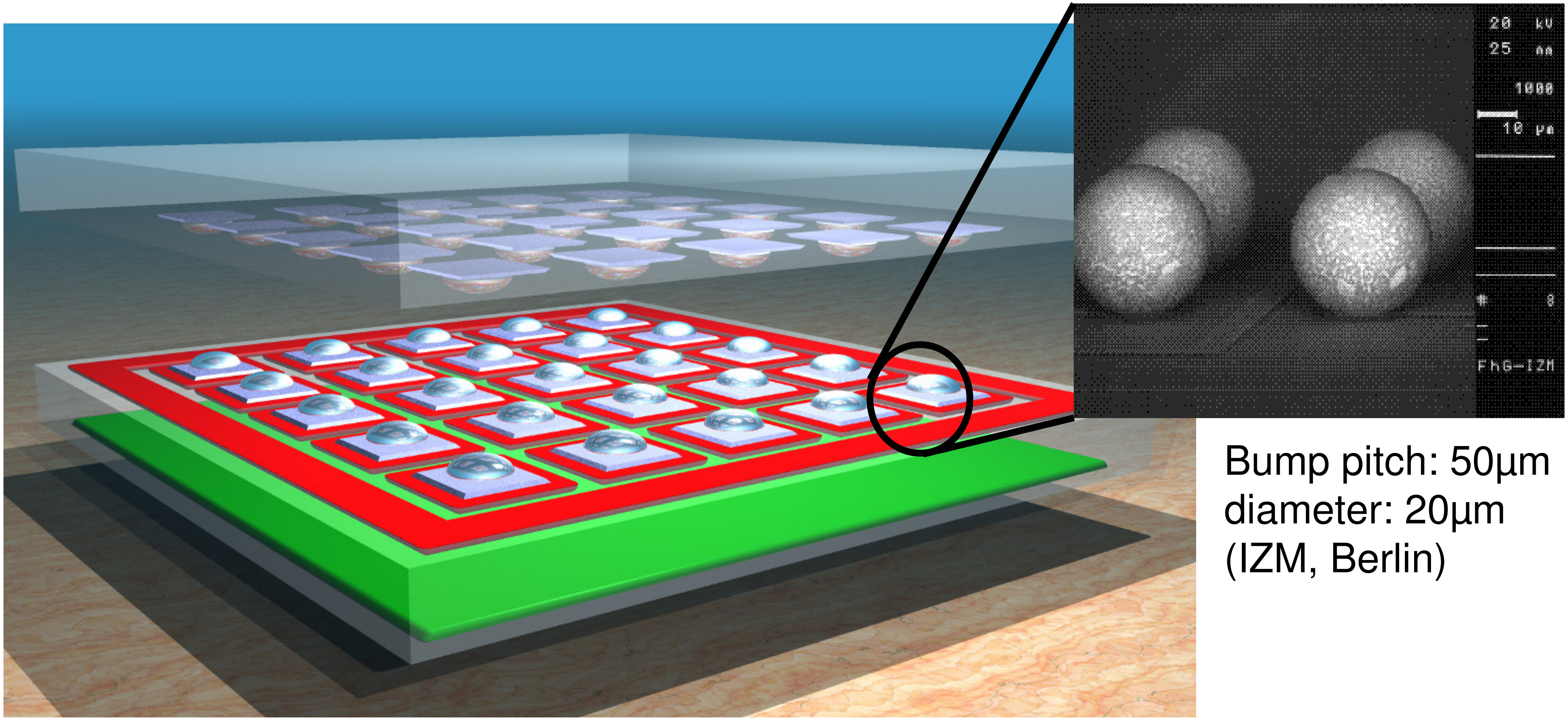
- Avoid ambiguities (‚ghost hits‘) at high multiplicities $\Rightarrow$ need true 2D detector !



- Survive high radiation level $\Rightarrow$ need very low noise

- Note: Strip detectors have better resolution & shorter radiation length!

Hybrid Pixel detectors



Bump pitch: 50µm
diameter: 20µm
(IZM, Berlin)

- Every pixel is connected to a separate amplifier on the readout chip
- Low input C ⇒ low noise ⇒ low threshold ⇒ can operate with thin detectors and small signals after irradiation ⇒ intrinsic radiation hardness

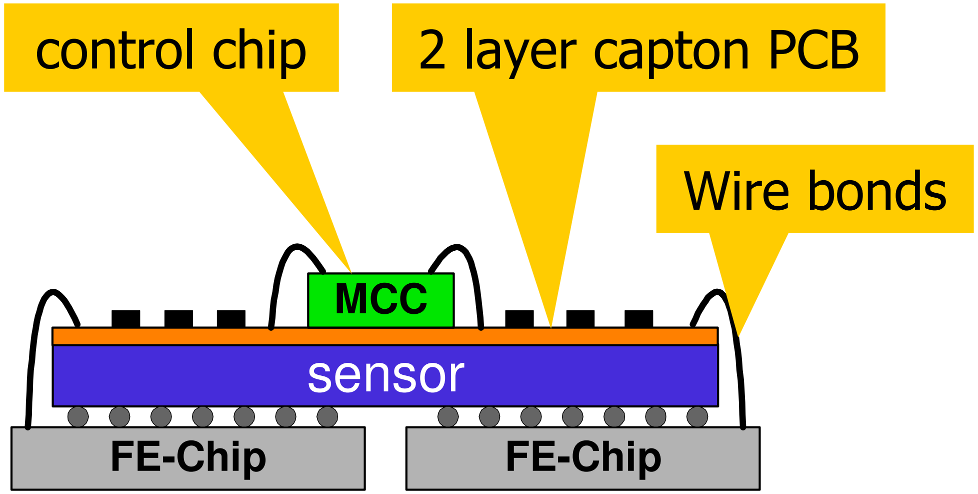
Requirements for pixel detectors in HEP

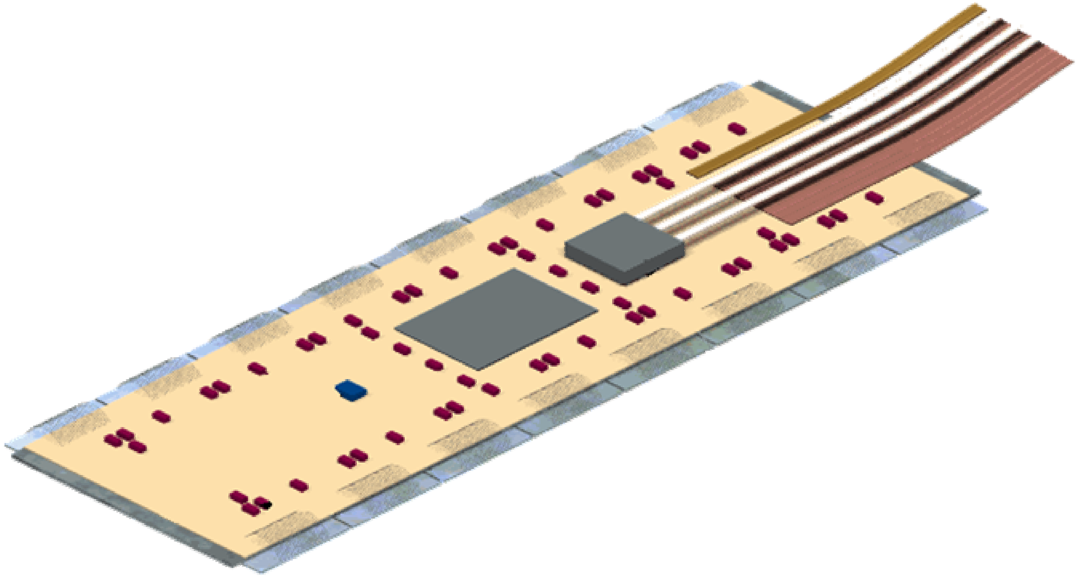
▪ Pixel Size	50 x 400 μm^2 (ATLAS)	(as small as possible, limit is power)
▪ Worst case signal	1fC = 6000 electrons	(mip in 300µm silicon in pixel corner)
▪ Threshold	2000 electrons	(quite a bit smaller than signal)
▪ Noise	200 electrons	(quite a bit smaller than the threshold)
▪ Threshold dispersion	200 electrons	(comparable to the noise)
▪ Leakage current tolerance	100nA / pixel	
▪ Speed	25ns timing precision	(bunch crossing of LHC, 'time walk')
▪ Data storage	up to 160 clock cycles	(level 1 latency)
▪ Radiation Tolerance	50 Mrad, 10^{15} n/cm^2	(10 years operation)
▪ Power	50µW / pixel	(including periphery, ~ 10W / Module)
▪ Material	~ 1% X_0 per layer	an unrealistic goal at the end...
▪ Track efficiency	≥ 99 %	(including gaps between sensors)
▪ Many channels	10^8	(**must** have zero suppression)

The Module

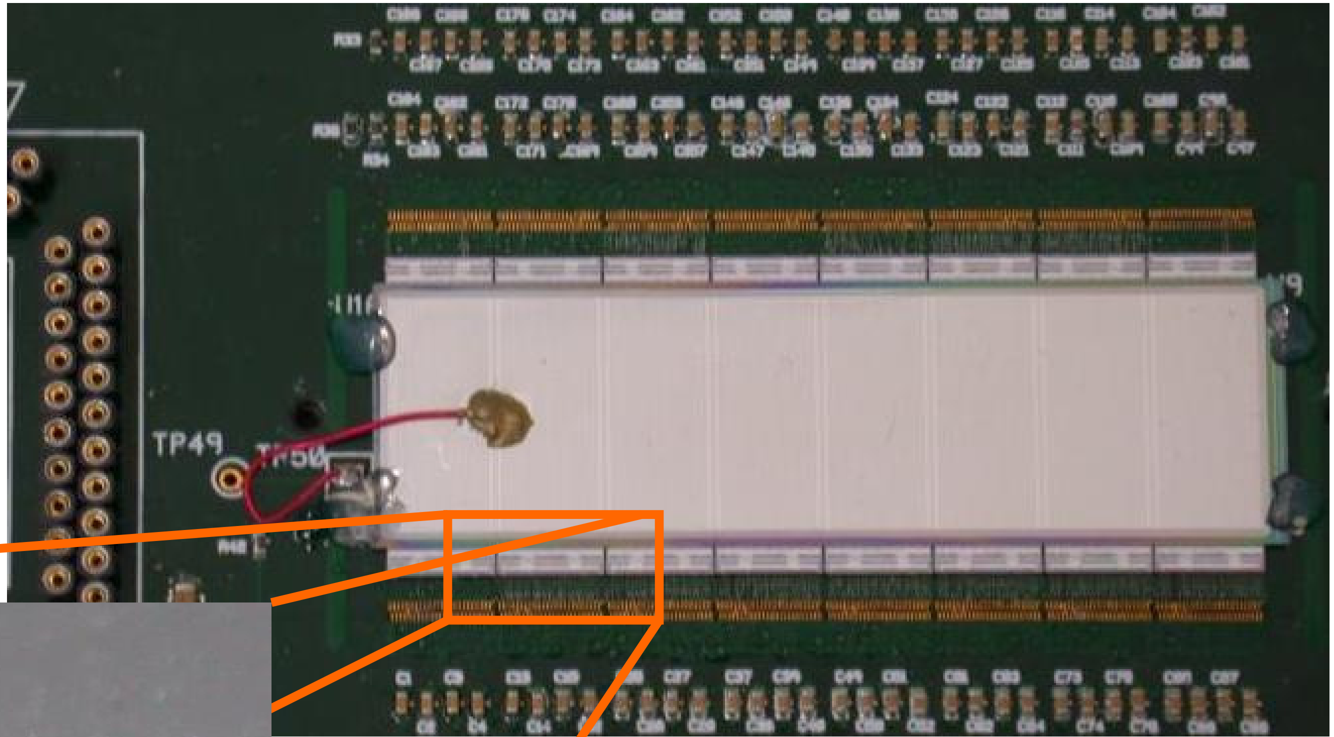
Flex capton solution:

- Connections between FE-Chips, module control chip, other components and cable through a thin capton PCB
- Larger pixels between chips
- Size = 16.4×60.8 mm^2
- 16 chips with ~ 50000 pixels total
- ~ 2000 modules needed

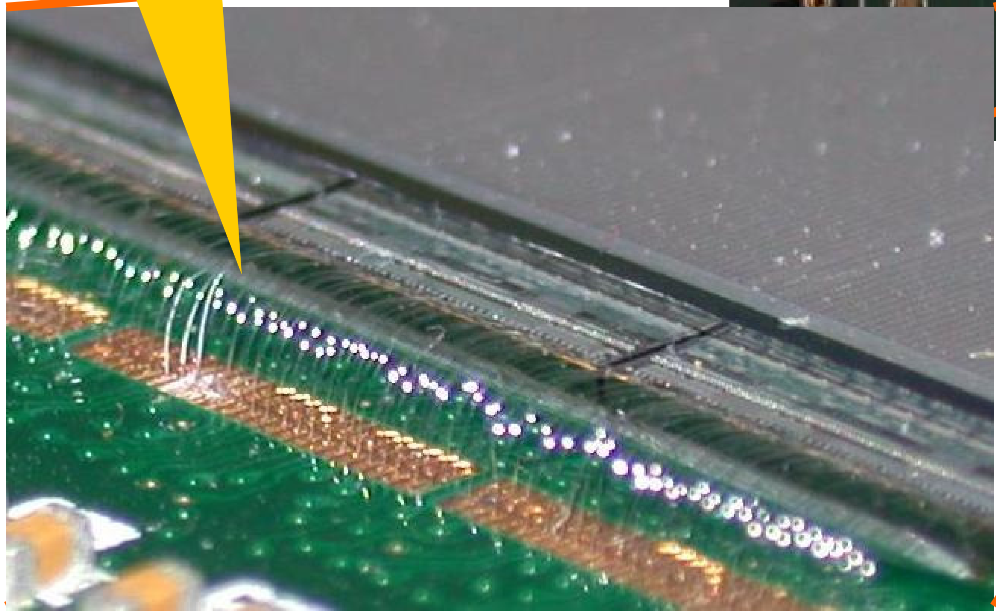


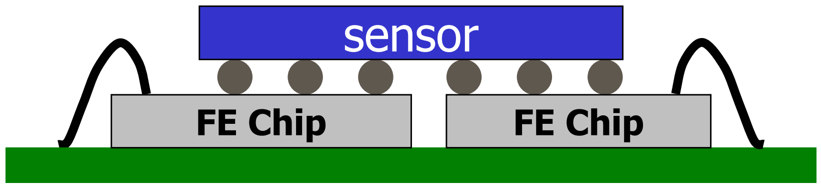


1st generation: flex on support

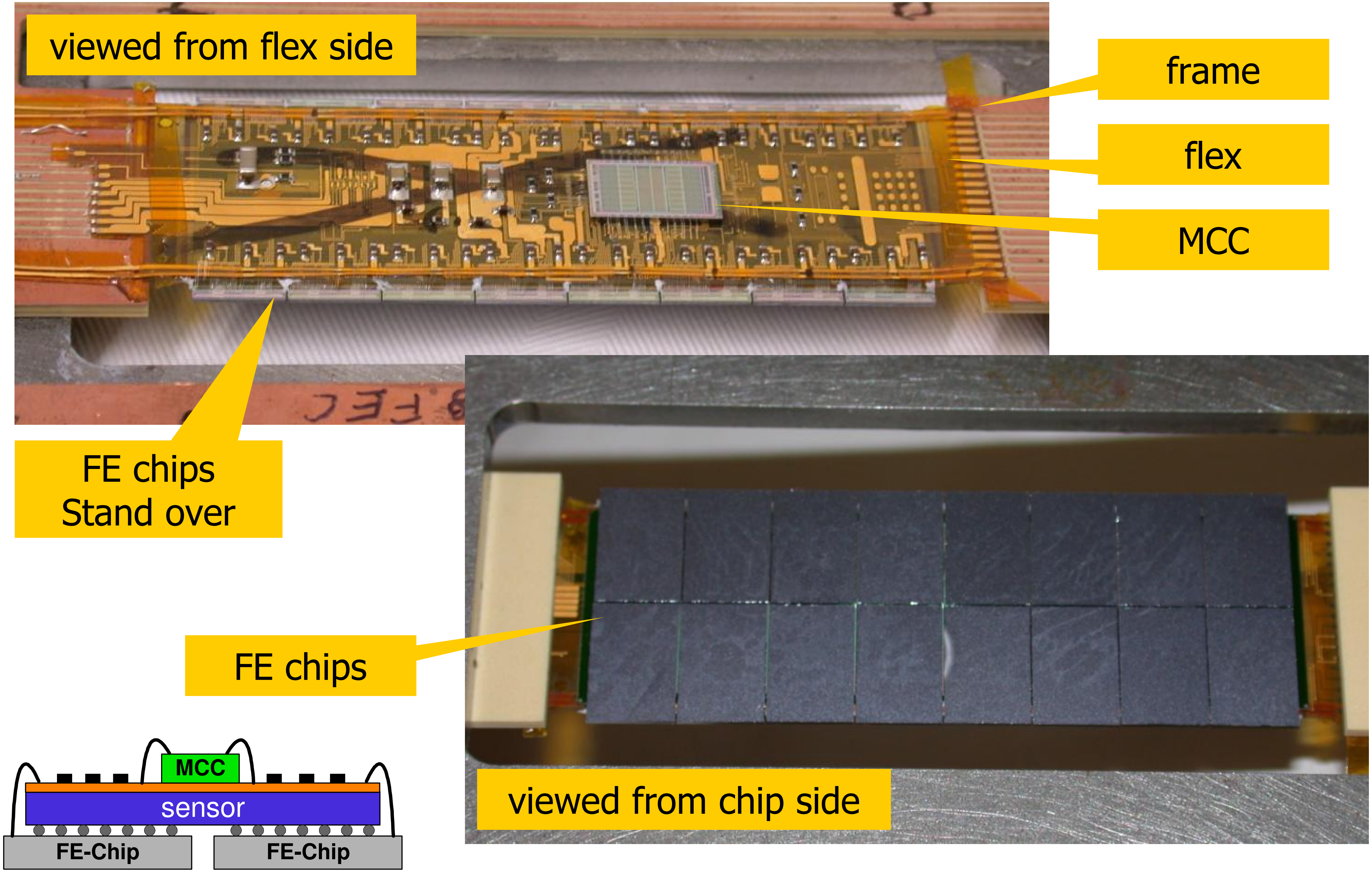


ALL wire bonds must be good!

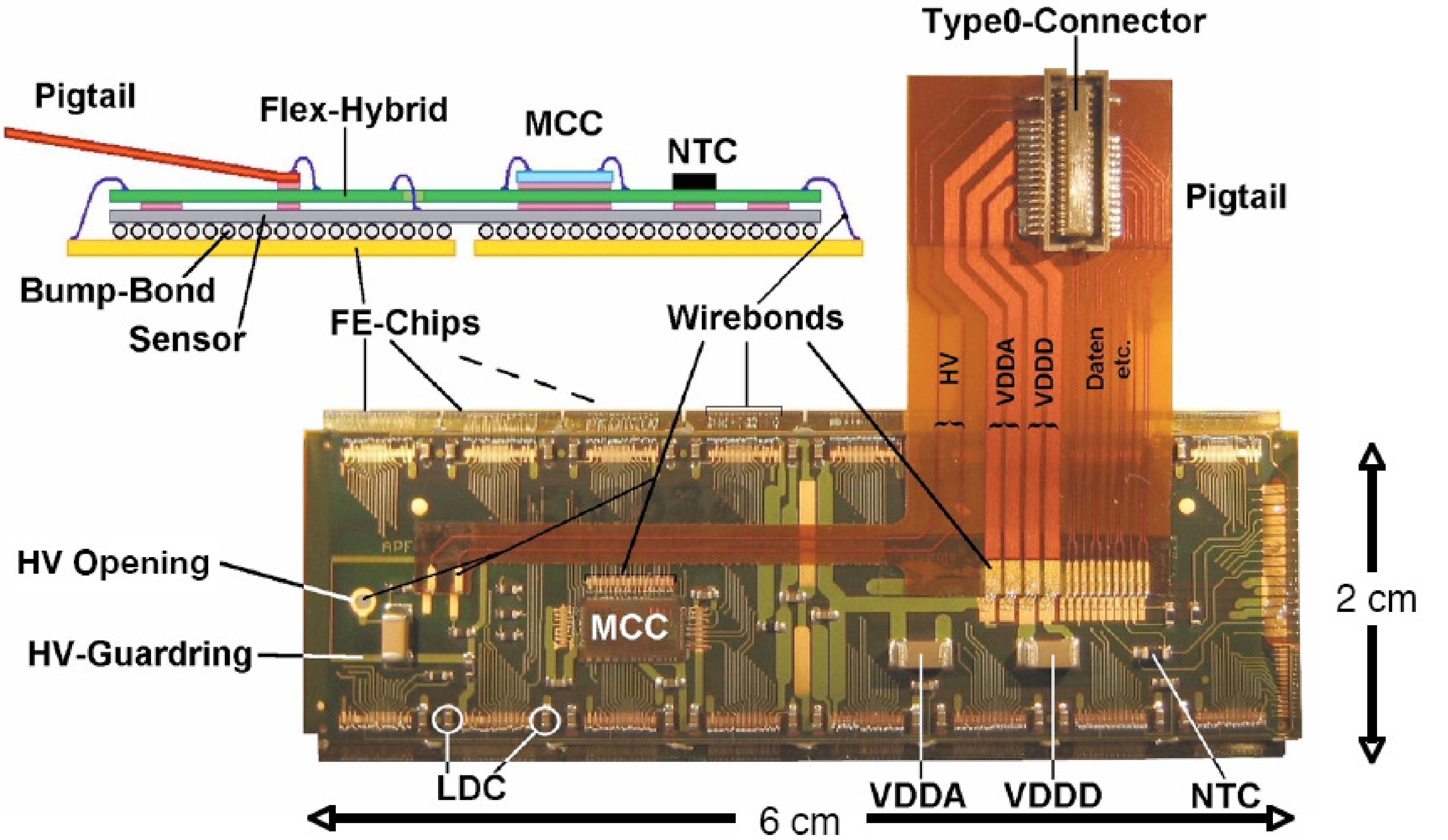




2nd generation: flex module in mounting frame

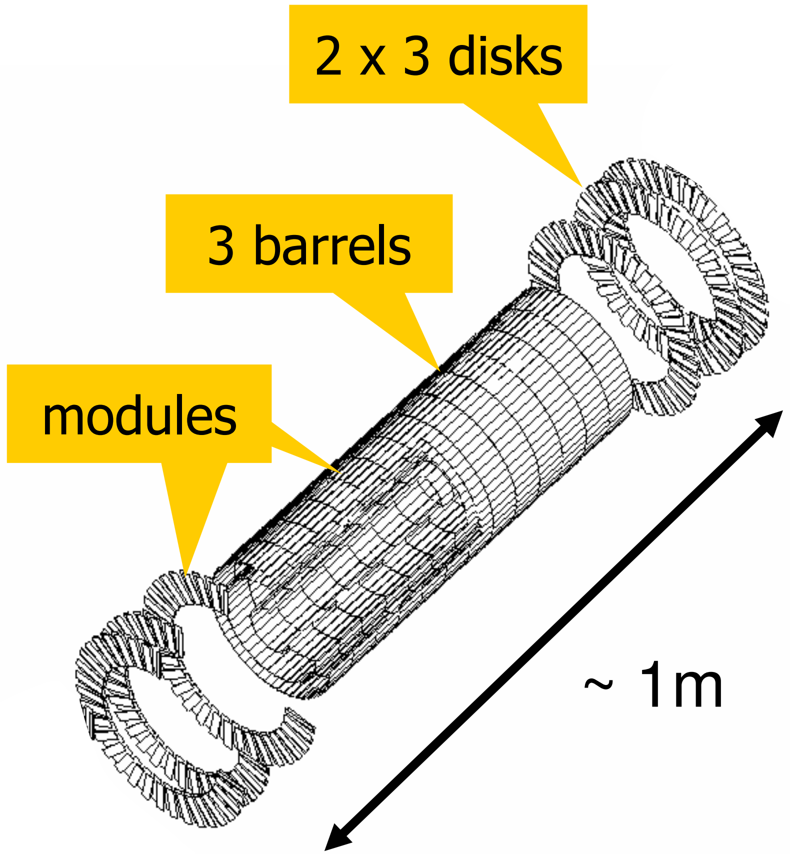


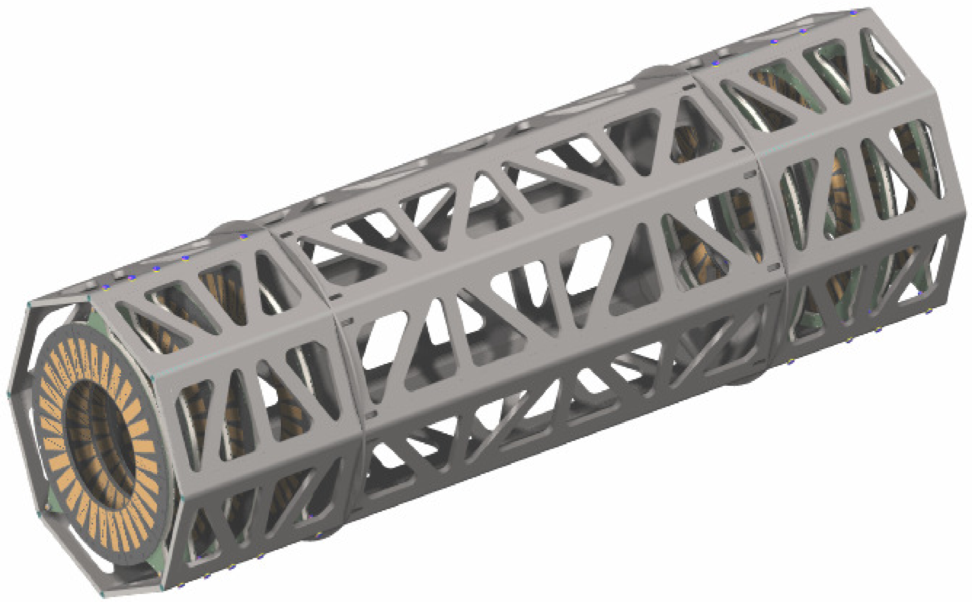
Final Pixel Module



slide by M. Christianzini, Bonn

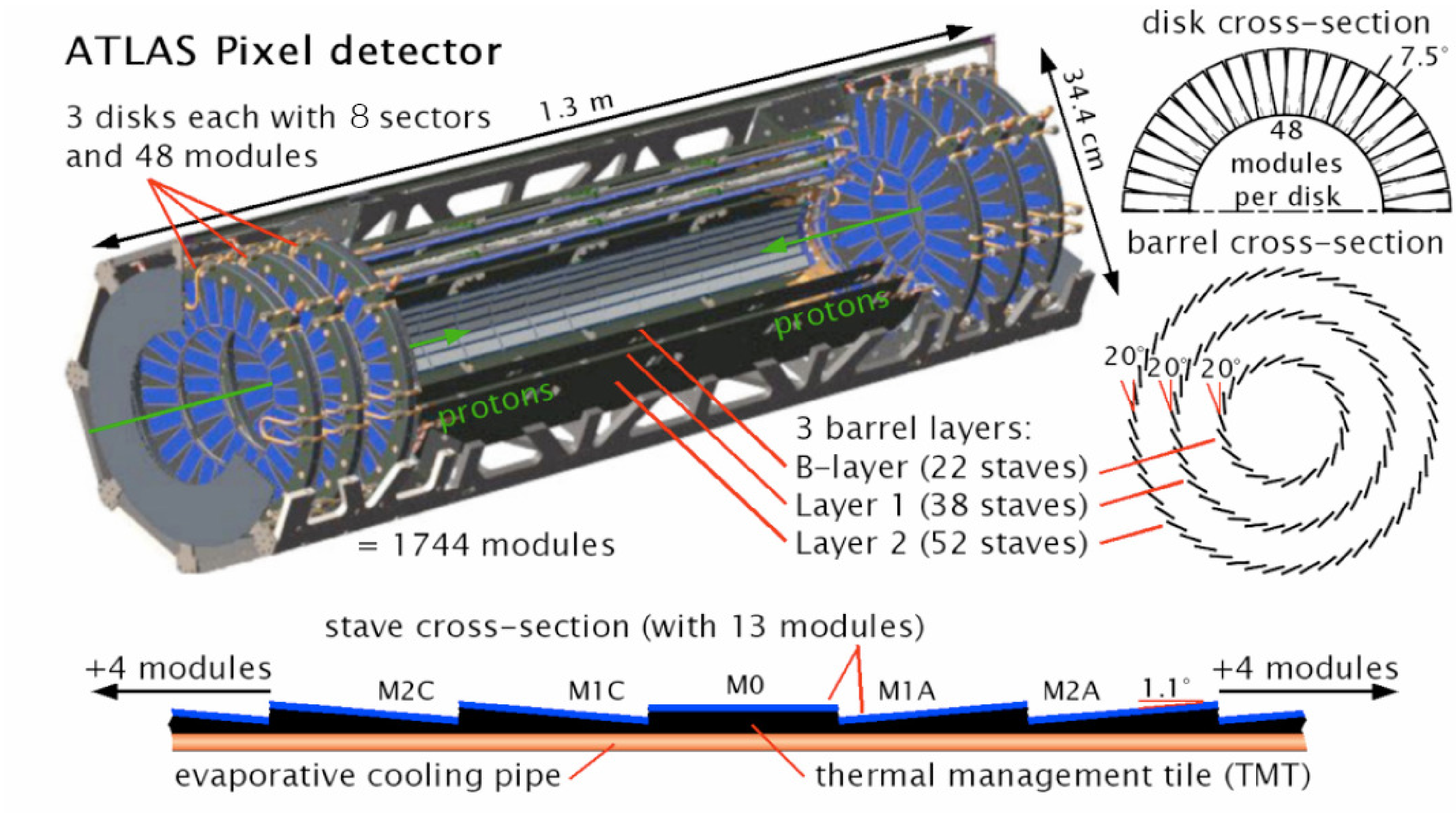
Overall Layout





- Global support is a flat panel structure
- Made from carbon composite material (IVW, Kaiserslautern)
- Total weight is 4.4kg
- 3 pieces, center part consists of two half-shells to open

Geometry Details



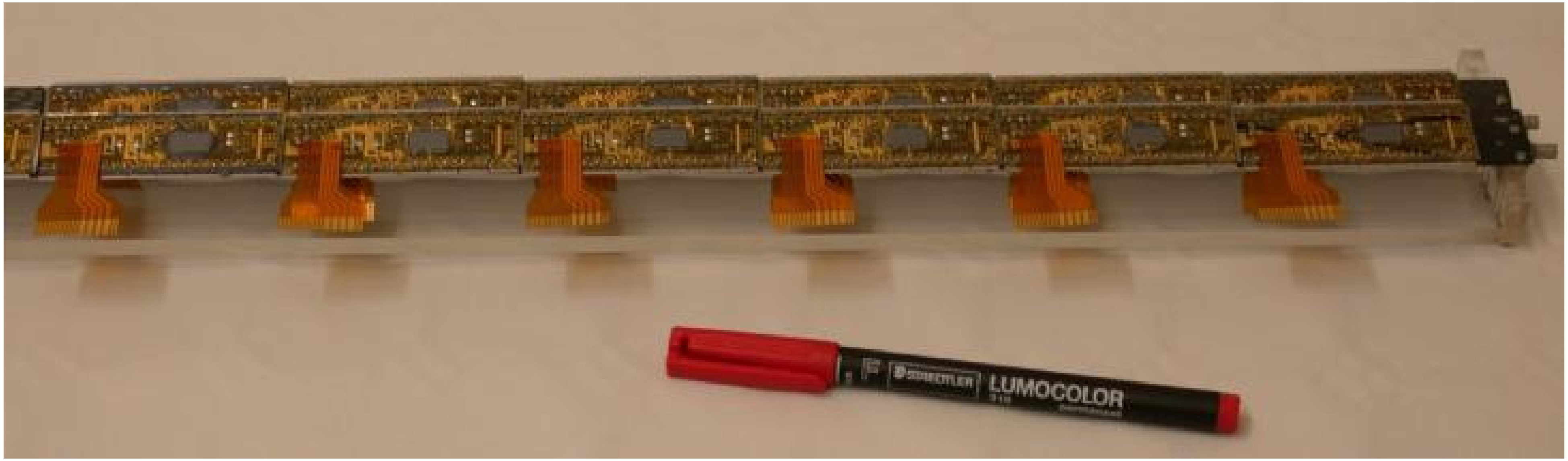
slide by M. Christianzini, Bonn

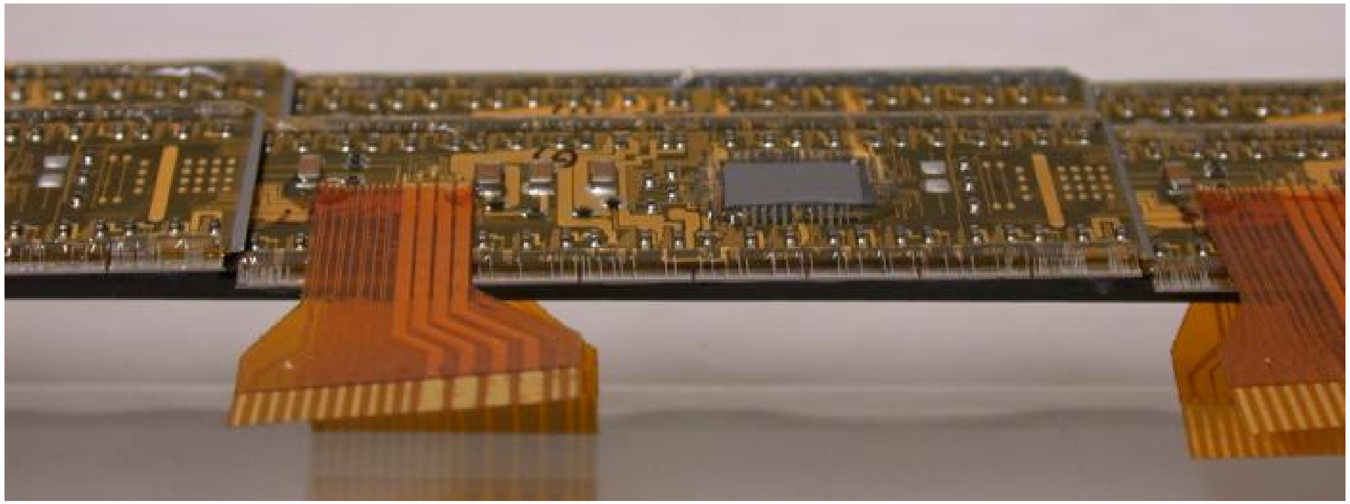
Cooling

- Very important
  - Contributes significantly to material budget
  - Limits the power / performance of electronics
  - Detectors must stay below –6°C to limit damage from irradiation (see later)
- ‚binary ice' solution dropped
  - Cooling power is marginal
  - Fail safe operation for leaks in tubes not possible
  - Liquid is too much material
- ATLAS adopted evaporative cooling:
  - Cooling by evaporation of fluorinert liquid (C_4F_{10} or C_3F_8) @ -20°C. Needs pumping.
  - Low mass (gas!), small diameter tubes (only small pressure drops)
  - Very large cooling capacity
  - Aluminum tubes must withstand 6 atm if pumping stops and coolant develops its full vapor pressure.
- All components must cope with thermal cycling 25°C ⇔ -20°C

Barrels and staves

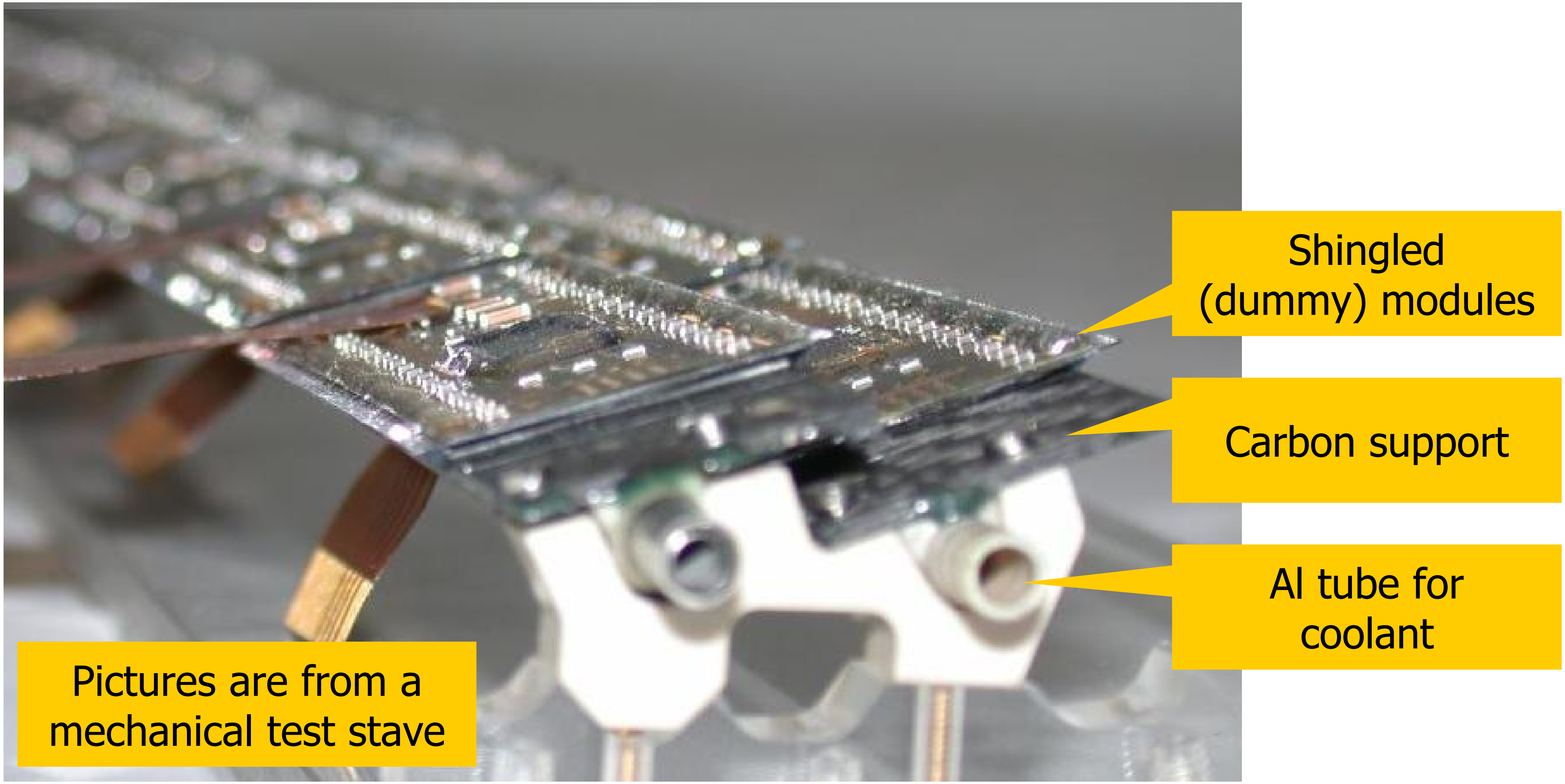
- Barrels are made from parallel staves
- One stave contains 13 modules which are shingled for overlap in z





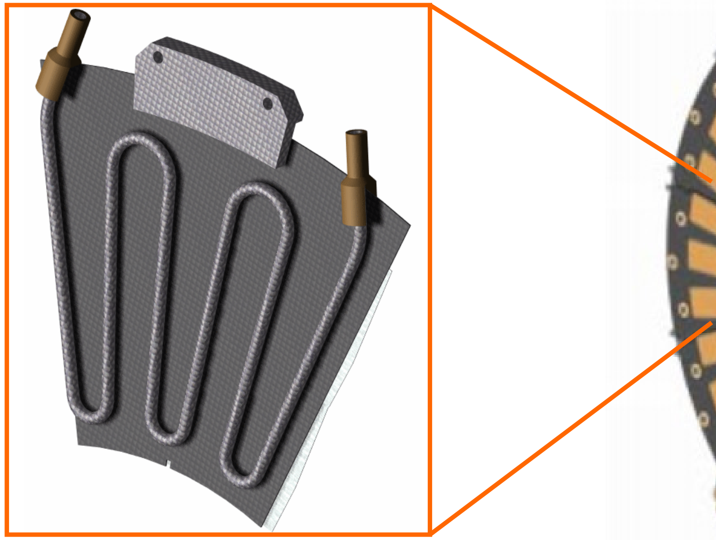
Barrels and staves

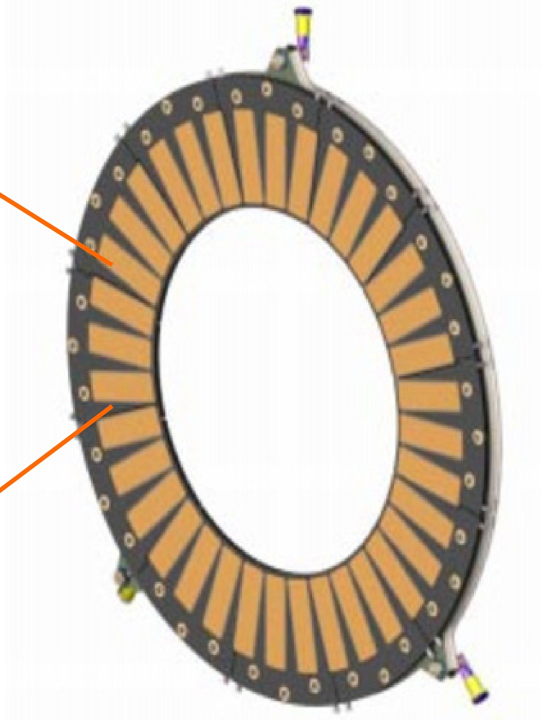
- A Stave is a carbon structure with an Al tube for cooling
- Staves are tilted for overlap in phi (+change sharing)
- Production mainly in Germany, Italy, France

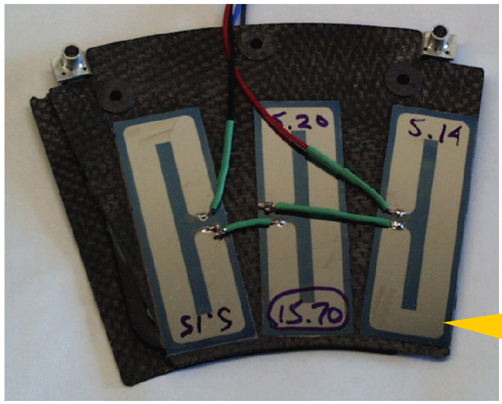


Disks and Sectors

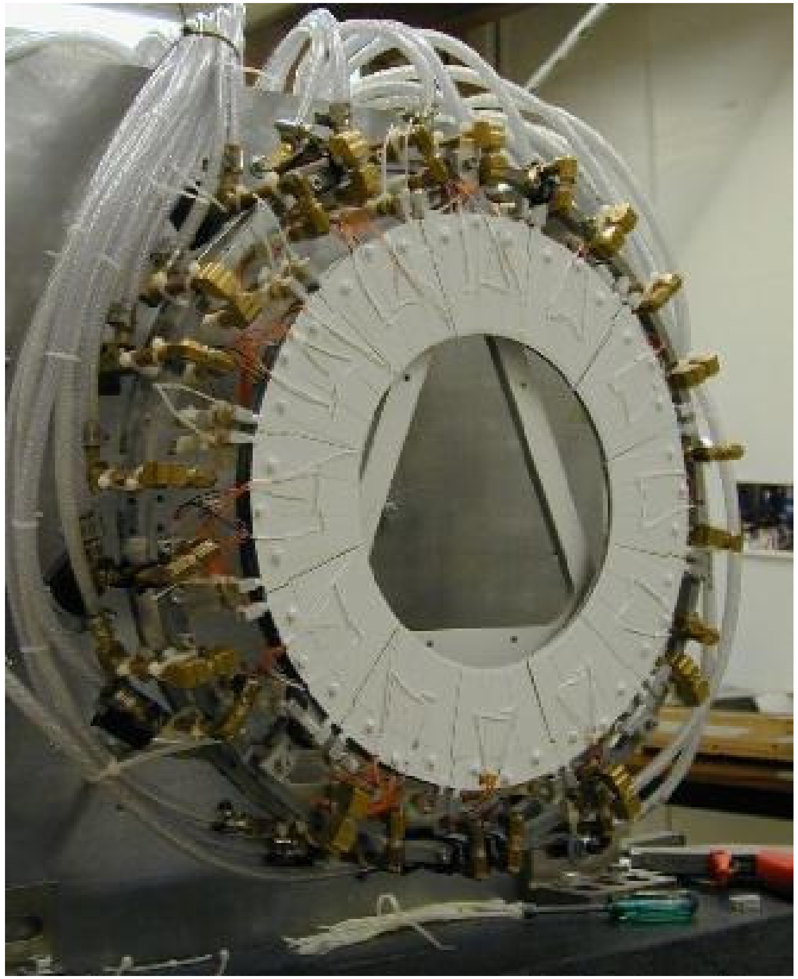
- Disks are divided into sectors
- Coolant flows in tube between two C-C facings
- Modules are arranged on both sides for overlap
- Production in USA







Sector with 3 ‚modules'

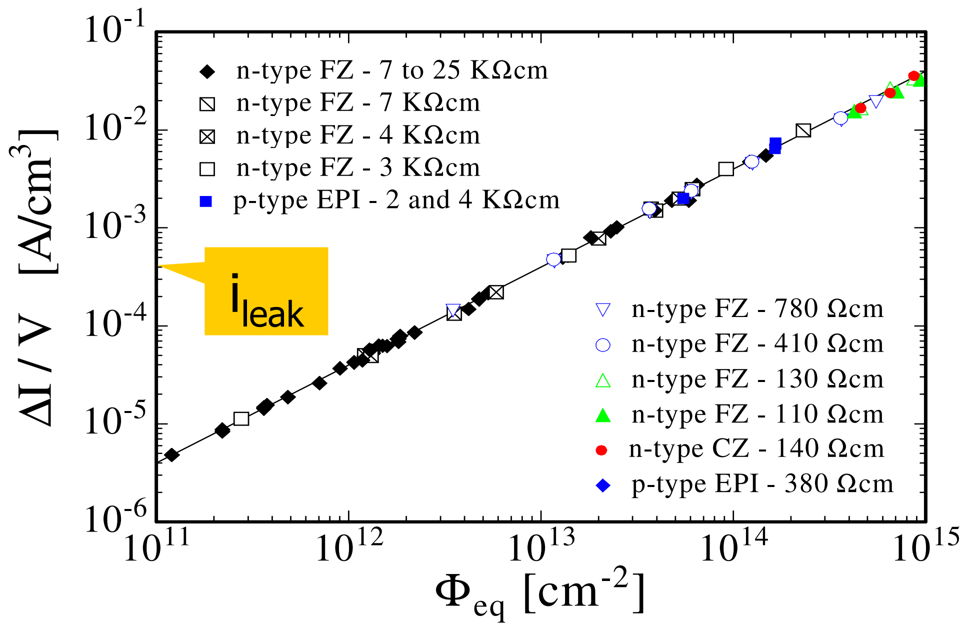


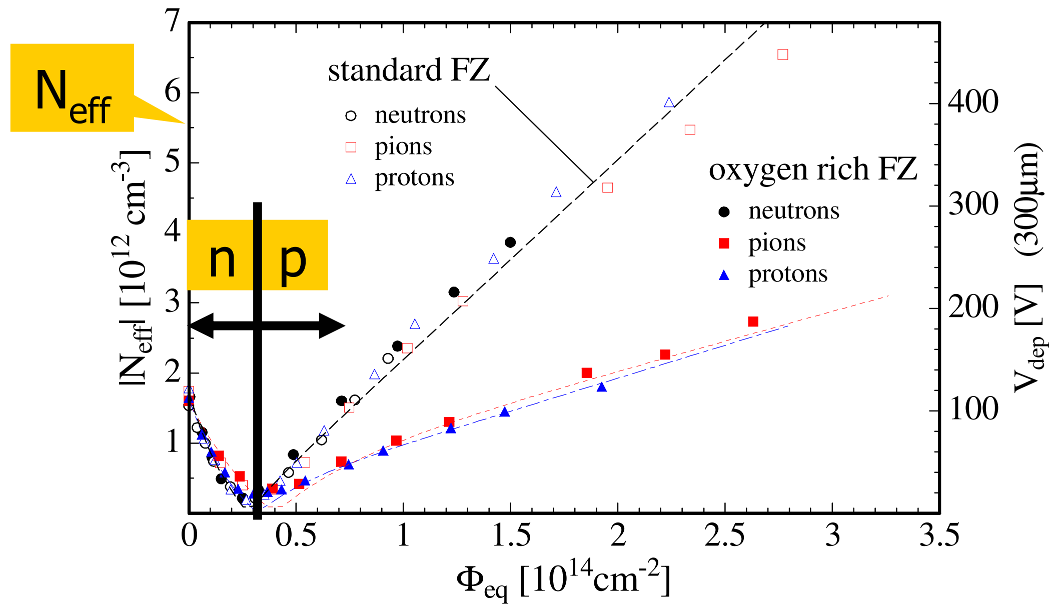
cooling test of full disk
(@ LBNL)

Silicon Pixel Detectors – Today and Tomorrow

Radiation damage of silicon Sensors

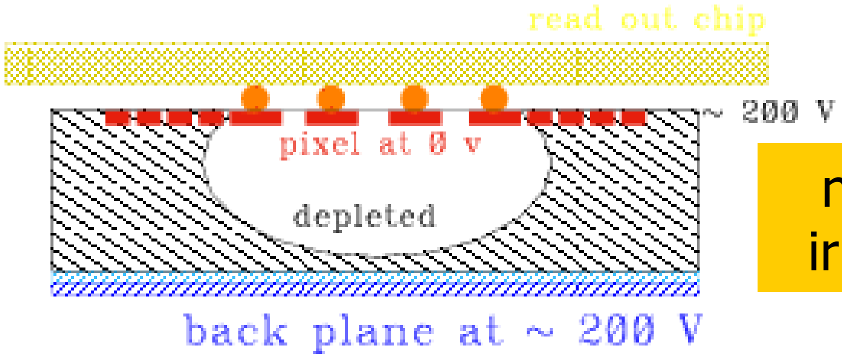
- Irradiation of silicon leads to bulk damage and oxide charges at the surface
- Bulk damage:
  - increased i_{leak} → increased noise
  - ‚reverse annealing' → keep sensor cold (- 6⁰C)
  - Type inversion → n-side readout
  - Change in doping → increased depletion voltage (guard rings!) , partial depletion
- Oxide charges:
  - increased field strength → special designs



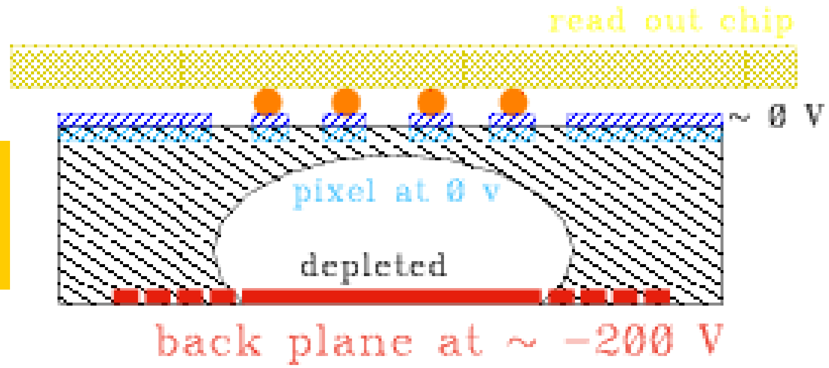


Problem of type inversion

p^{+} pixels on n^{-} material

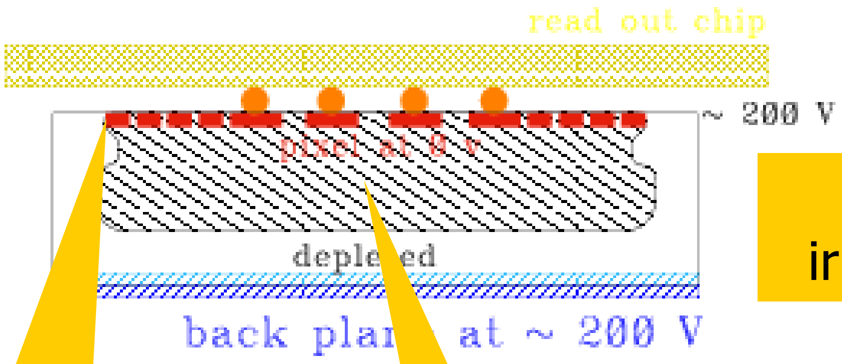


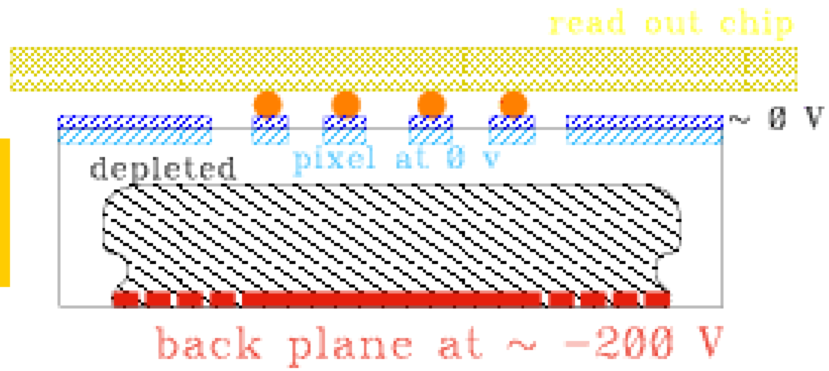
n^{+} pixels on n^{-} material



n^{-} before irradiation

p^{-} after irradiation





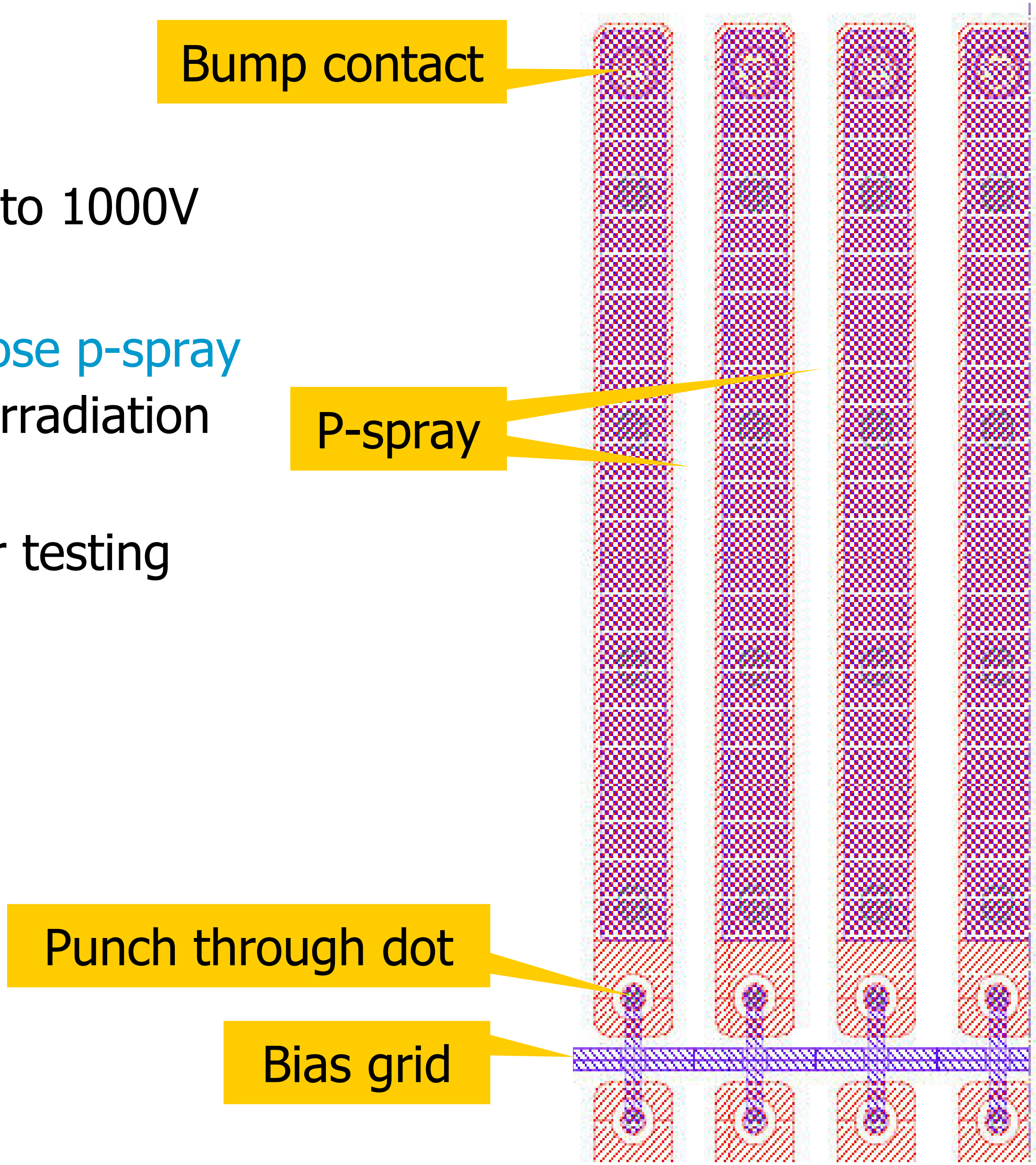
Voltage drop on Readout side

Need full depletion!

Can be operated partially depleted

ATLAS pixel sensor development

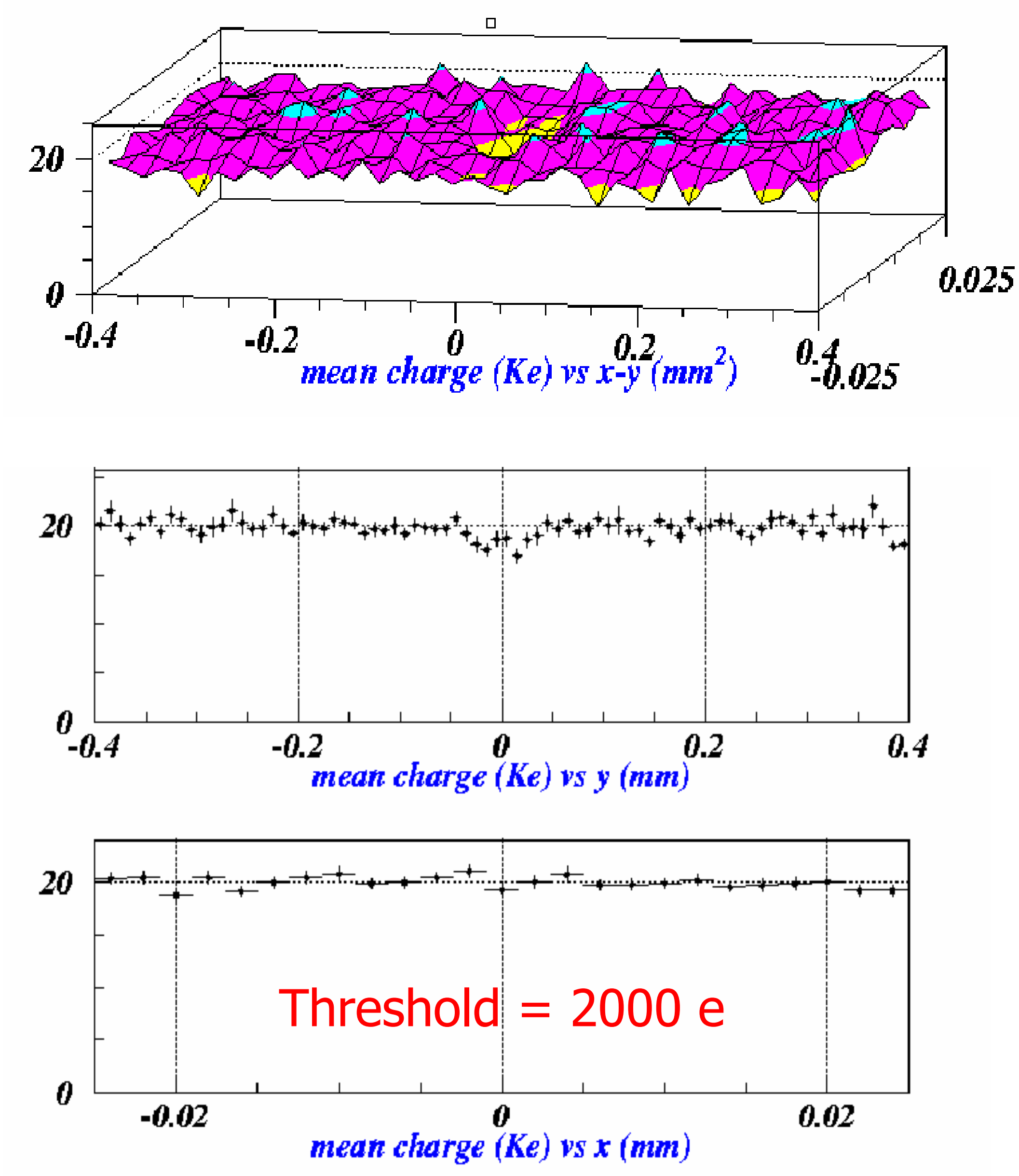
- n+ pixels in n- sensor
- Multi guard ring structures hold up to 1000V
- Isolation of pixels with moderate dose p-spray has highest field strength BEFORE irradiation
- Punch through dot and bias grid for testing before bumping
- Use of oxygenated silicon



Performance of irradiated sensor

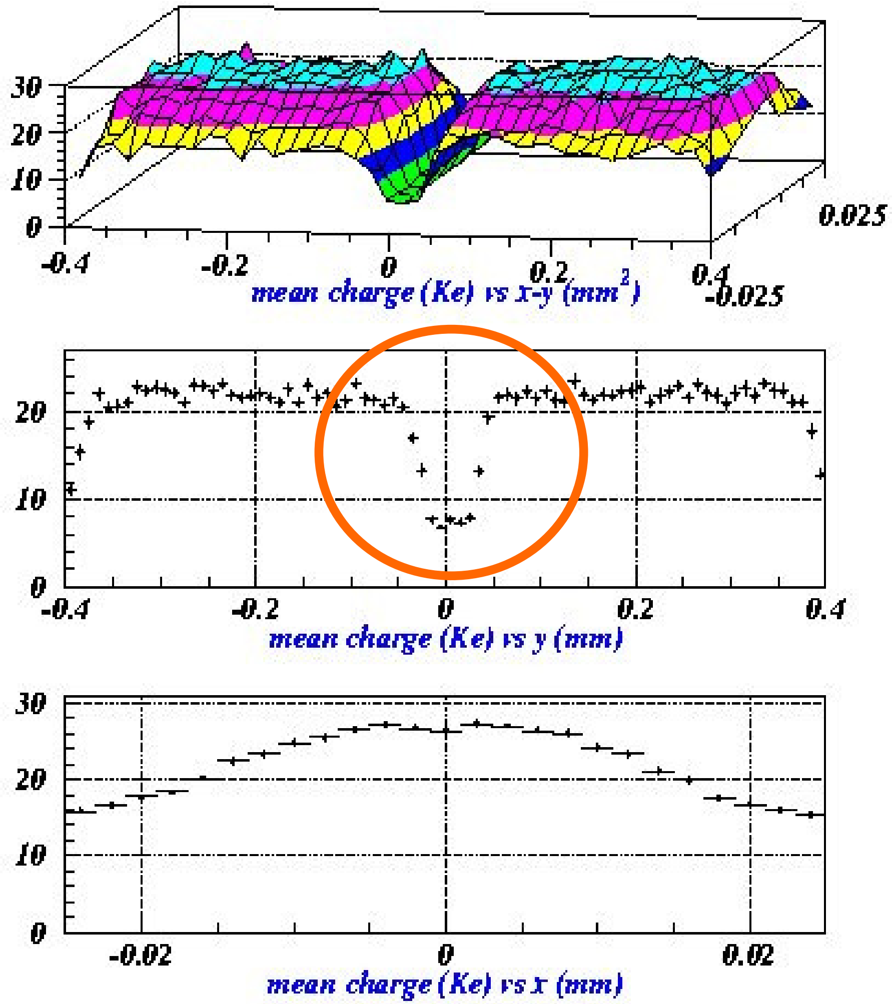
- Sensors are irradiated to full ATLAS fluence (10^{15} n_{eq}/cm^2)
- They are then bump bonded to rad-soft ATLAS Prototype FE-Chips
- Measurements are performed in test beam with a Si-Strip telescope as reference detector
- Pixel Chips give some information about collected charge.

- V_{bias} > 600V possible!
- Homogenous charge collection also in pixel corners
- These sensors will survive 10 years of ATLAS operation!

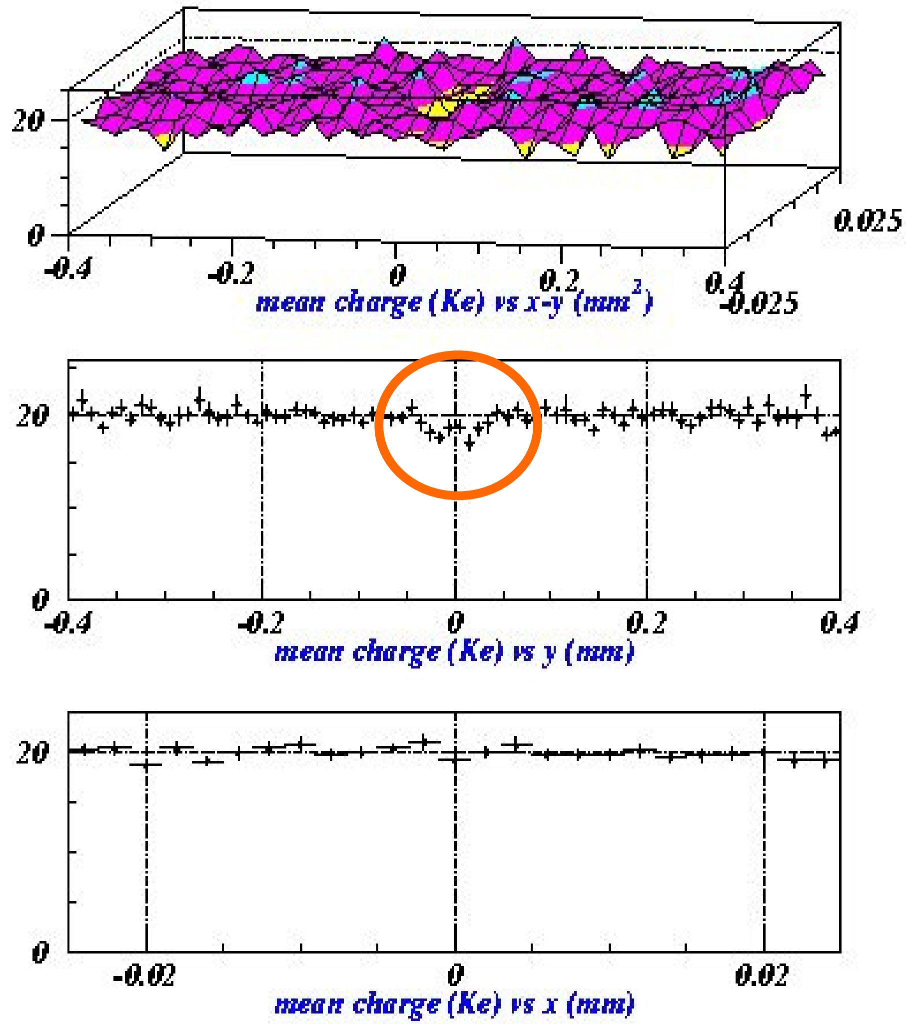


Comparison of Sensor designs

Design with losses at pixel edge

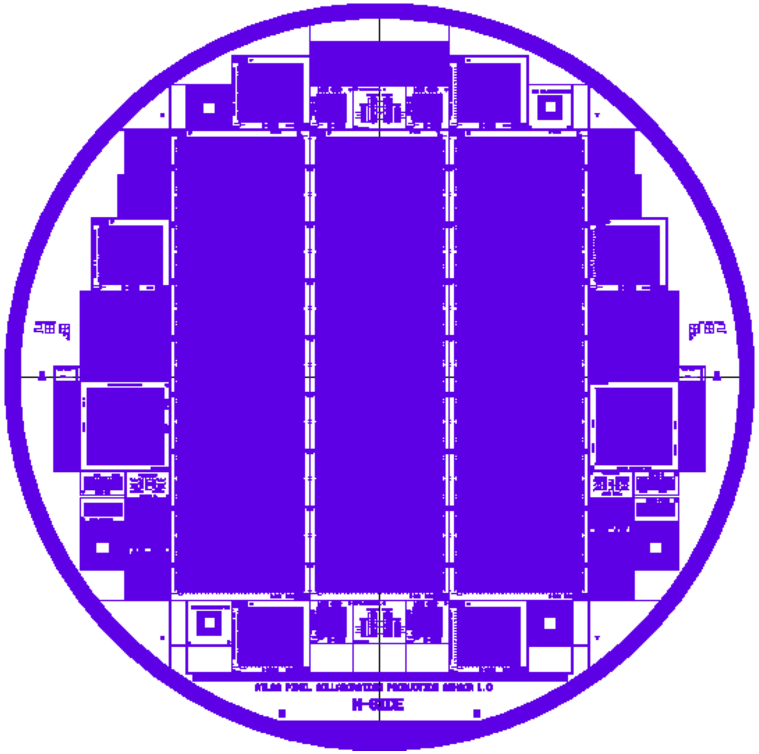


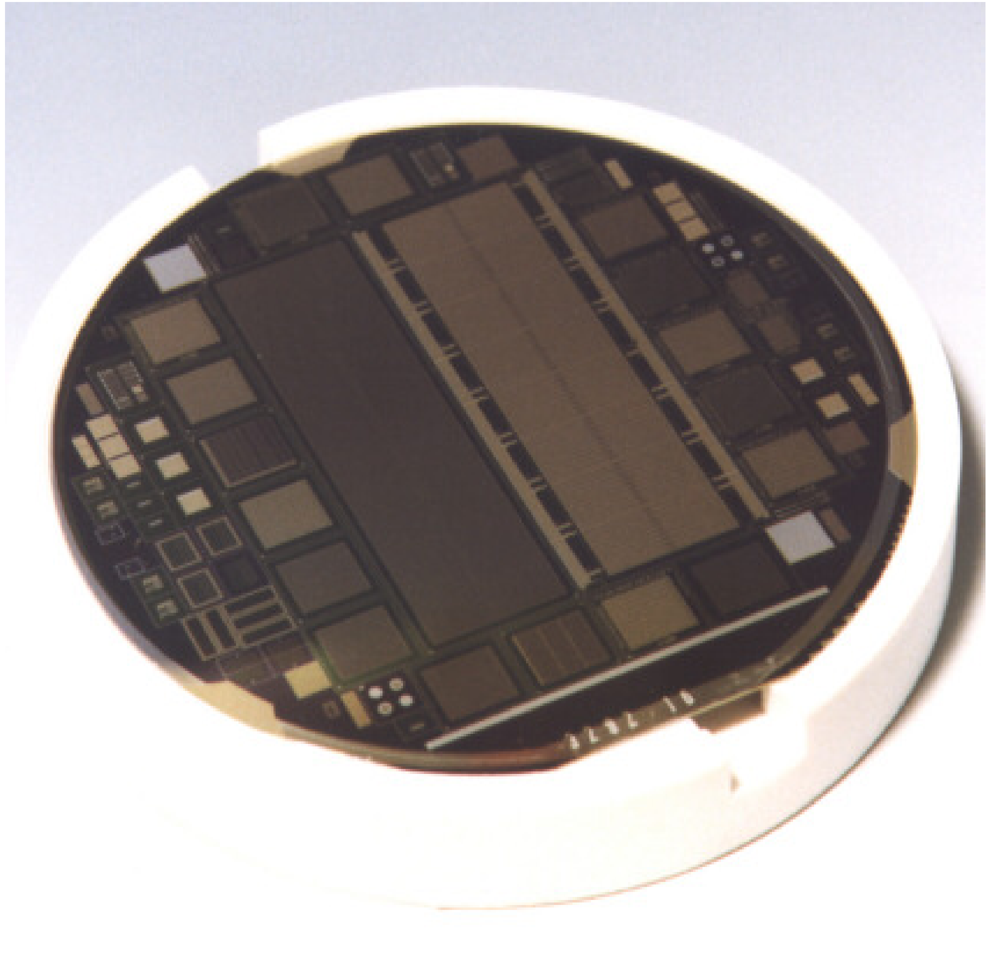
final design with punch through dot



Production sensor

- 3 prototyping generations optimized
  - geometry
  - isolation technique (p-stop vs p-spray)
  - biasing
  - charge collection efficiency
  - radiation hardness
- Very good final design!





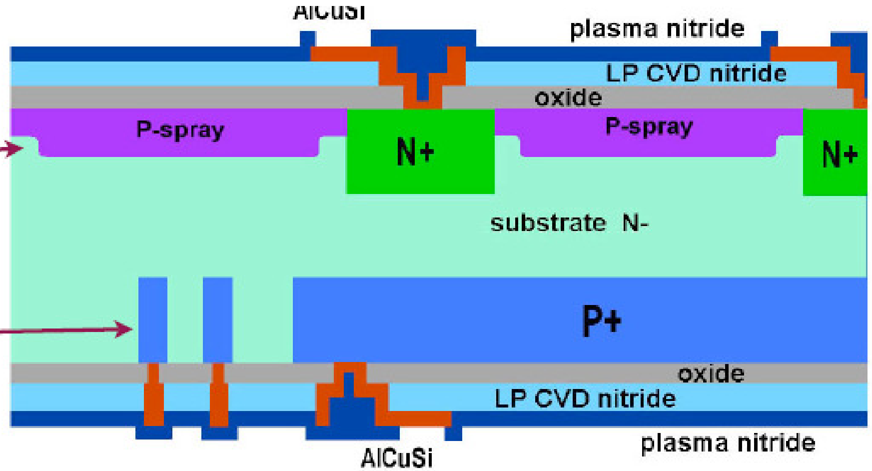
ATLAS prototype sensor wafer
2 sensors + test structures
(Teflon chuck for double sided probing)

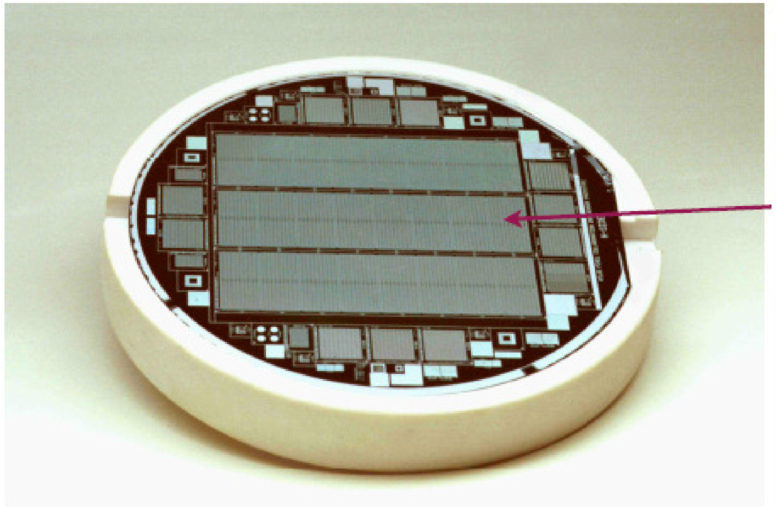
Sensor details

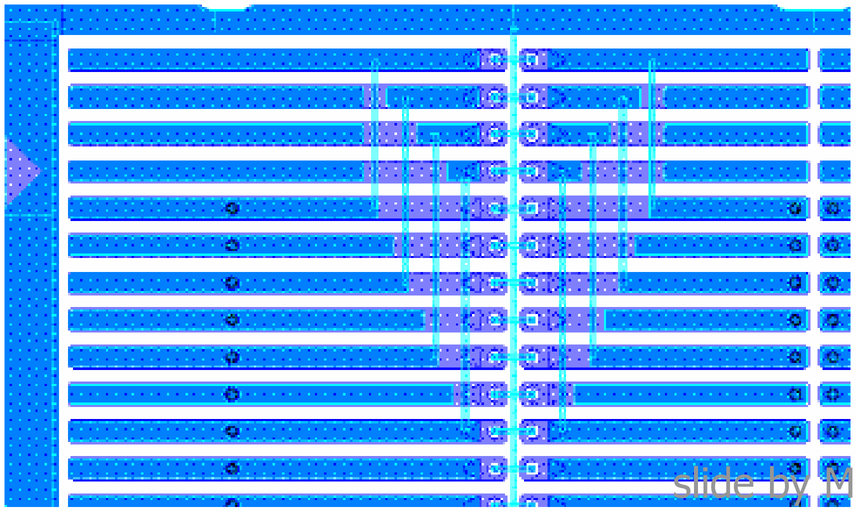
- Design driven by radiation hardness requirement
  - n^+ pixels in n-bulk (oxygenated Si) with moderate p-spray
  - 16.4 mm x 60.8 mm x 280μm , 46080 pixels (50x400 μm²)

isolation of n+ implantations:
moderated p-spray

multi guard ring
on the p-side







Special pixels in inter-chip region

“long”,”ganged”

slide by M. Christianzini, Bonn

Silicon Pixel Detectors – Today and Tomorrow

Why pixels?

- Requirements and challenges

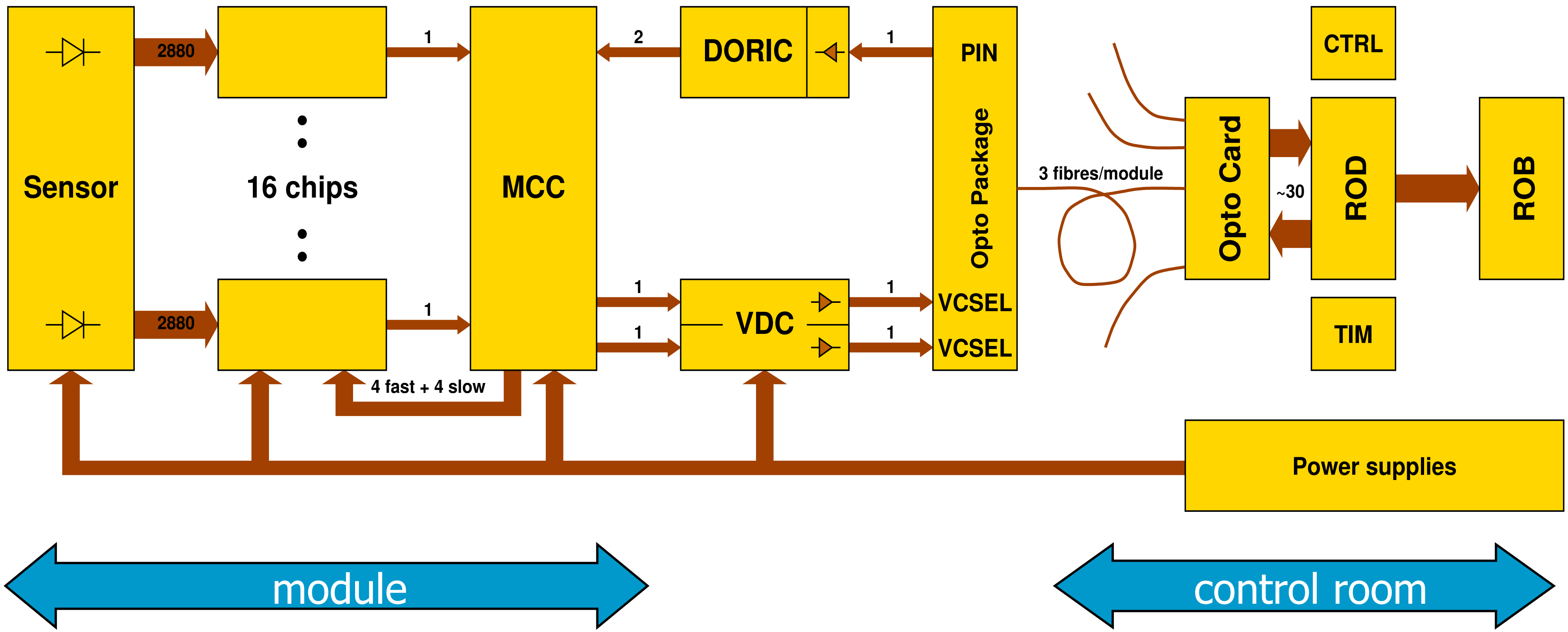
The ATLAS pixel detector

- Modules, mechanics etc.
- The sensor
- The front end electronics
- Some results / status

The next generation (for TESLA)

Other applications of hybrid pixel detectors

Electronic Components of the Pixel System



1	Sensor	
16	front end chips	(FE)
1	module controller chip	(MCC)
2	VCSEL driver chips	(VDC)
1	PIN diode receiver	(DORIC)

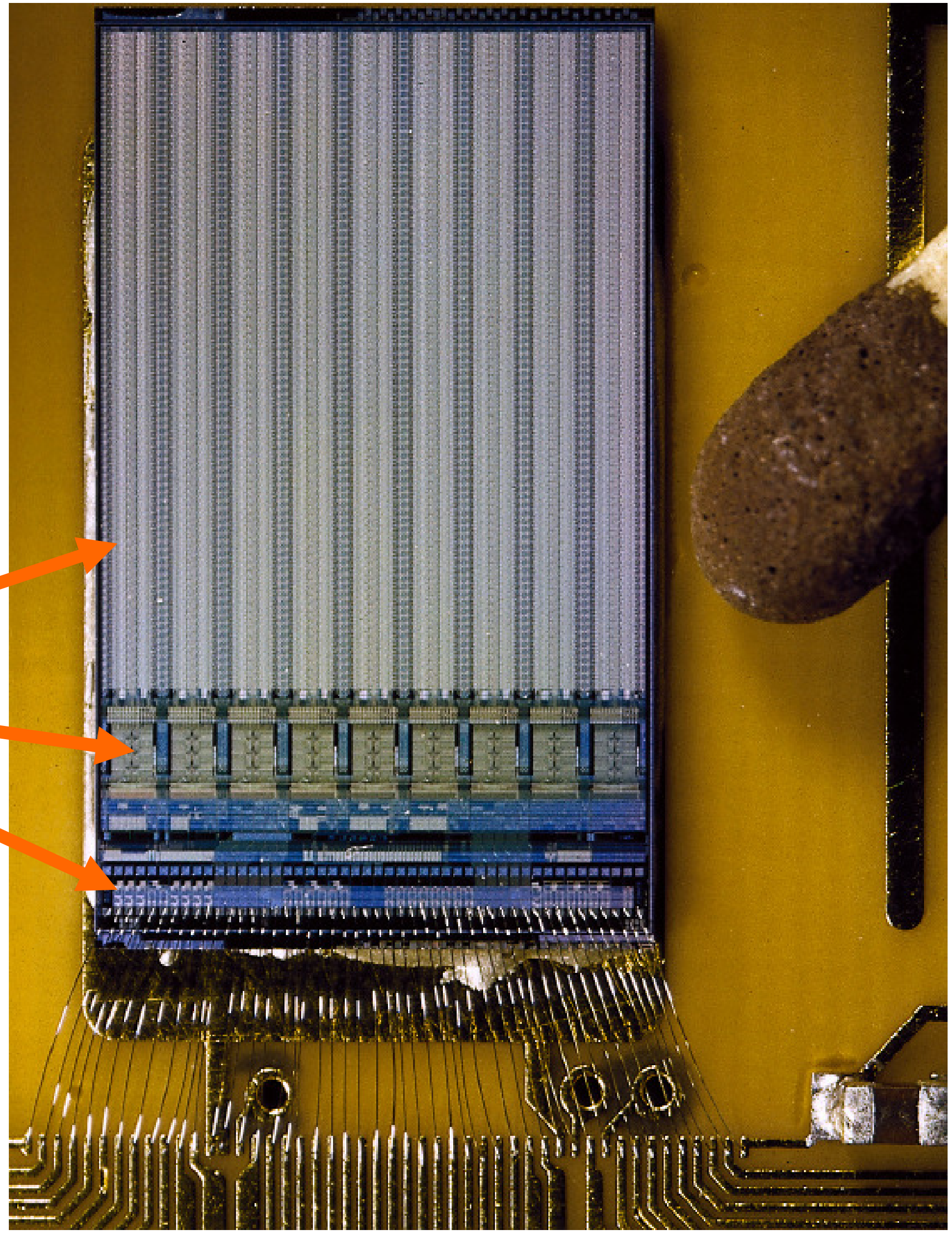
Optical receivers	
Readout Drivers	(ROD)
Readout Buffers	(ROB)
Timing Control	(TIM)
Slow Control, Supplies	

The Front End Chip

- Chip size: 7.4mm x 11mm
- Pixels: 18 x 160 = 2880
- Pixel size: 50µm x 400µm
- Technologies: 0.8µm CMOS (FEA,FEB)
  0.8µm BiCMOS (FED)
  0.25µm CMOS (FEI)

- Operates at 40 MHz
- Zero suppression in every pixel
- Data is buffered until trigger arrives
- Serial control and readout, LVDS IO

- Analog part with
  - 40 µW power dissipation / Pixel
  - ~200 e noise
  - Amplitude measured via pulse width

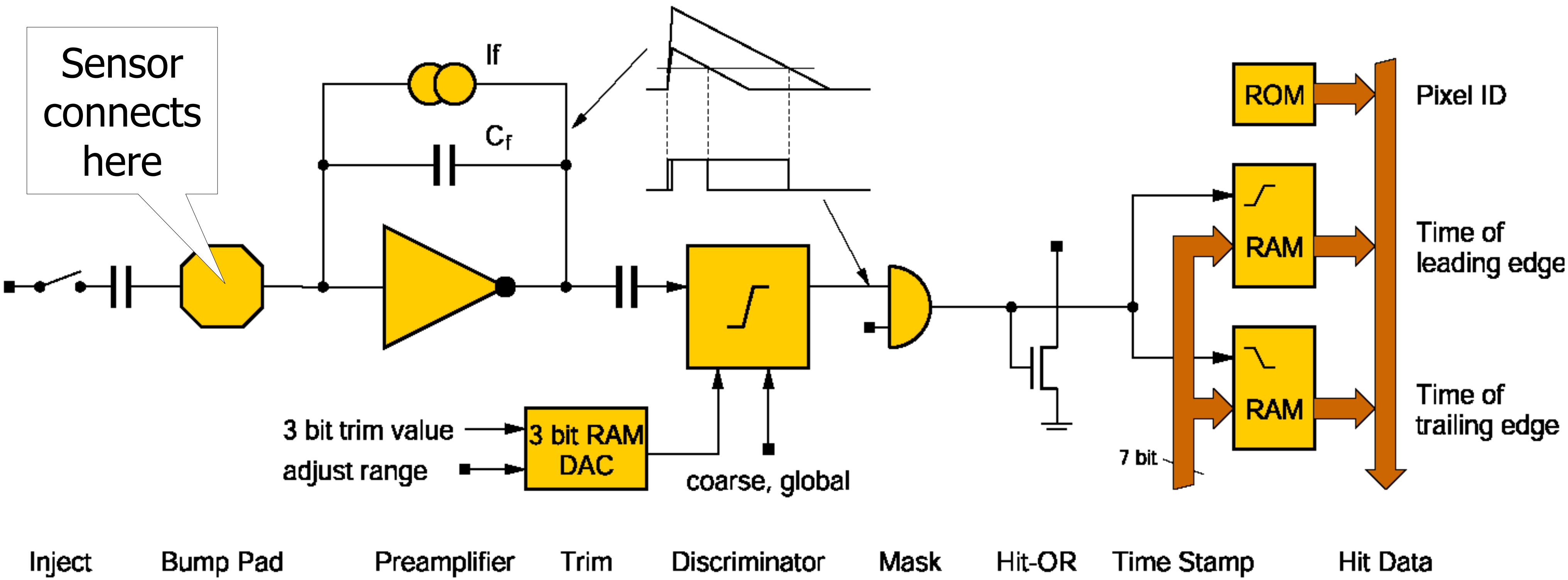


Pixel Analog Part

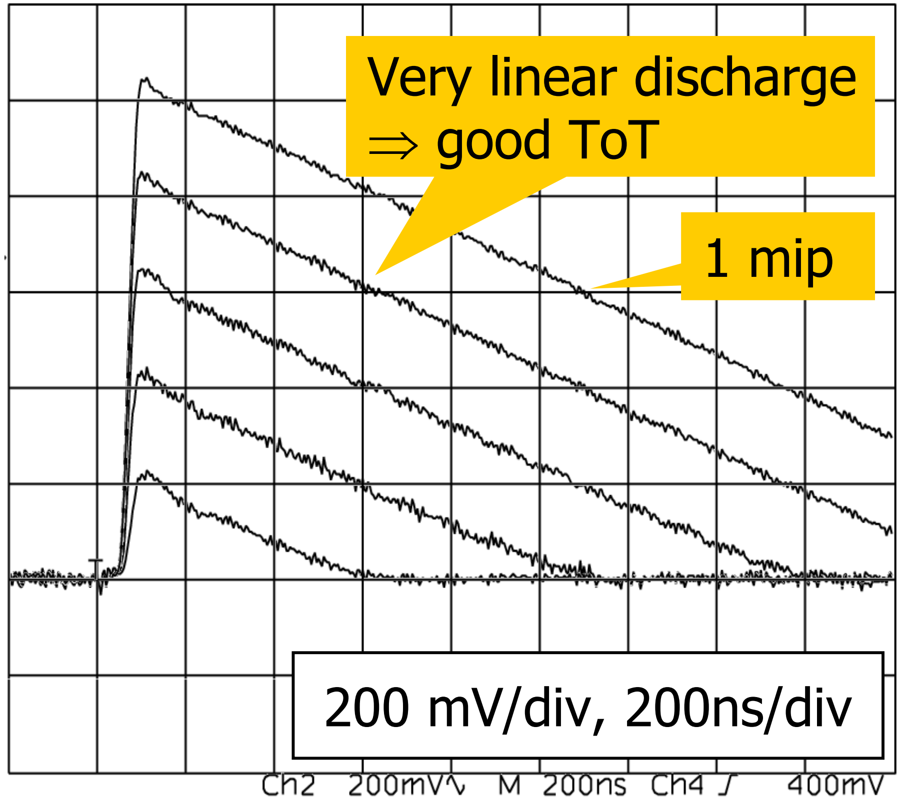
feedback uses constant current
- high stability for fast shaping
- tolerates > 100 nA leakage
- linear decay

Analog information
- measure width of hit
- works nicely due to linear discharge

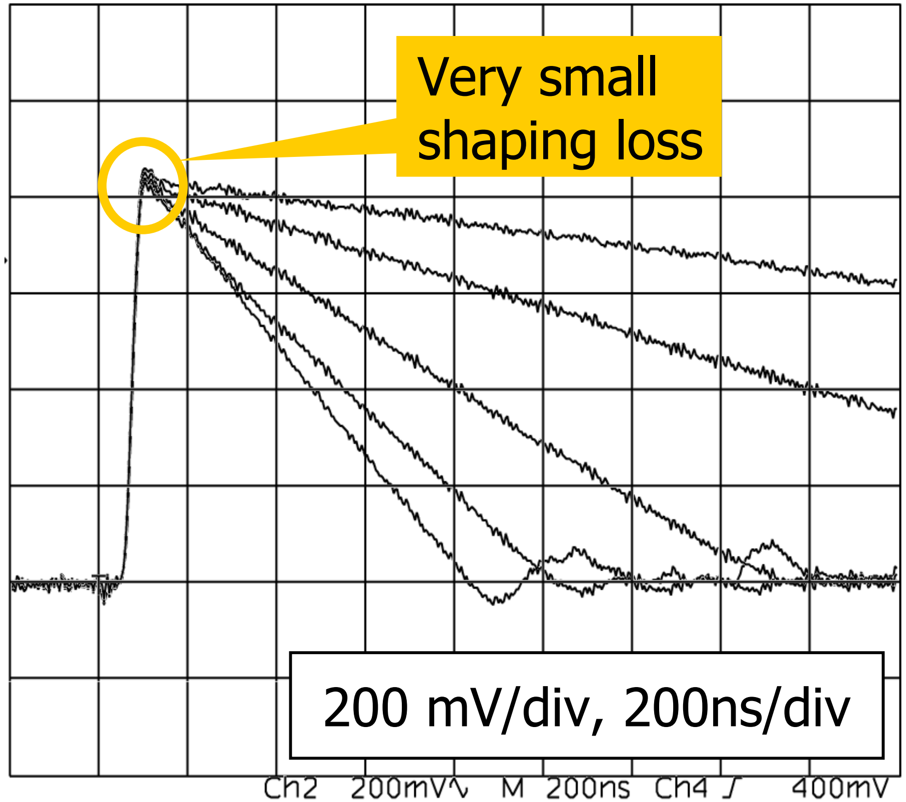
Individual adjustment of
- Threshold
- feedback current (FEI)
- ranges are adjustable



FED: Preamplifier Pulse Shapes



Different injected charges



Different feedback currents

(Measured on FED test chip with internal chopper, no sensor)

Data Readout

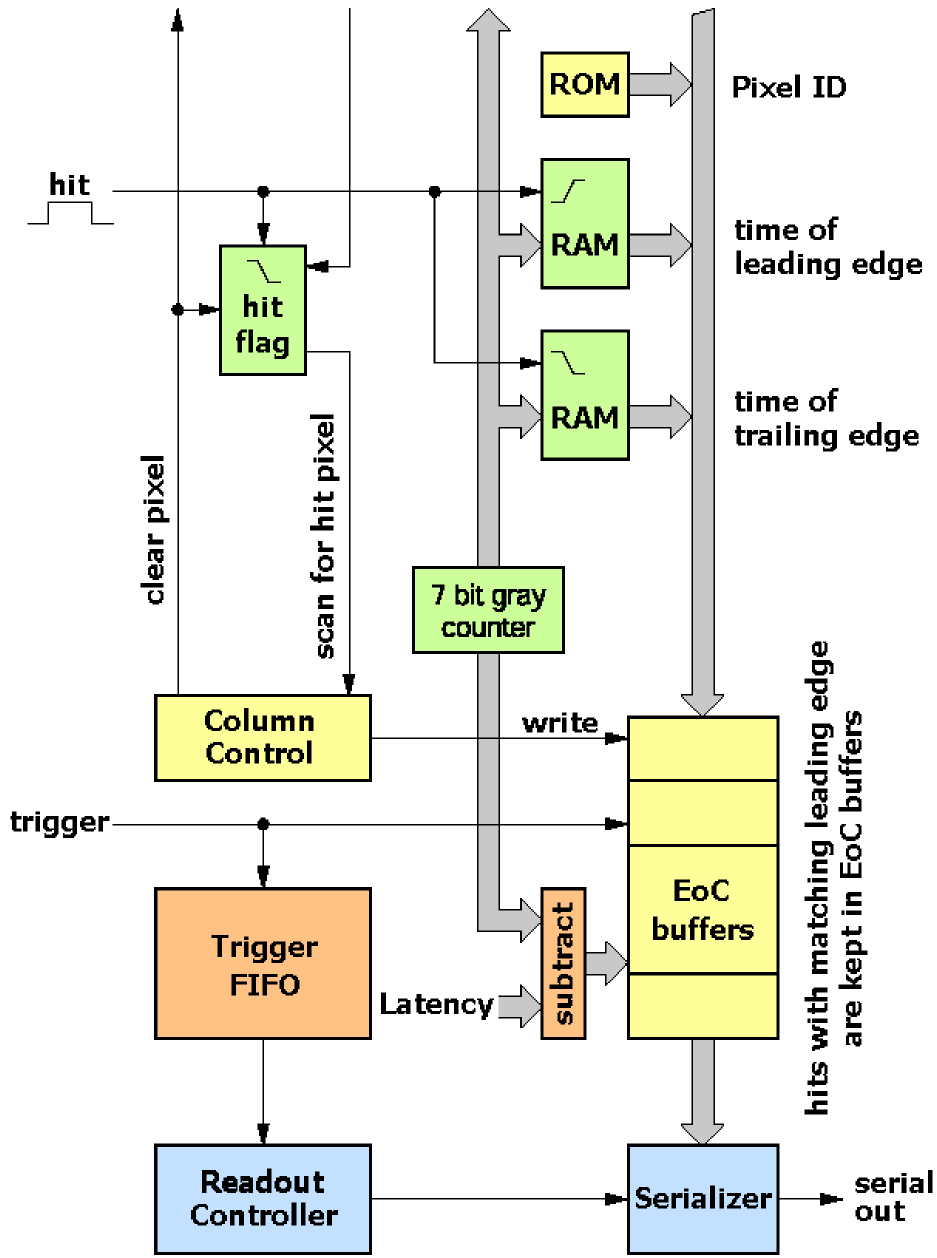
4 simultaneous tasks are running permanently:

- A time stamp (7bit Gray Code) is distributed to all pixels
- When a pixel is hit, the time of rising and trailing edges are stored in the pixel

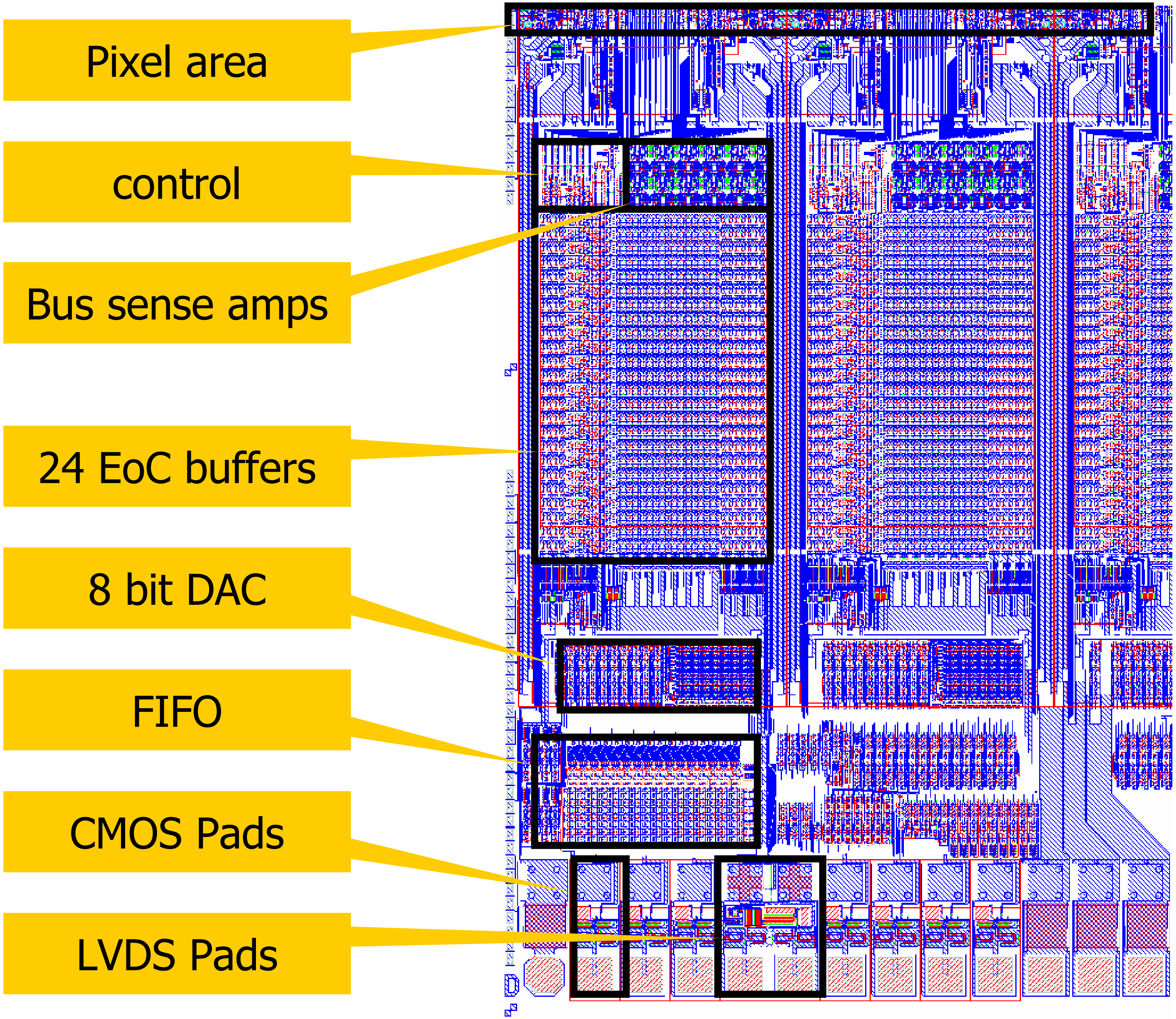
- The hit is flagged to the periphery with a fast asynchronous scan
- Time information and pixel number are written into a buffer pool (common to a column pair)
- The hit in the pixel is cleared

- If a trigger arrives, the time of the hit (leading edge data) is compared to the time for hits associated to this trigger. Valid hits are flagged, older hits are deleted.
- The trigger is queued in a FIFO

- All valid hits of a trigger are sent out serially. All triggers in the FIFO are processed.



Layout of FED chip (bottom left)



Radiation damage to the electronics

- Pixel chips are traversed by all particles -> irradiation is very high

- Problem: increasing positive oxid charge.
  - threshold shifts of the FETs
  - Generation of parasitic FETs. current flows ‚arround' the gate and between FETs.
- Also: (rare) deposition of large charges in storage nodes
  - stored bits can flip (‚single event upset', SEU). ⇒ special designs for logic & RAMs

- Two possible Solutions:

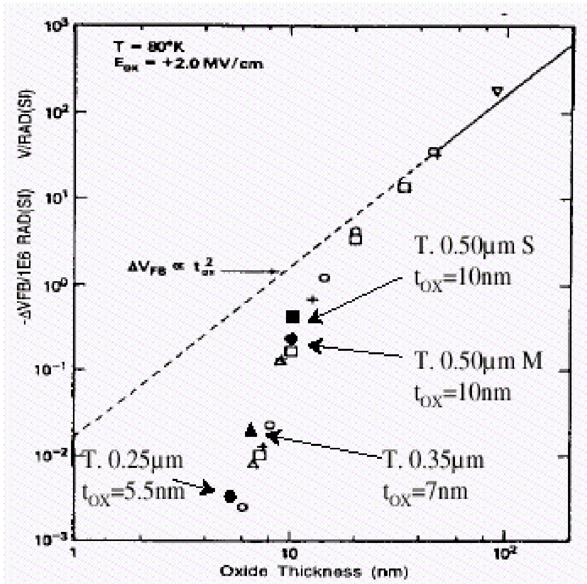
  - use specialized rad-hard technology (DMILL, Honeywell - only few vendors left...)
    - We have done a full FE chip (2 submissions) in DMILL.

      We have dropped this technology mainly because of the extremely poor yield.

  - use a deep-submicron technology (DSM, $L_{gate} \leq$ ¼µm) with special layout rules.

Radiation tolerant design approaches

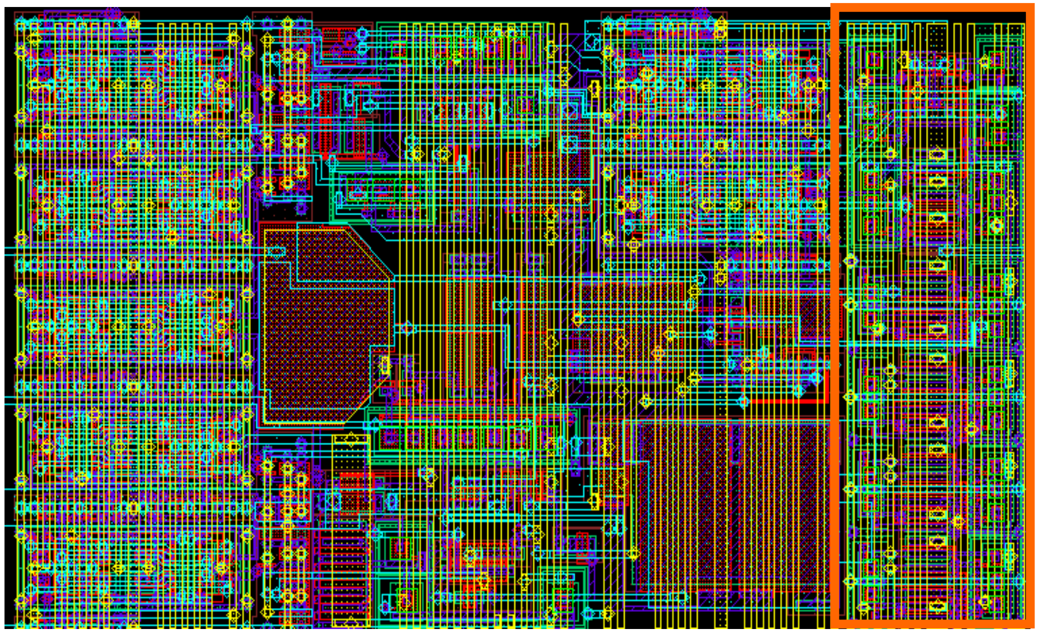
- Use specialized rad-hard technology (DMILL, Honeywell - only few vendors left...)
  - ATLAS has done a full FE chip (2 submissions) in DMILL.
    We have dropped this technology mainly because of the extremely poor yield.
- Use a deep-submicron technology (DSM, $L_{gate} \leq$ ¼µm) with special layout rules.
  Radiation hardness is achieved by:
  - The thin gate oxide (5nm). Holes generated by ionizing radiation can tunnel out of the gate oxide so that threshold shifts become very small
  - Leakage current 'around' the gate (bird's beak) under the (thick) field oxide is eliminated by annular NMOS devices. This would lead to much too large layouts in coarser technologies.
  - Current between devices is eliminated with p+ guard rings (substrate contacts)



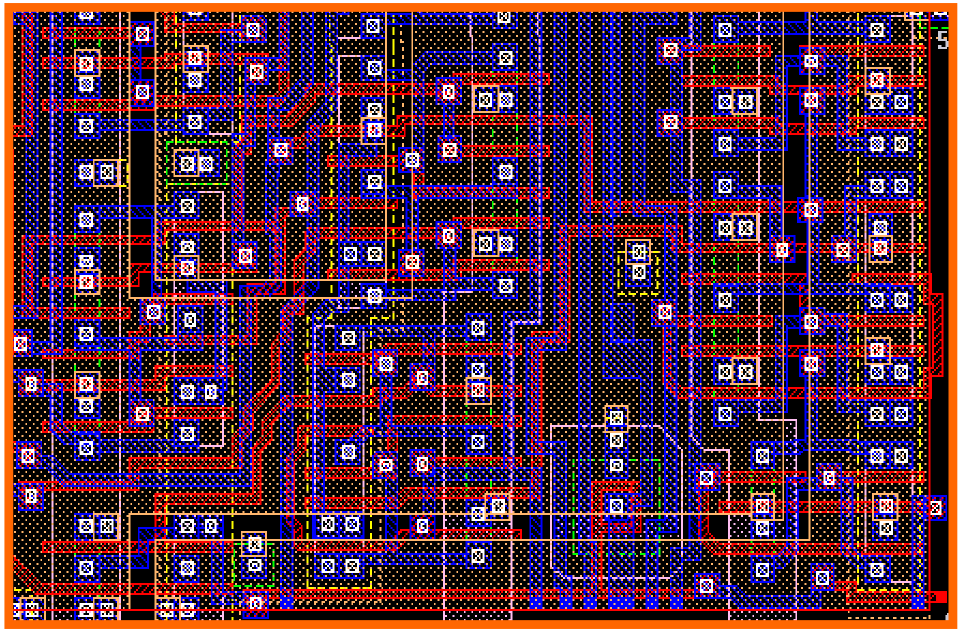
Saks 84, RD49 (1MRad)

  - These technologies are available to outside customers since few years only.
    This was not an option when chip development started...

Layout comparison: 0.8µm ⇔ annular 0.25µm



Pixel of ATLAS FE chip

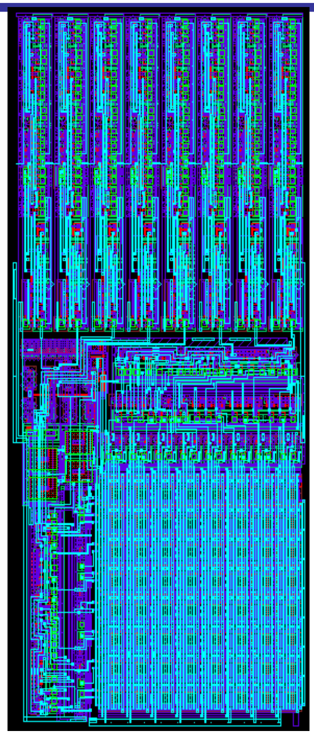


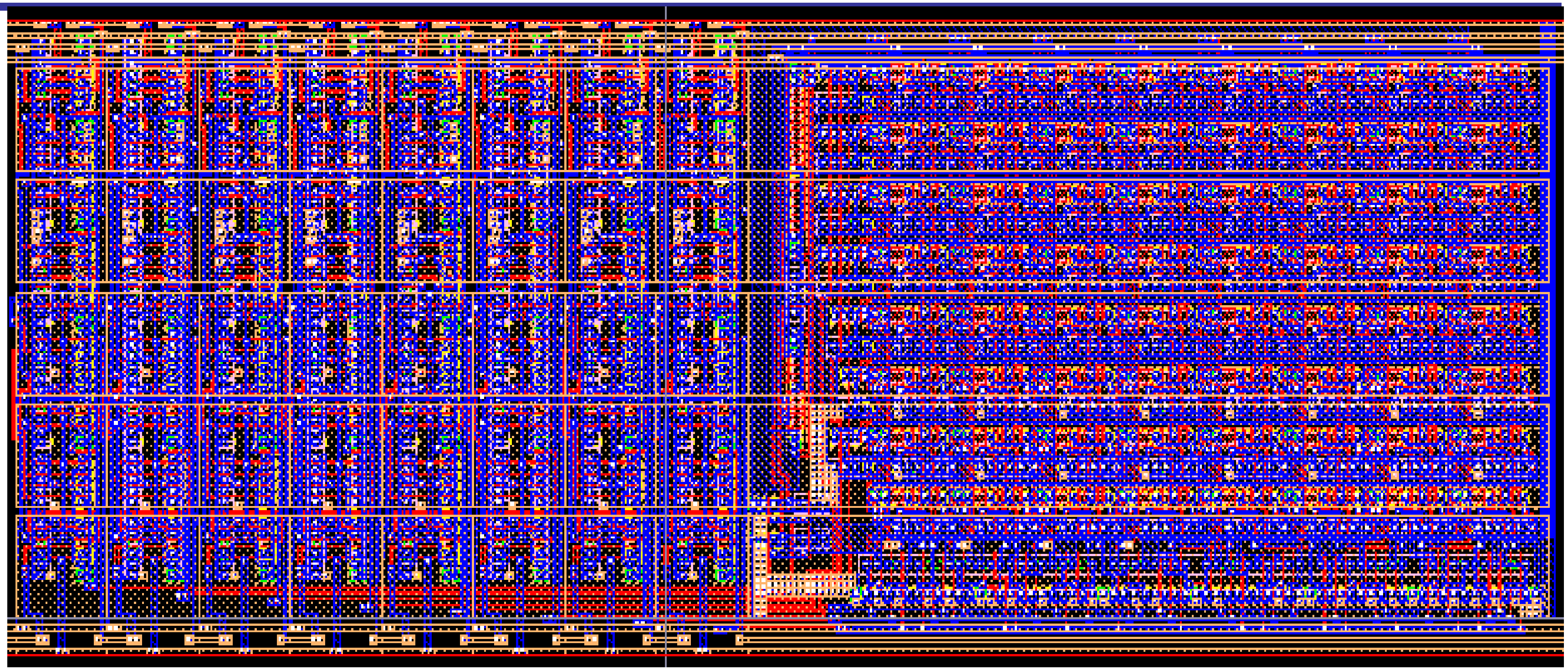
0.25µm:
63 devices, 16x50 µm2
< 1 day work

DMILL:
59 devices, 90x50 µm2
> 1 week work

We got a x 6 gain the density (full custom digital) with much less layout effort

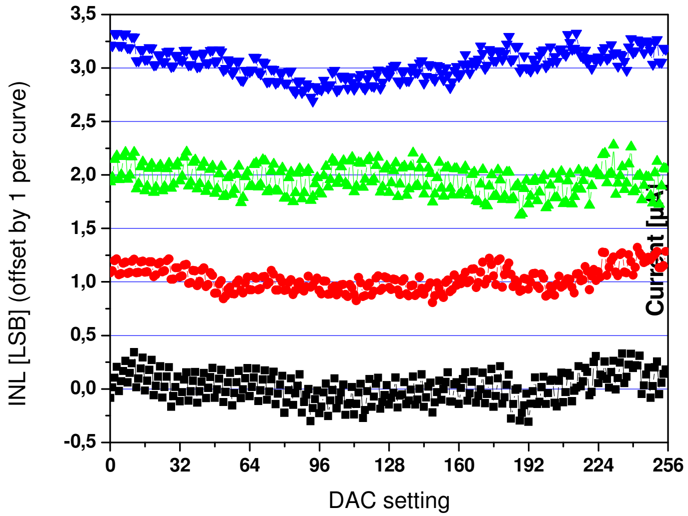
Example: 8 bit DAC 0.8µm ⇔ annular 0.25µm

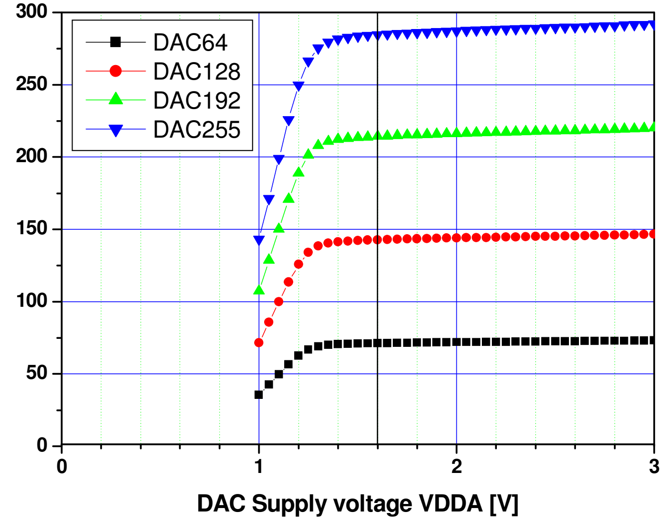




0.25µm 80x200 µm2	DMILL 500x200 µm2

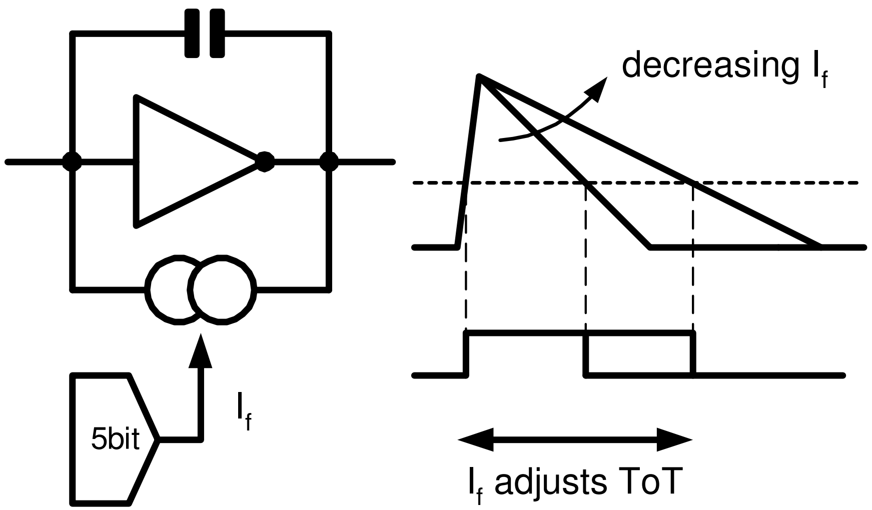
gain x 6 in mixed mode
full custom layout





ATLAS chip in 0.25µm technology

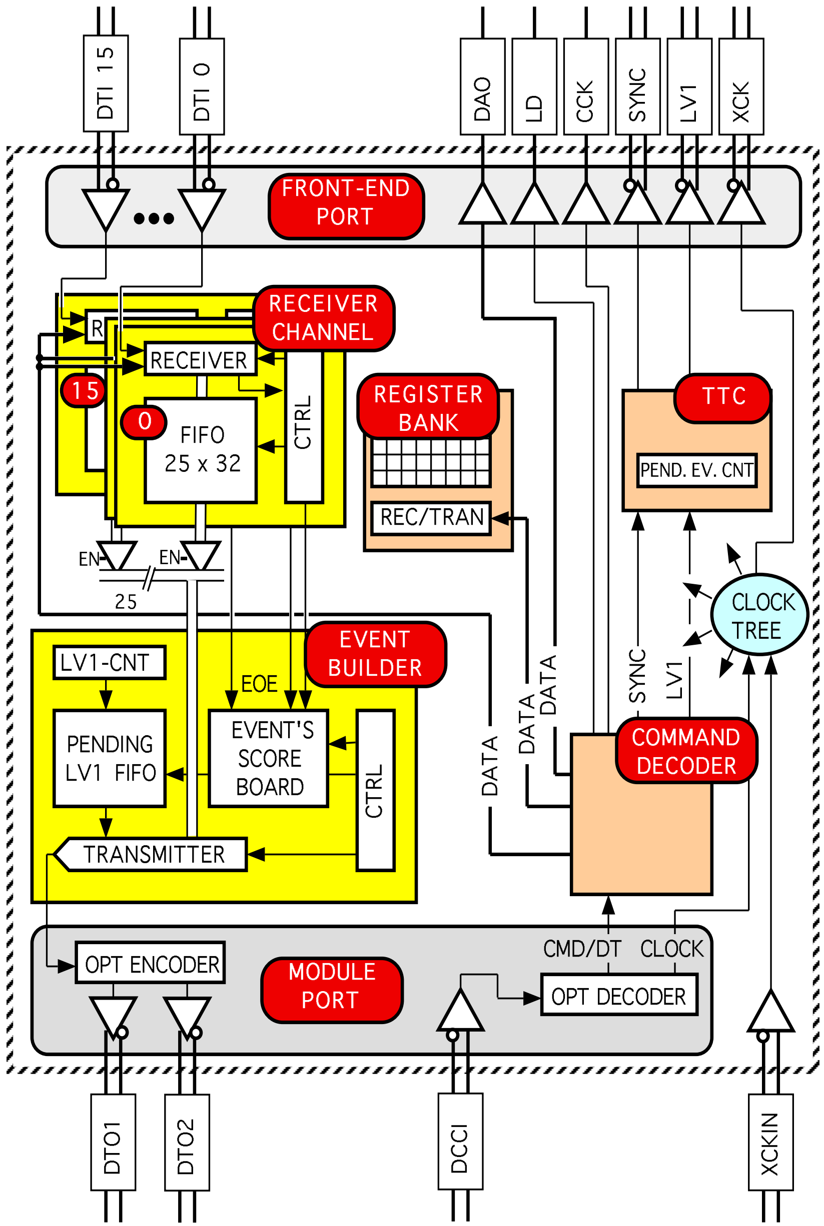
- We have converted our FED design to 0.25µm technology
- Benefit from high integration density and 5 metal layers.
- Examples:
  - Reduce cross coupling between digital ⇔ analog (also through sensor)
  - Add EoC buffers (now 64)
  - Threshold trim increased to 5 bit (!) on 25x25µm²
  - On-chip decoupling added, on-chip voltage regulators, ...
  - ToT trim added
  - Time walk correction: correct leading edge value if measured ToT is small



The MCC: Event building & Control

Tasks of module control chip MCC:

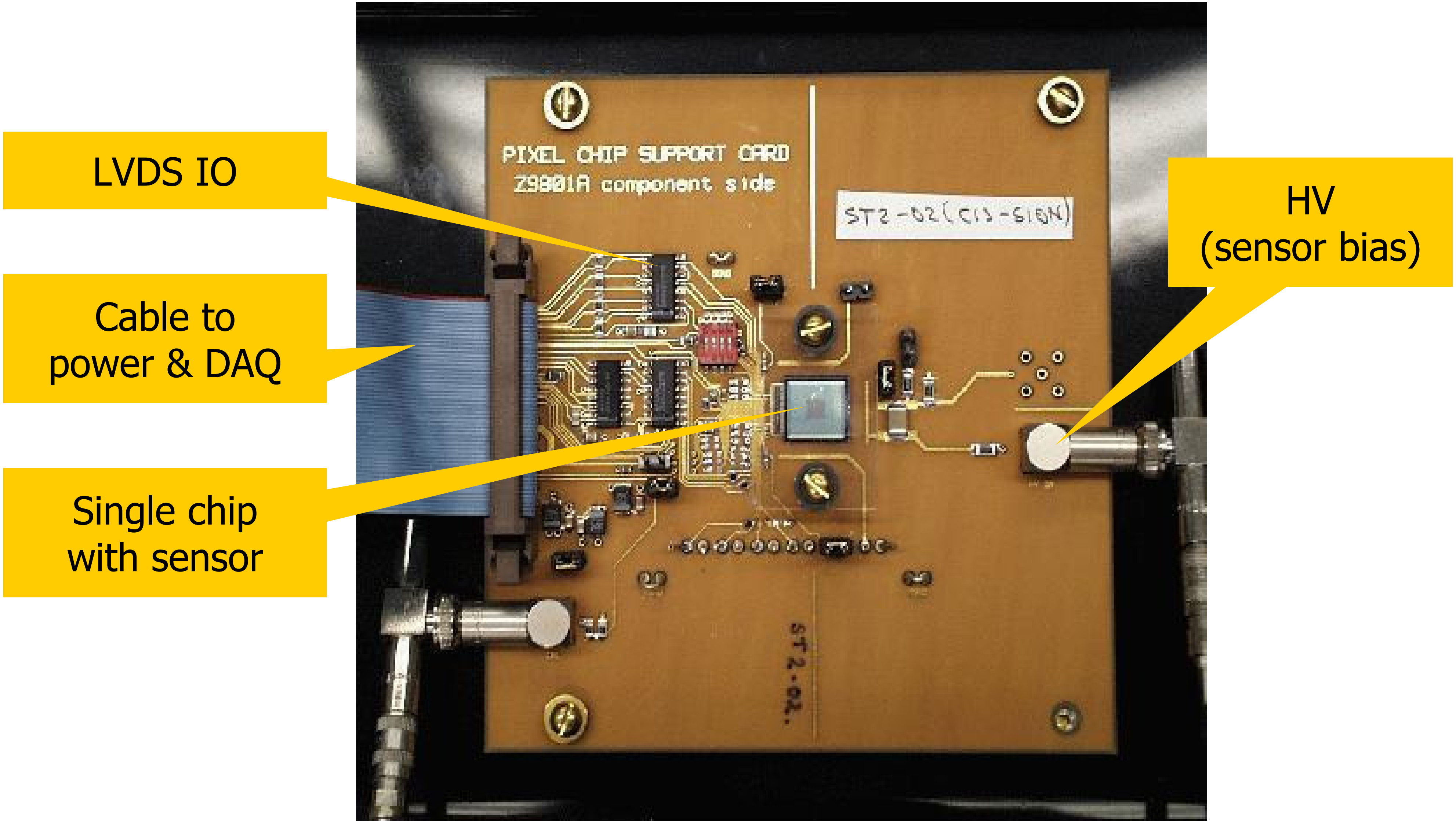
- Decode data/command signal (from DORIC)
  - ⇒ configuration data
  - ⇒ ‚slow' commands
  - ⇒ ‚fast' commands (trigger, SYNC, ...)
- Generate control signals for FE chips
- Receive serial data from 16 FE chips, accumulate data in FIFOs
- Check consistency of event (‚score board')
- Build complete module event
- Send event to DAQ (via VDC)
- Error handling, fault conditions (disable defective FE chips, ...)



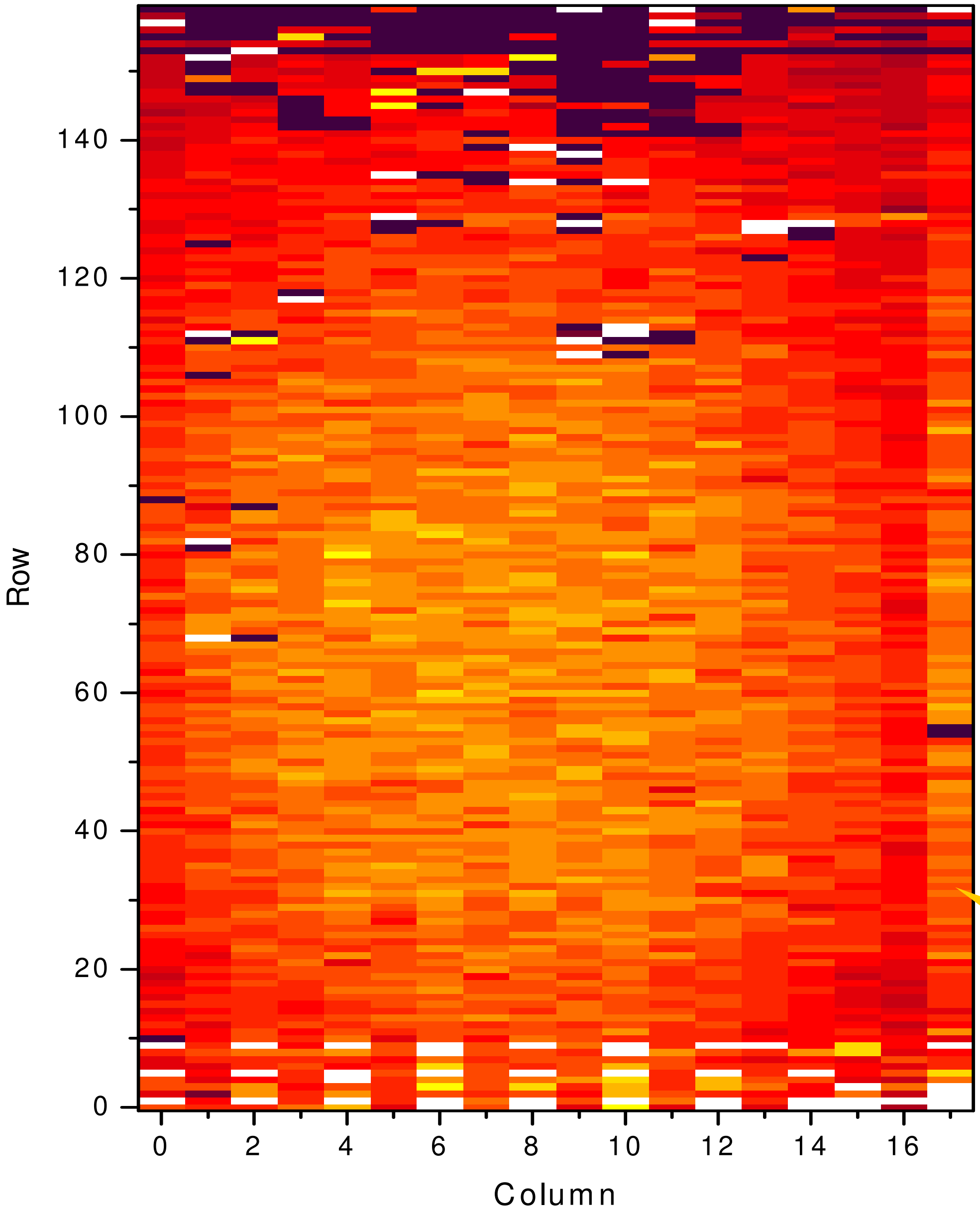
Silicon Pixel Detectors – Today and Tomorrow

- Why pixels?
  - Requirements and challenges
- The ATLAS pixel detector
  - Modules, mechanics etc.
  - The sensor
  - The front end electronics
  - Some results / status
- The next generation (for TESLA)
- Other applications of hybrid pixel detectors

Results of single chip & module prototypes



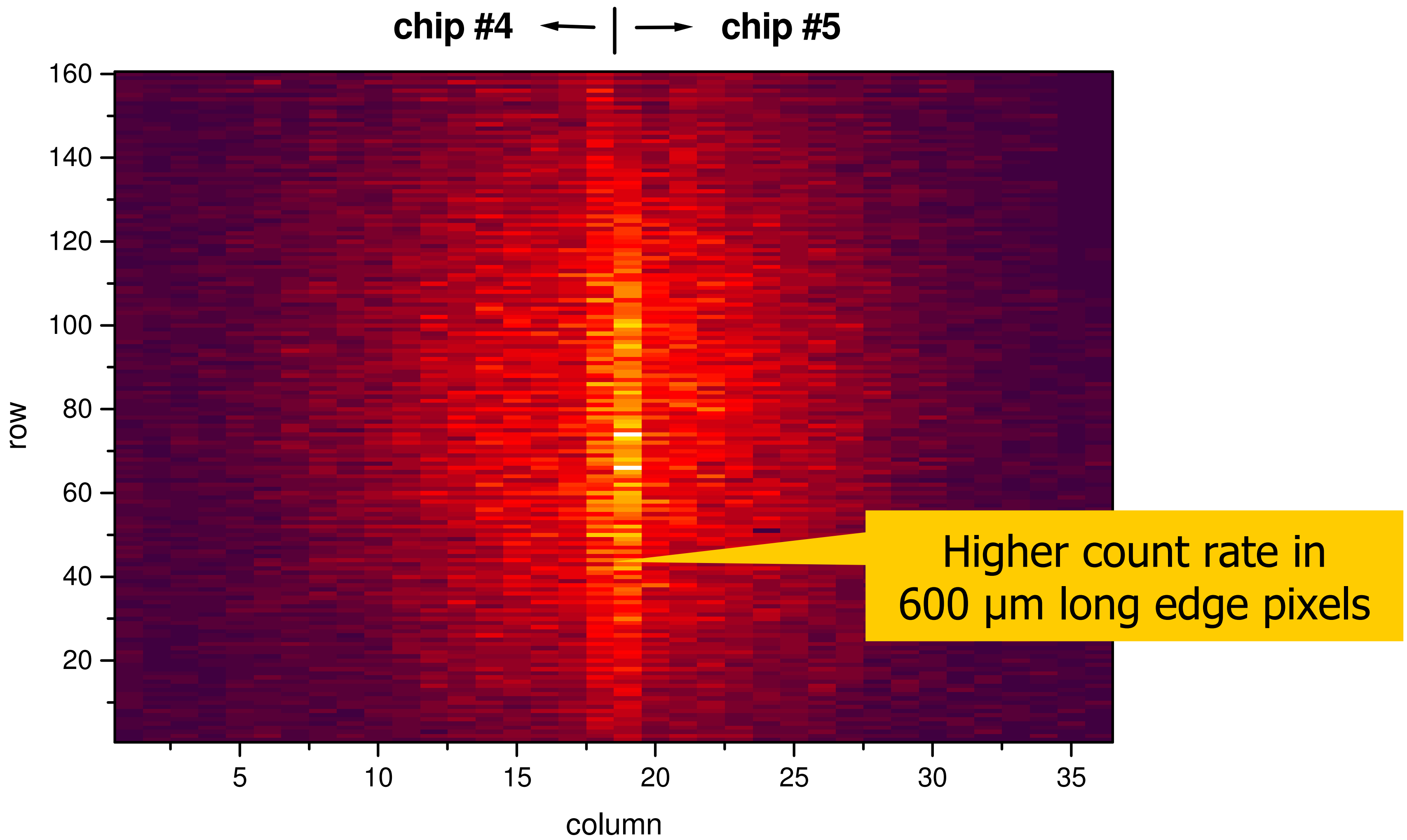
Source measurement with ^{55}Fe



- ^{55}Fe-source (6keV γ) deposits
  only 1700 eh-pairs
- FE-C chip with thresholds tuned to ~1200e$^-$
- Some bump problems at edge (one of the first assemblies)
- The chip can be operated at very low threshold

Edge sensors are longer (600 µm)
$\Rightarrow$ higher count rate

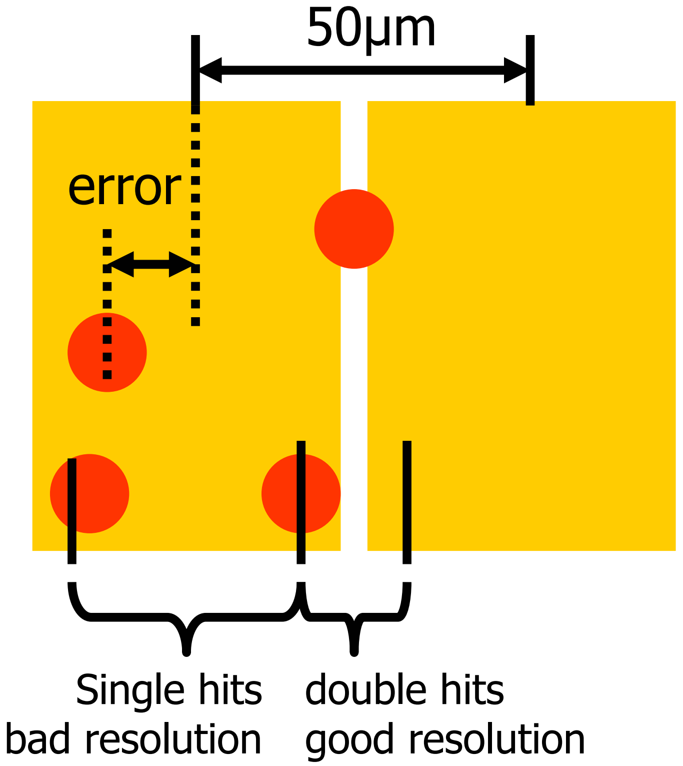
Source measurement on a module with ^{241}Am



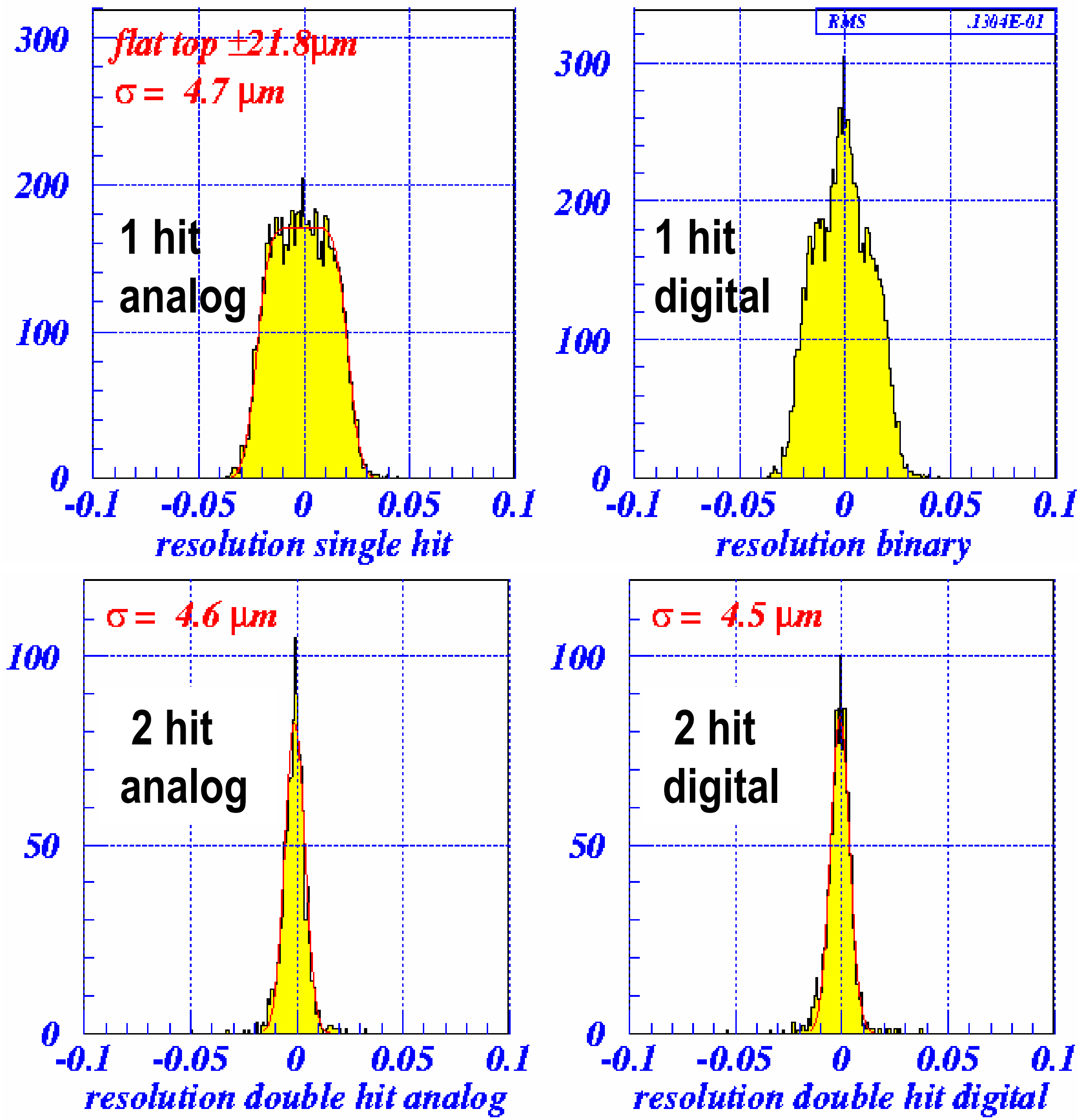
- Spot of ^{241}Am-source on two neighboring chips of a module
- Module without MCC: chips were illuminated one after the other

spatial resolution in testbeam

- Consider short pixel dimension:

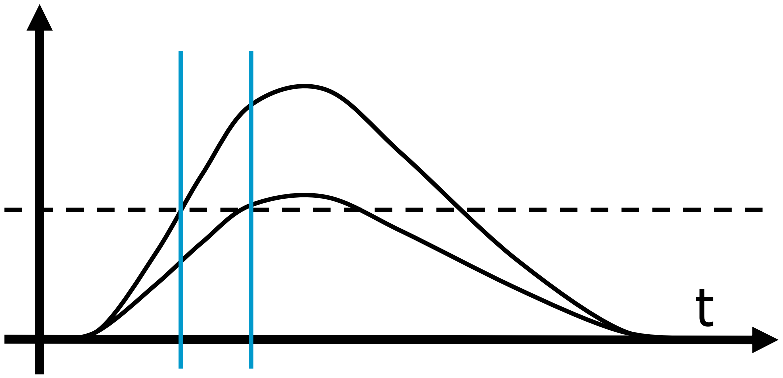


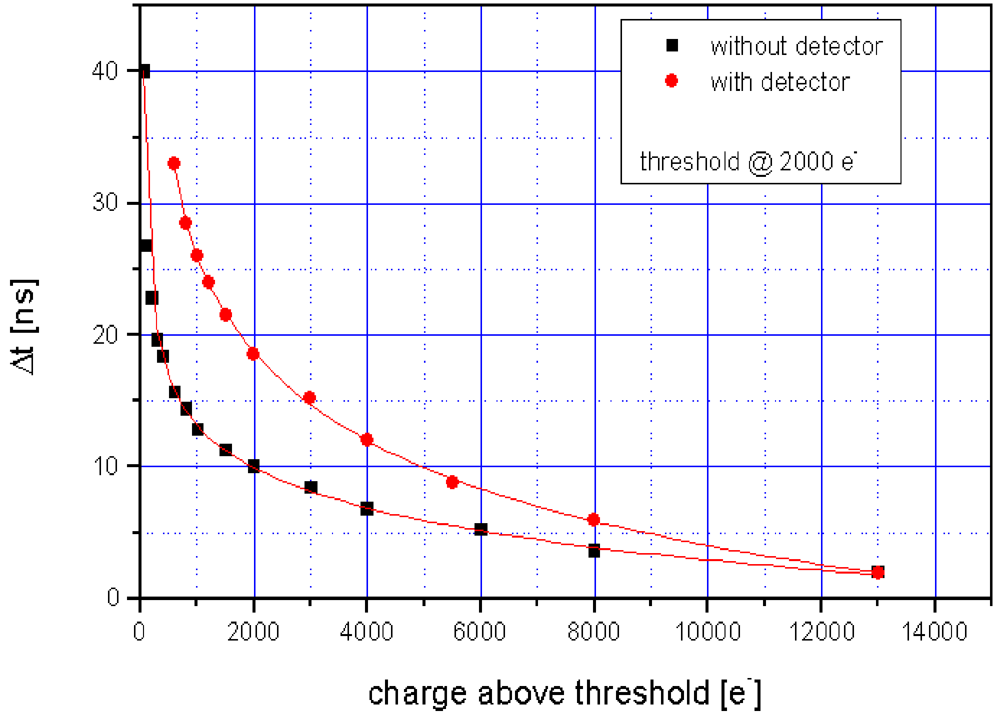
- σ_{1hit} = 22µm, σ_{2hit}=5µm
- σ_{all} = 13µm
- after irradiation: 14.5µm = 50µm/√12
- Less 2 hit clusters after irradiation
- No improvement with analog info



Time Walk

- Detector is a capacitive load
  $\Rightarrow$ preamplifier has slow rise time (limited by power!)
  $\Rightarrow$ hits only slightly above threshold fire discriminator later
  $\Rightarrow$ hit is lost if delay > 25ns

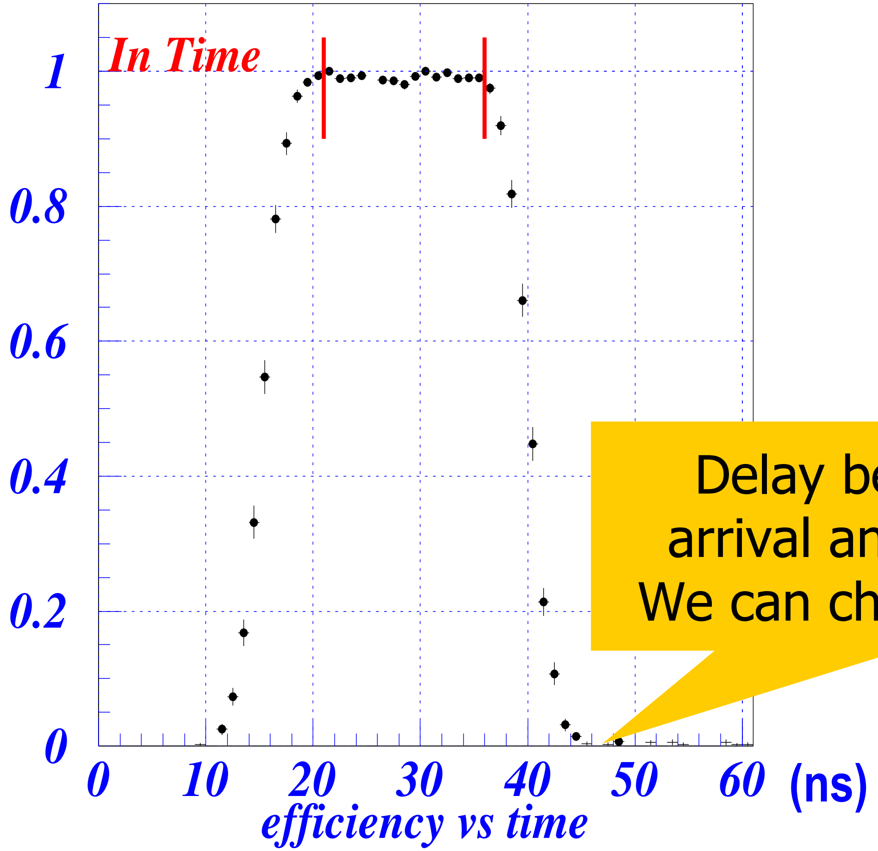




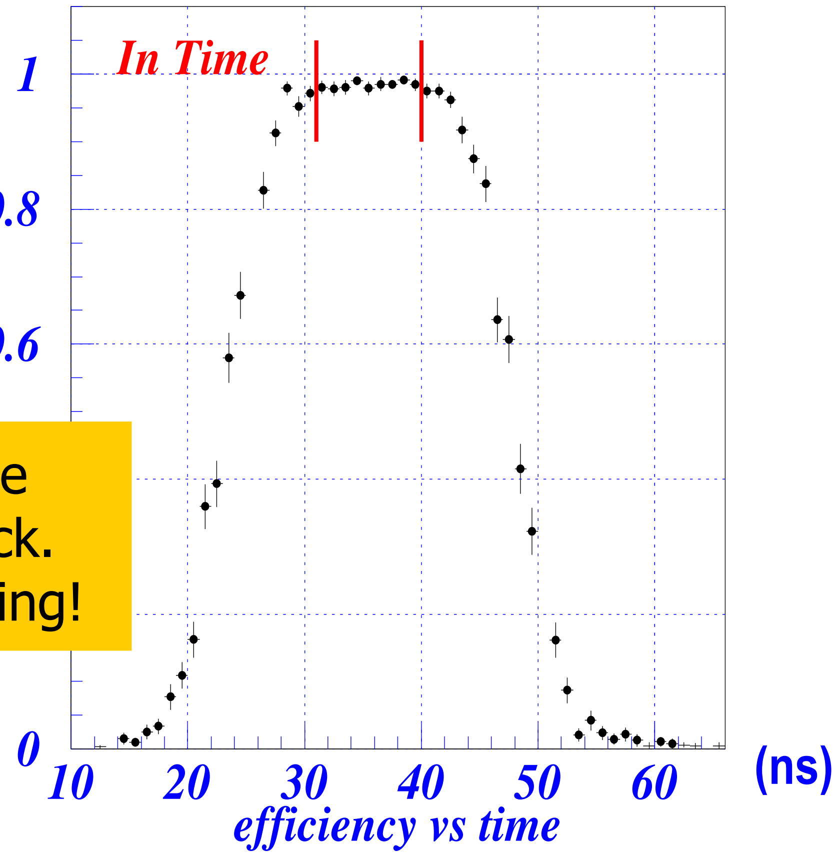
- This is one of our biggest problems.
  Possible improvements: zero crossing, digital correction (FEI)

Track Efficiency

- Despite marginal time walk, efficiency is ok after irradiation !
- Here: Sensor is moderate p-spray with bias grid. Chip threshold is 3000 e^-



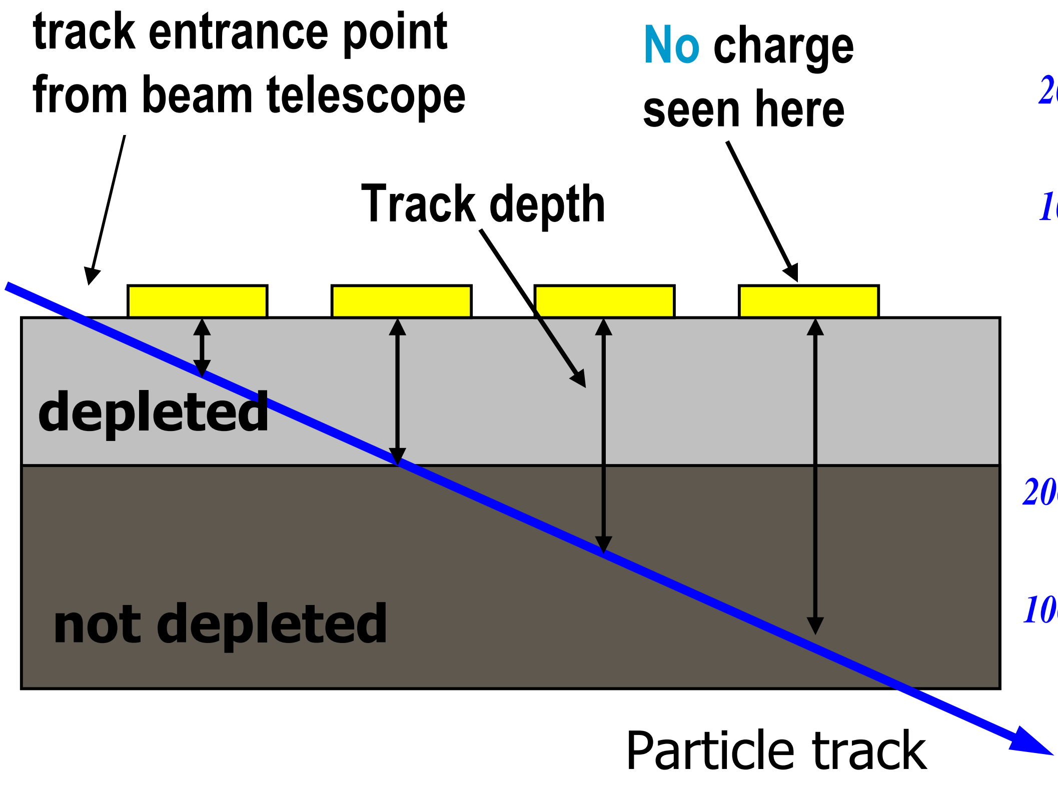
Delay between particle arrival and 40 MHz clock. We can choose best timing!

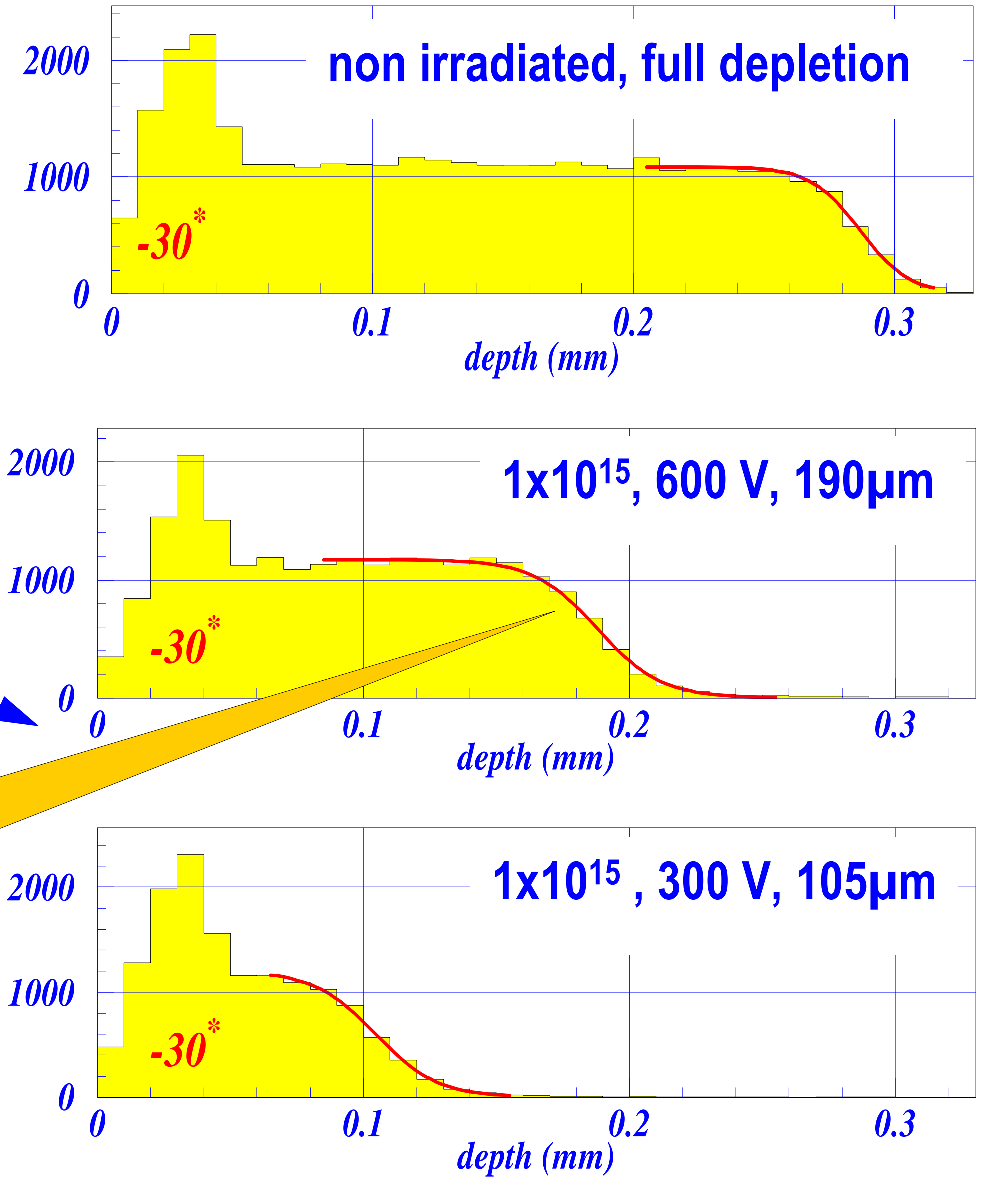


Non-irradiated
efficiency = 99.1%

Irradiated (10^{15} $n_{eq}cm^{-2}$)
efficiency = 98.4%

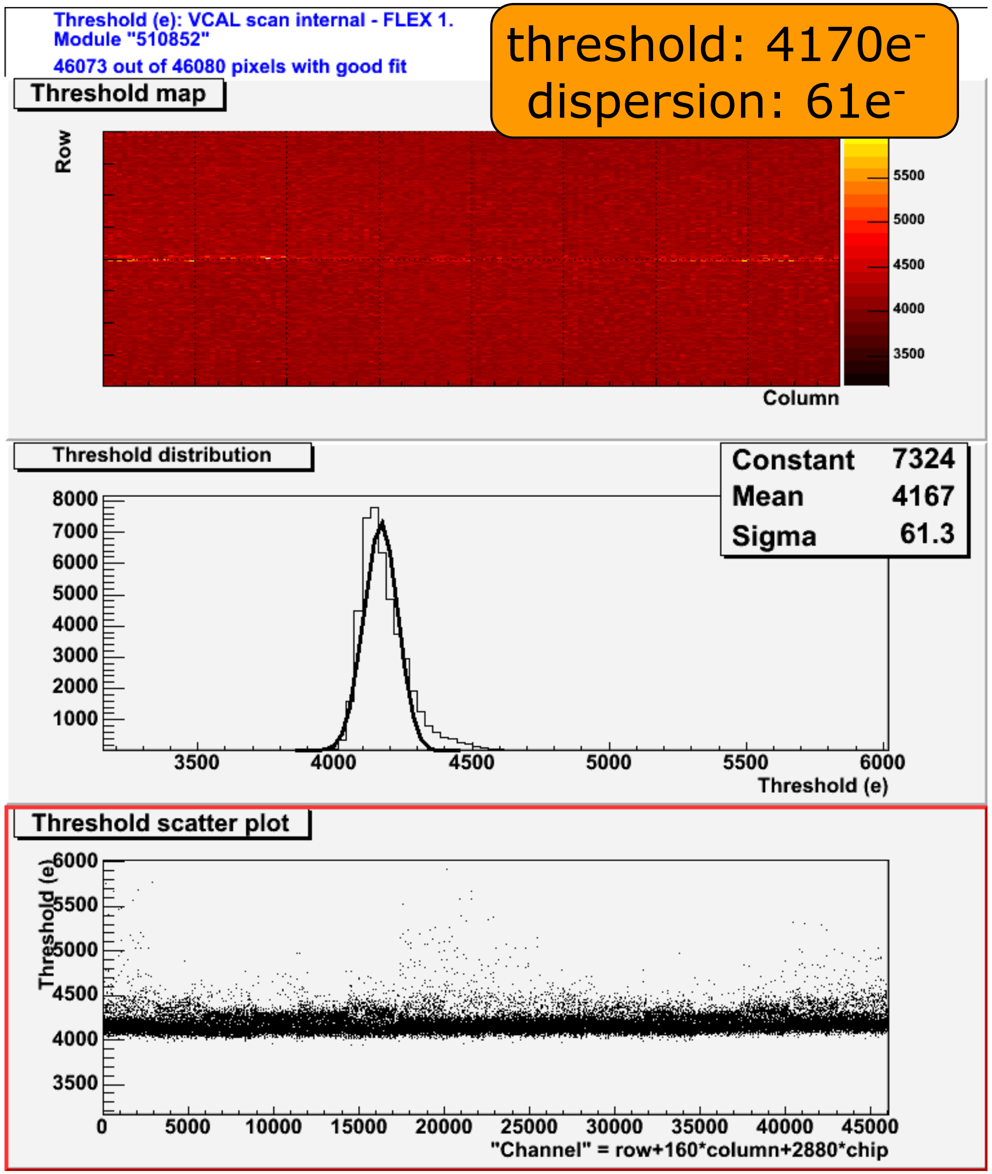
Depletion Depth after irradiation

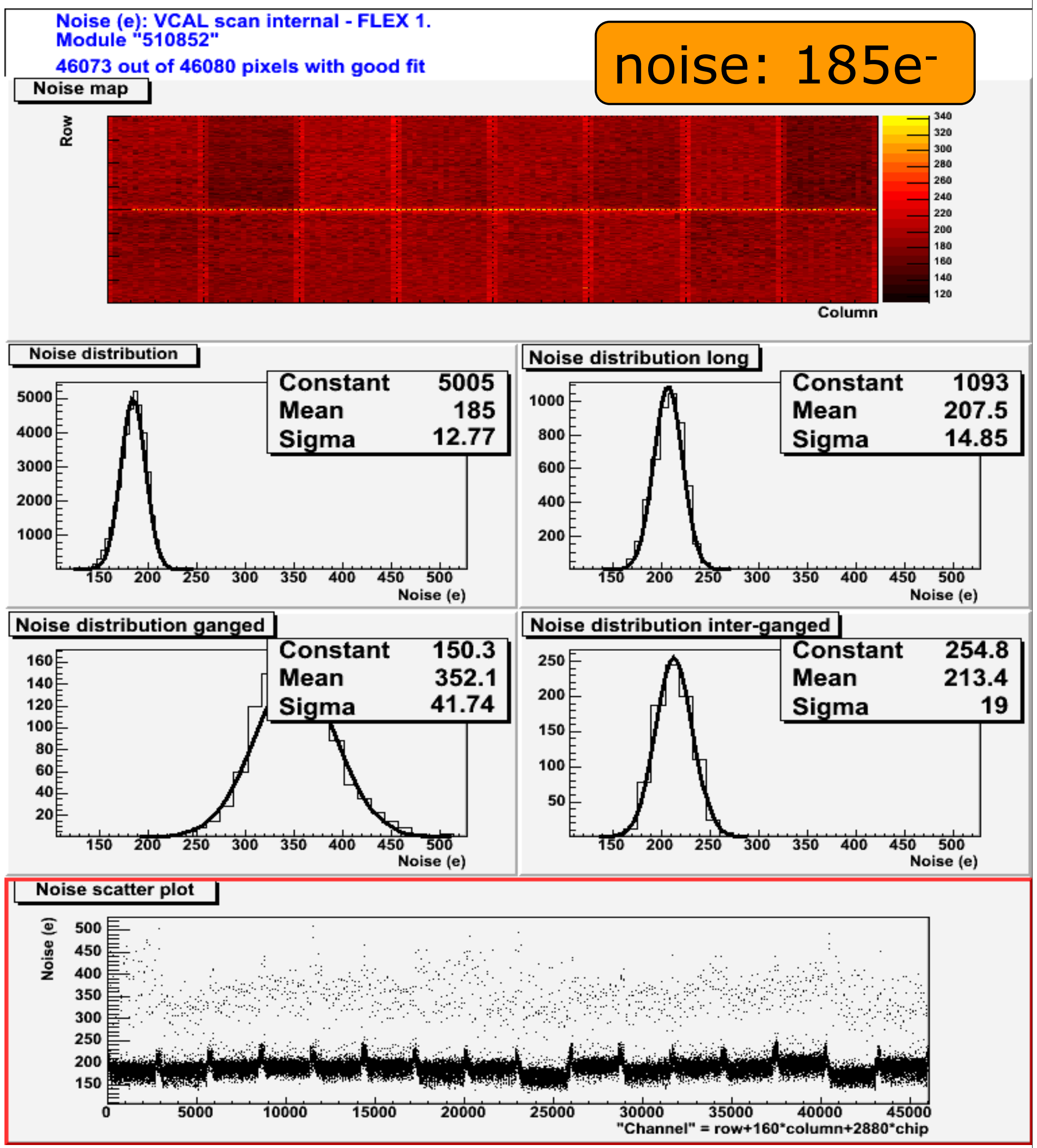




Depletion depth is 190 µm @ 600 V after 10^{15} cm^{-2} (full ATLAS dose!)

Module Lab Measurement





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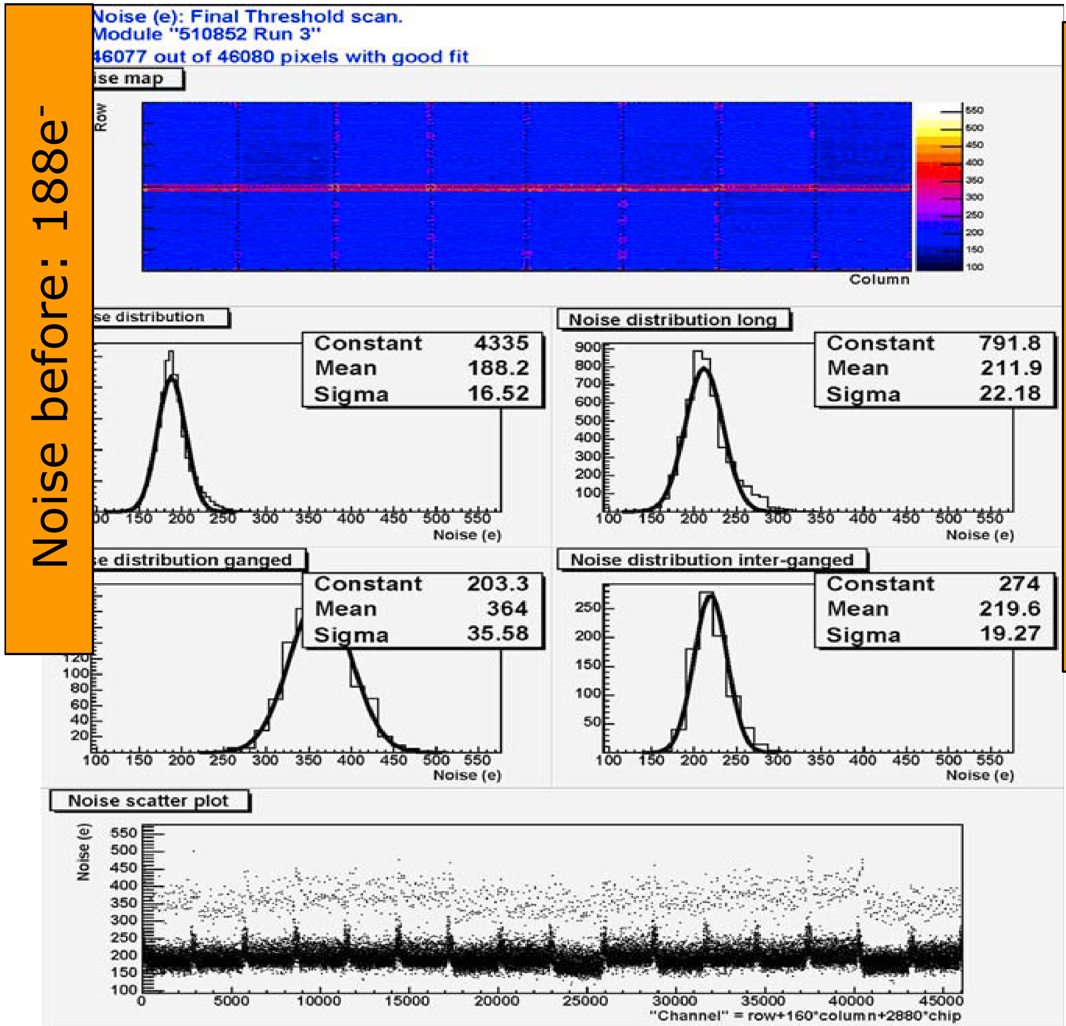
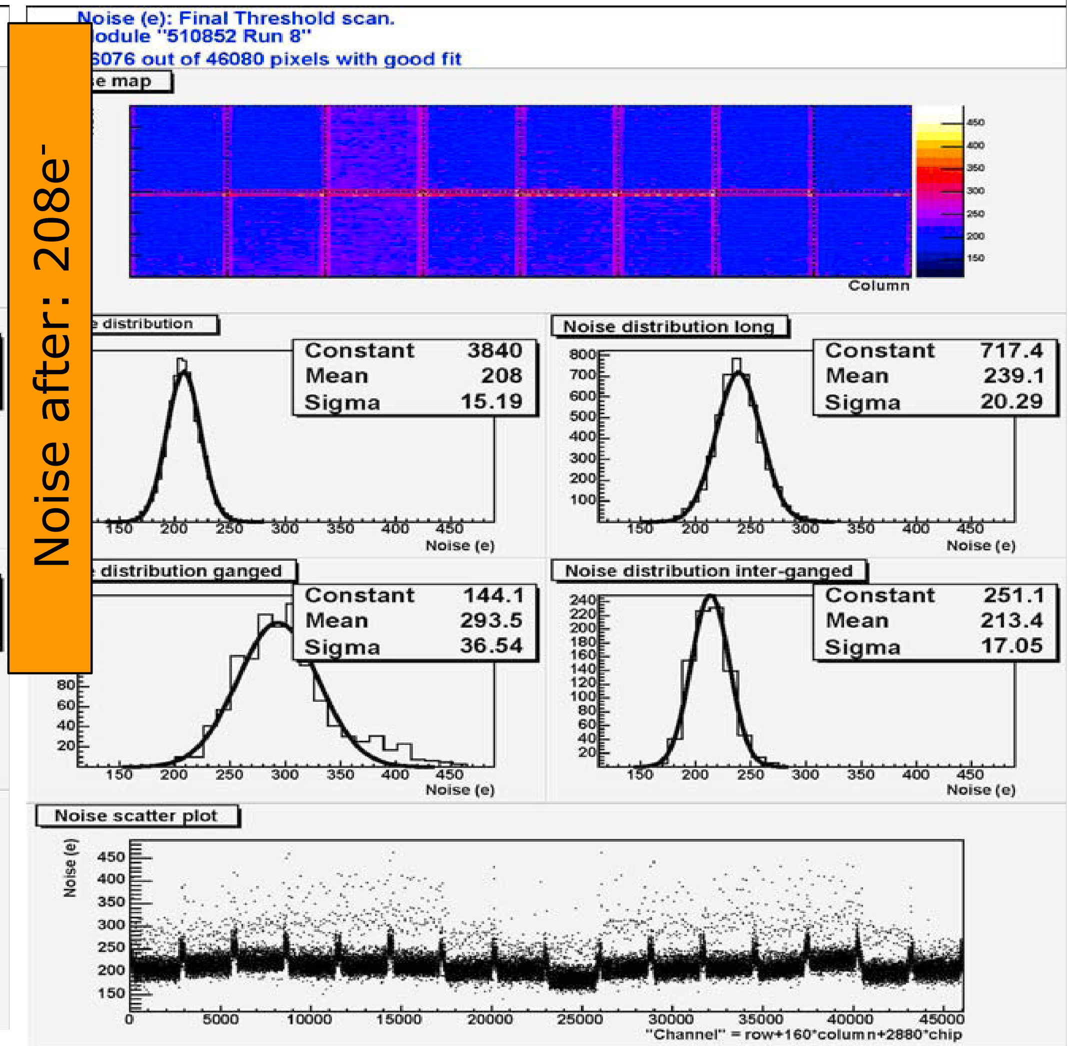
Tests after Module Irradiation

Extensive radiation studies at CERN PS, irradiation of 7 production modules to ATLAS lifetime dose (2×10^{15} p/cm^2 ≈ 50MRad).





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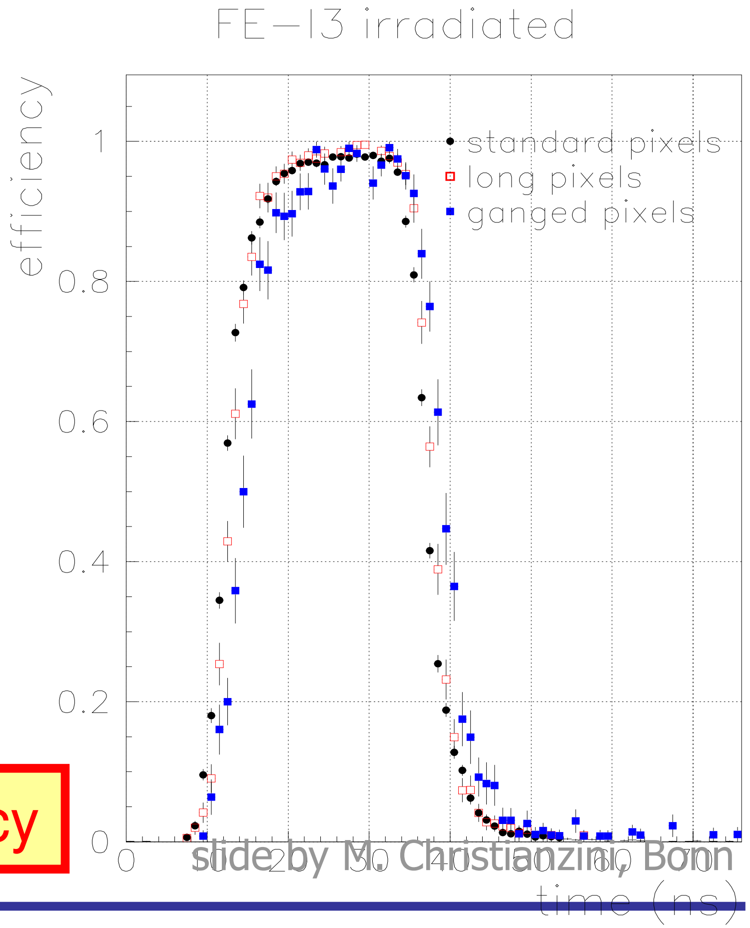
Test Beam Results (Irradiated Module)

- Test beam 2004 to characterize production modules
- Radiation hardness
  - Sensors almost fully depleted after 3 yrs high lumi with 600V bias
  - Charge collection efficiency reduced to 80% (trapping)
  - Lorentz angle decreases with increasing bias voltage (15°→5°)

- Detector performance after irradiation
  - In rφ direction 7µm (no irradiation) to 10 µm (after irradiation)
  - Efficiency: 99.9% → 98.2% after irradiation (@ 500V)
  - Pixel geometry slightly affects efficiency
  - High rate tests passed

In-time efficiency



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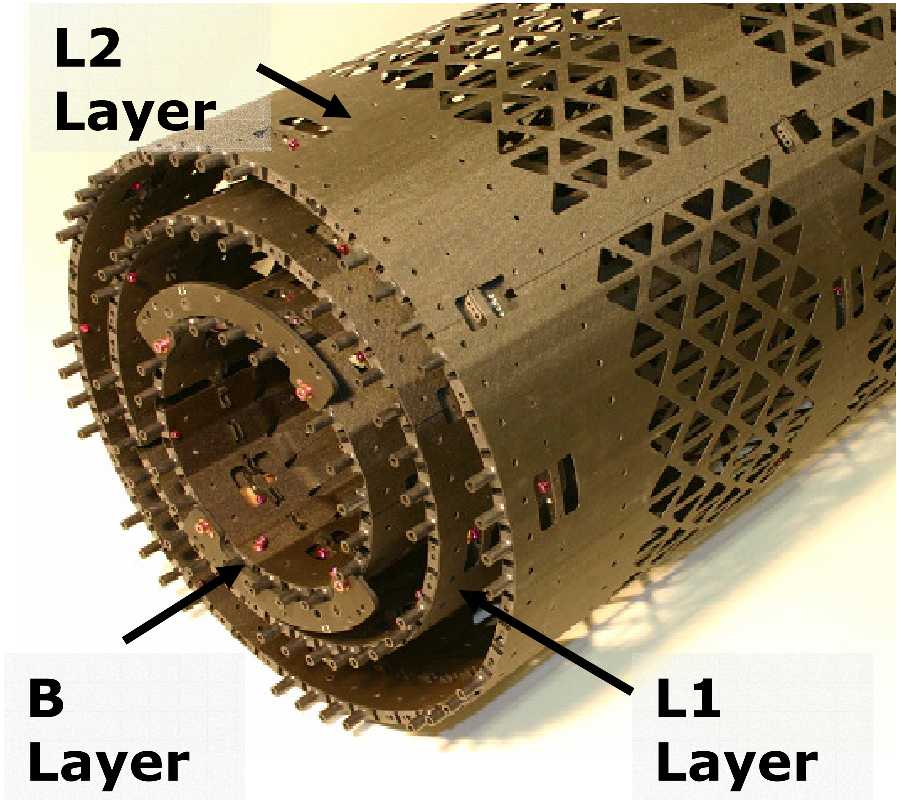
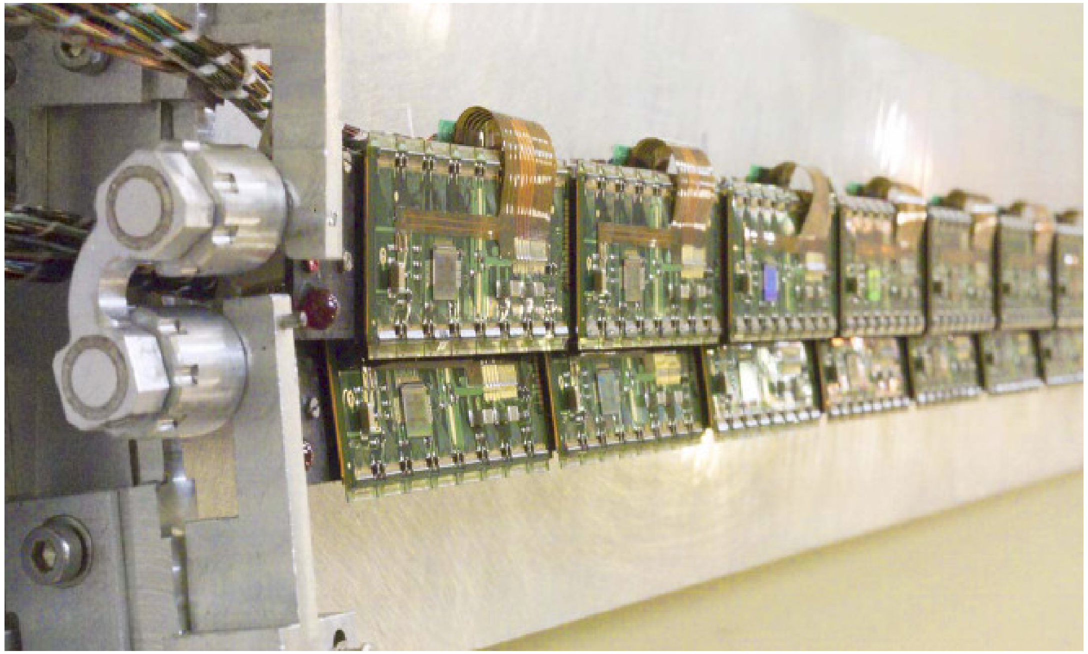
Assembly of the Pixel Barrel

- Barrel composed of
  - barrel frame (carbon fiber laminate)
  - staves
    - 13 modules
    - Shingled carbon-carbon support
    - All identical (except cabling)





- For integration two staves are linked by a unique cooling tube (bi-stave)

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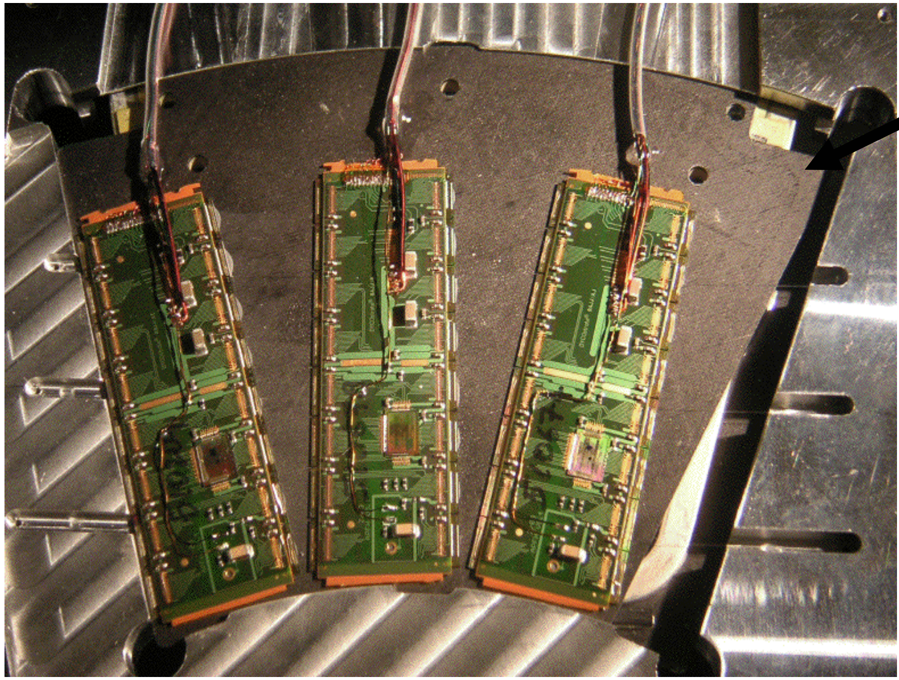
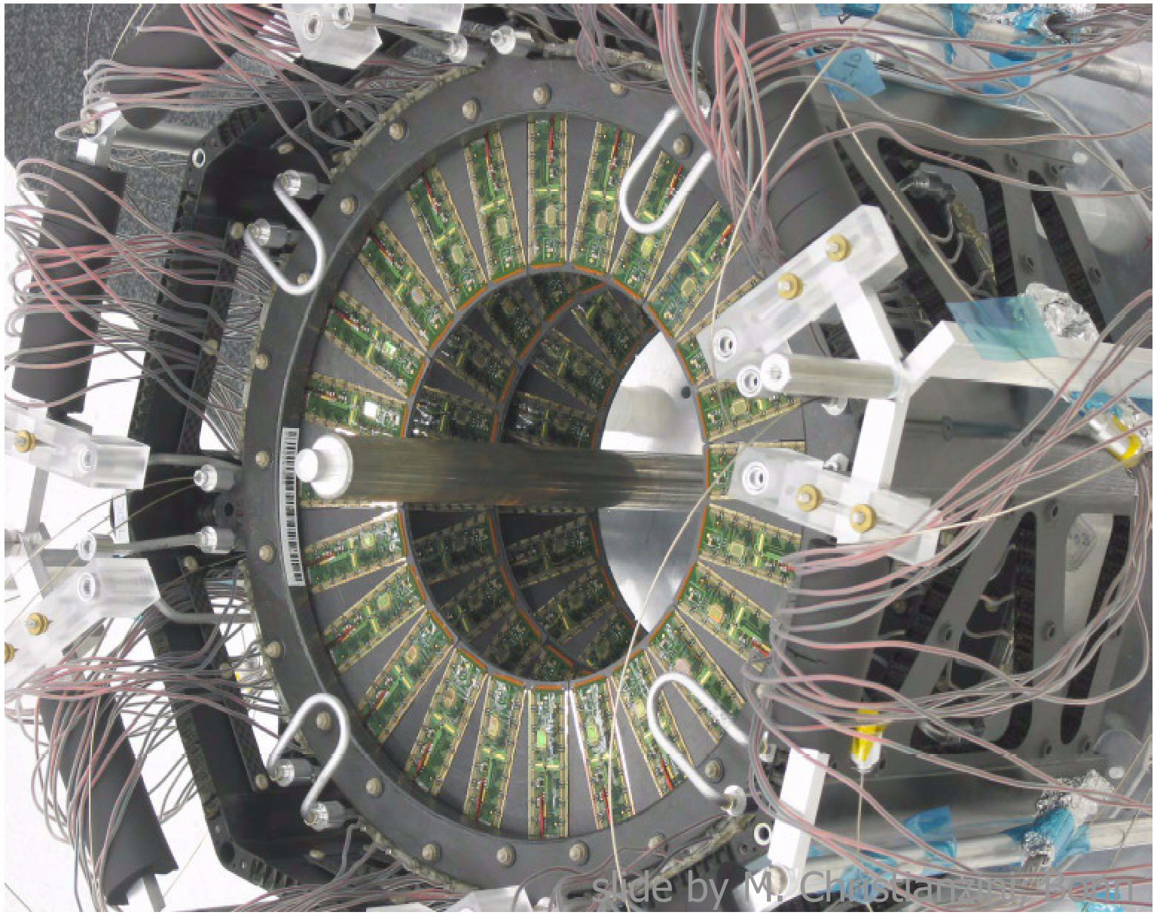
Pixel End Cap



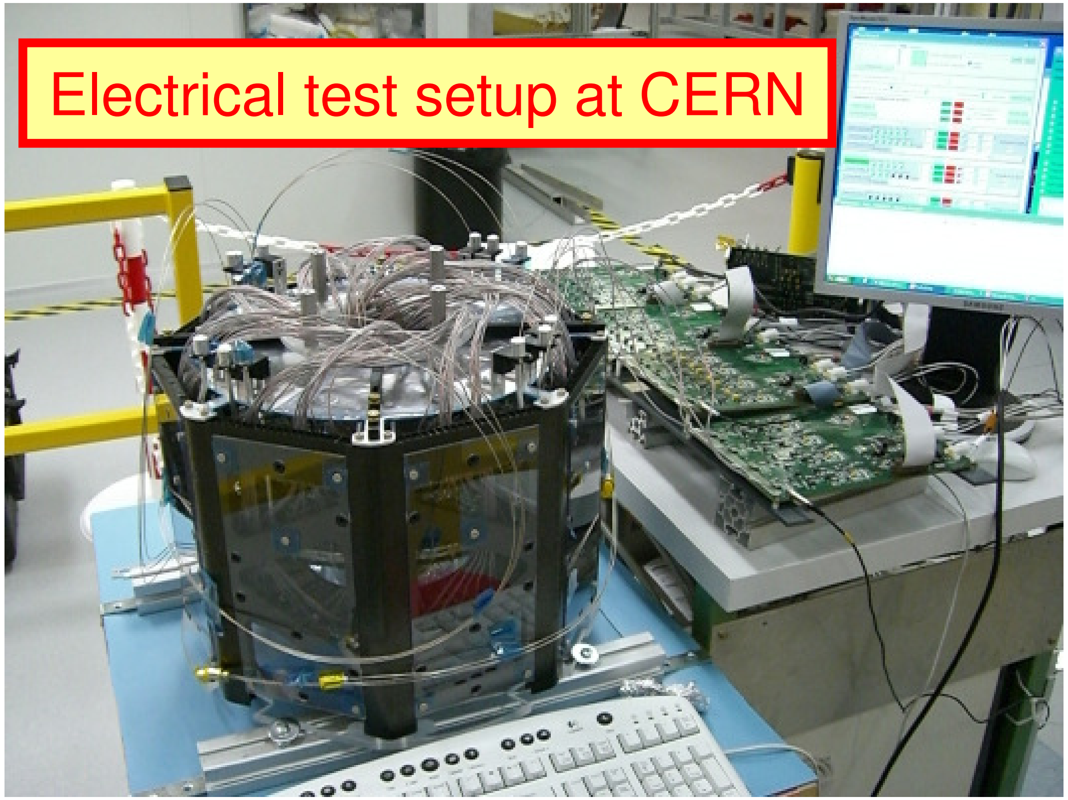
Sector assembly (1/8 of a disk):
6 modules are mounted on
carbon-carbon plates,
sandwiching the cooling pipe.

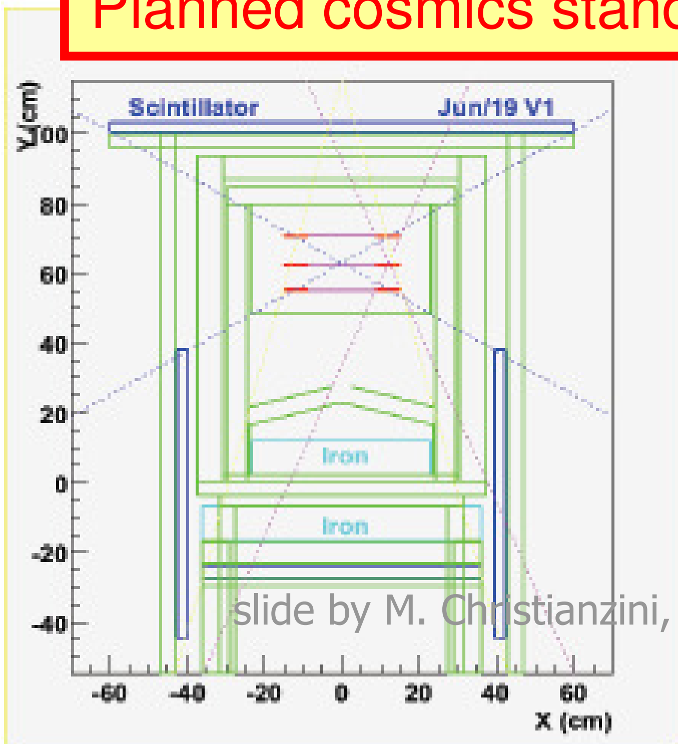


Assembled at LBL
and shipped to CERN
for integration

End cap status

- Both Pixel End Caps are not at CERN
  - Were fully assembled in LBL
  - dead channels at few per mil level
- Preparing for cosmic tests in November
  - test DAQ chain, services and software





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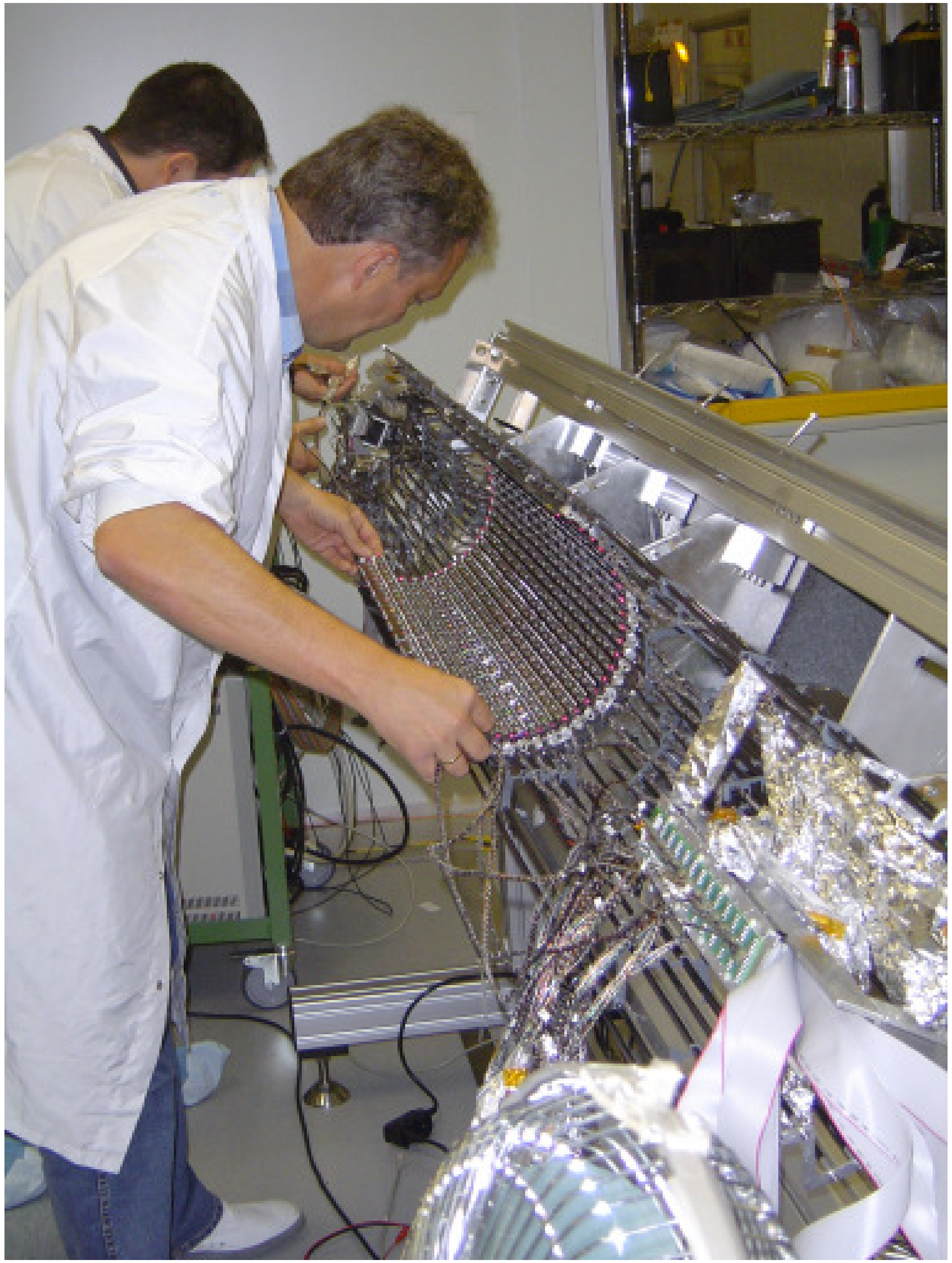
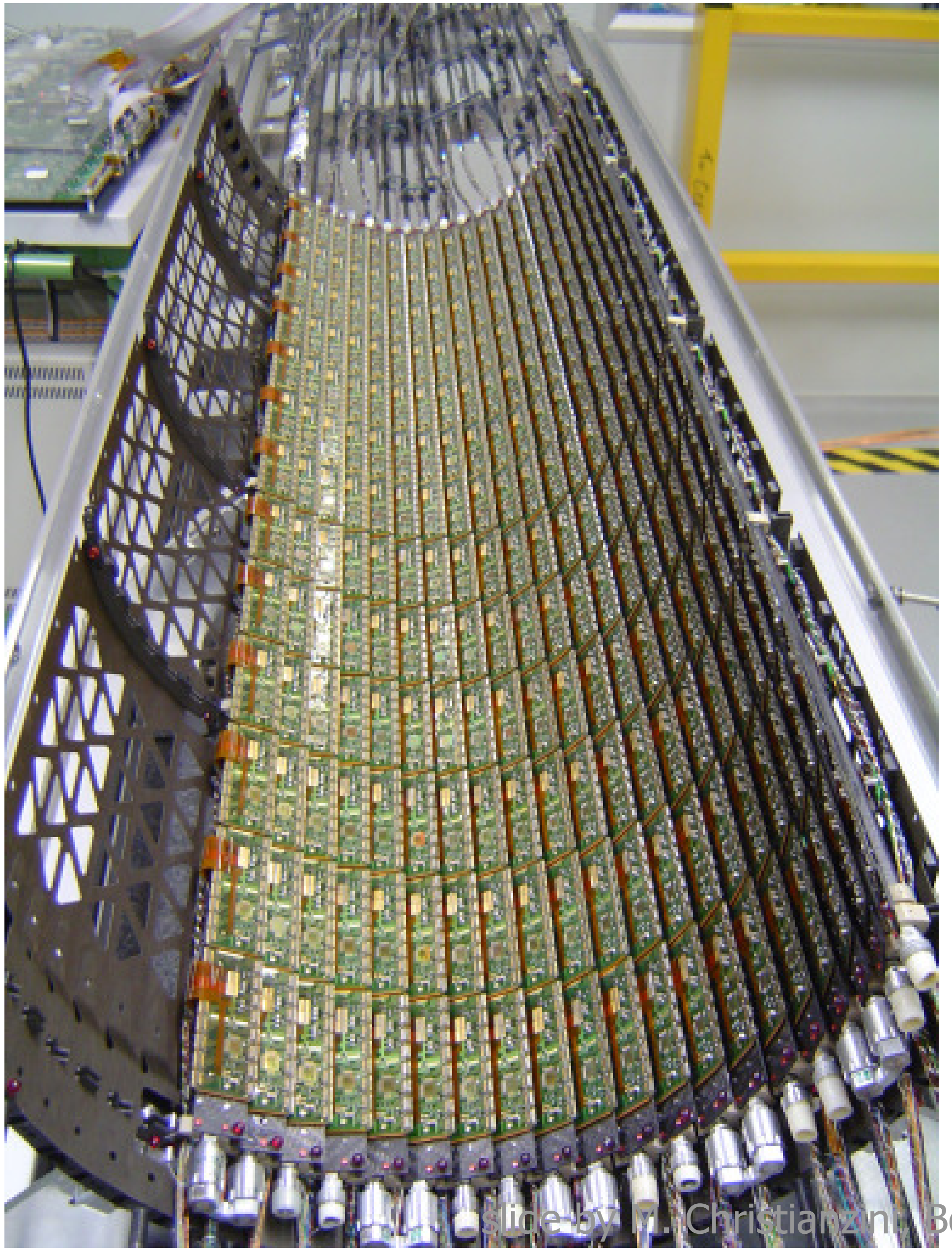
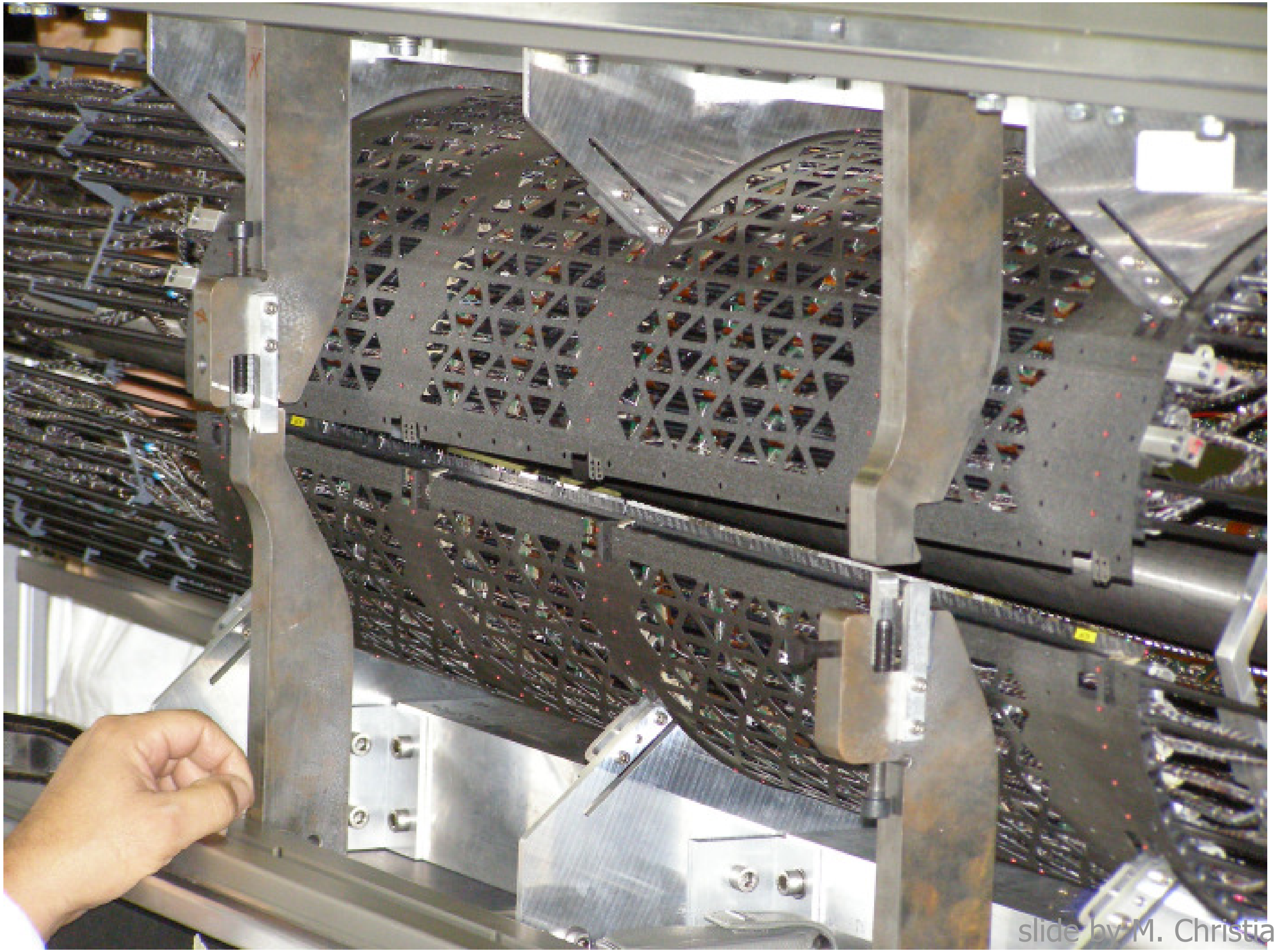
Barrel integration: Mounting Staves into Half-Shells





Barrel integration: Putting together Halve-Shells



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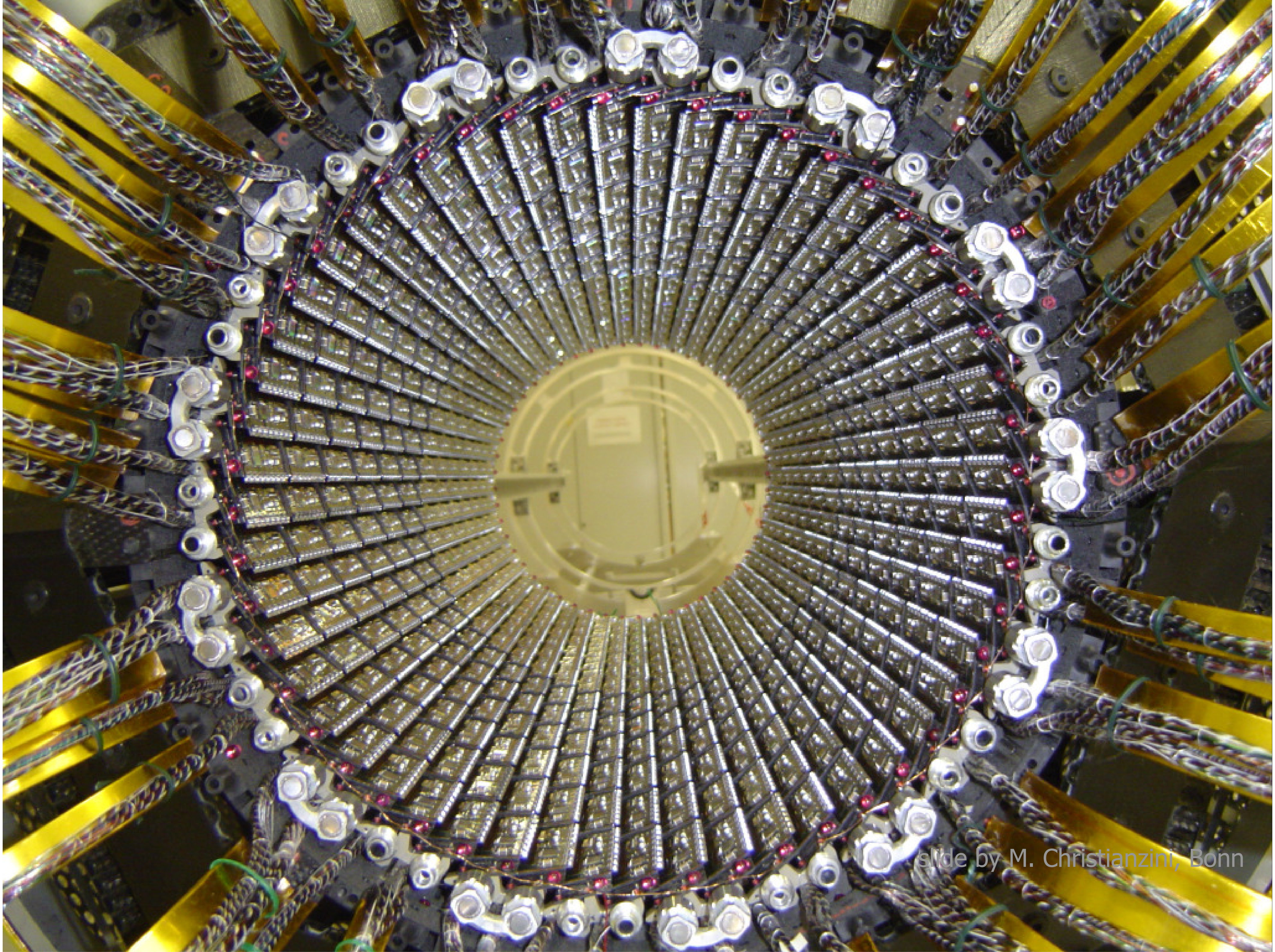
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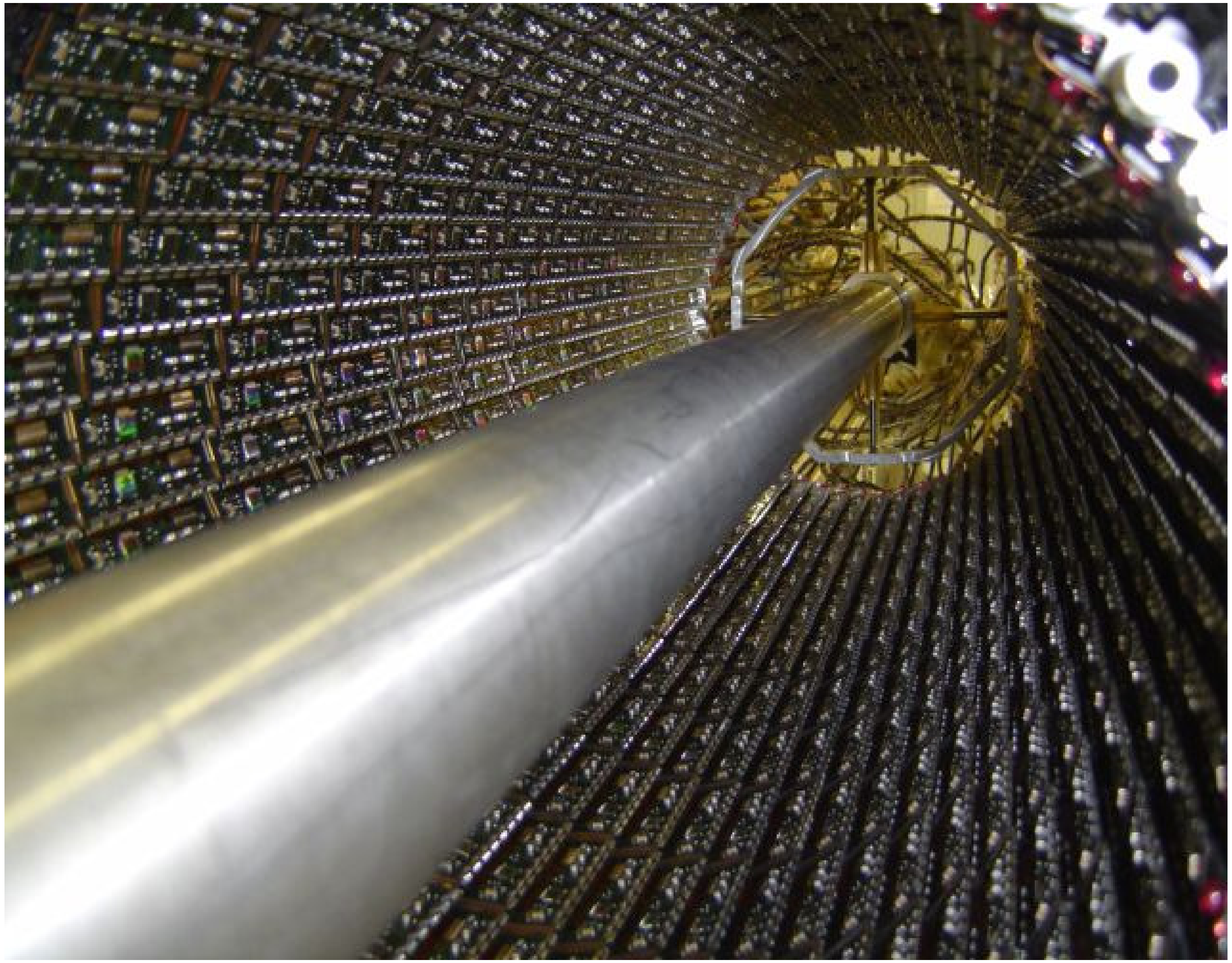
ATLAS Status

- After ~10years R&D the ATLAS pixel detector is nearly completed
- Test beam results and an extensive QC program makes us confident that the system will perform within specs



- A number of problems were tackled in a collaboration wide effort and solutions appear adequate
- Pixel will be integrated into ATLAS April 2007

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