


# Silicon Strip Detector + Beetle Readout Chip

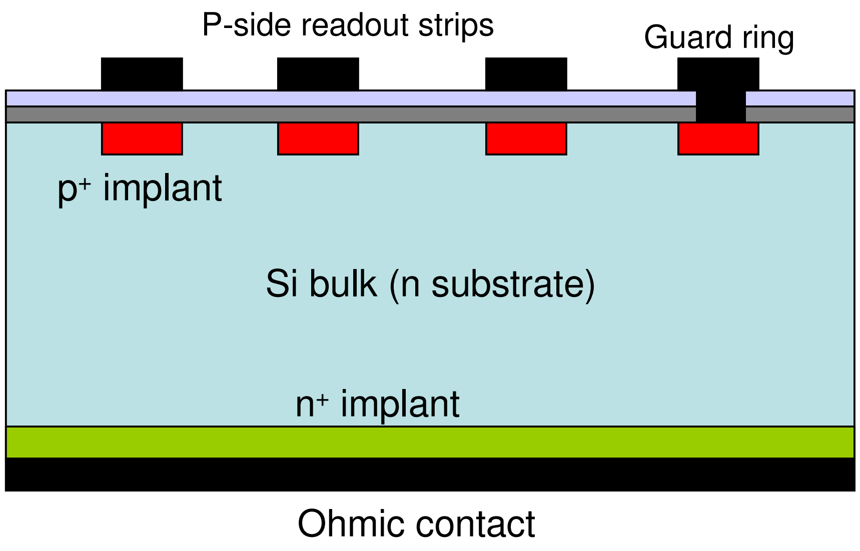
T. Alt, G. Øvrebekk, F. Rühr,
K. Aamoth

# Overview

- Introduction
- Setup
- Measurements
- Conclusion

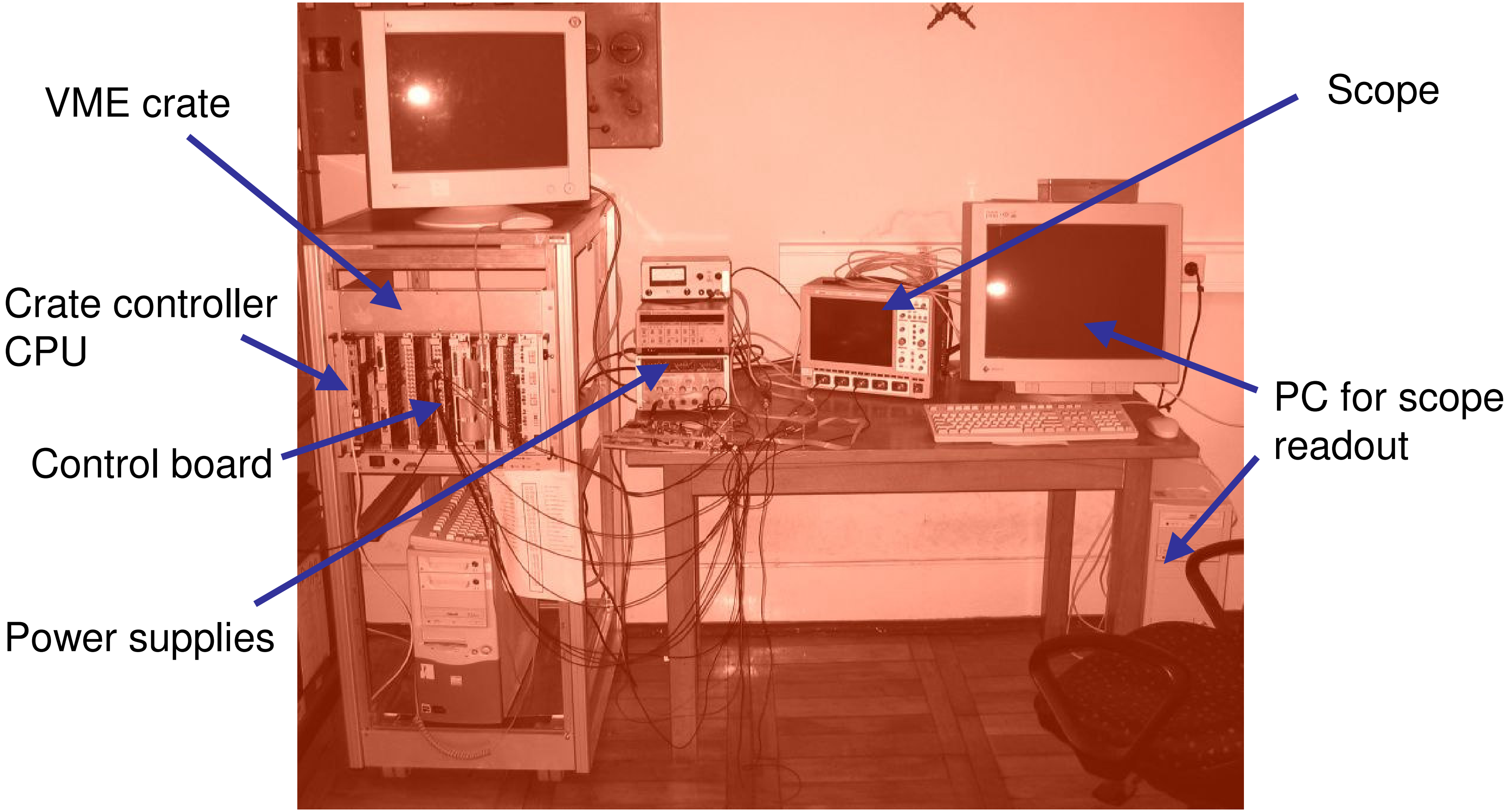
# Silicon strip detector

- The task was to explore the properties of a silicon strip detector consisting of a silicon strip and an analogue front-end chip and use it for simple signal measurements



# The beetle chip

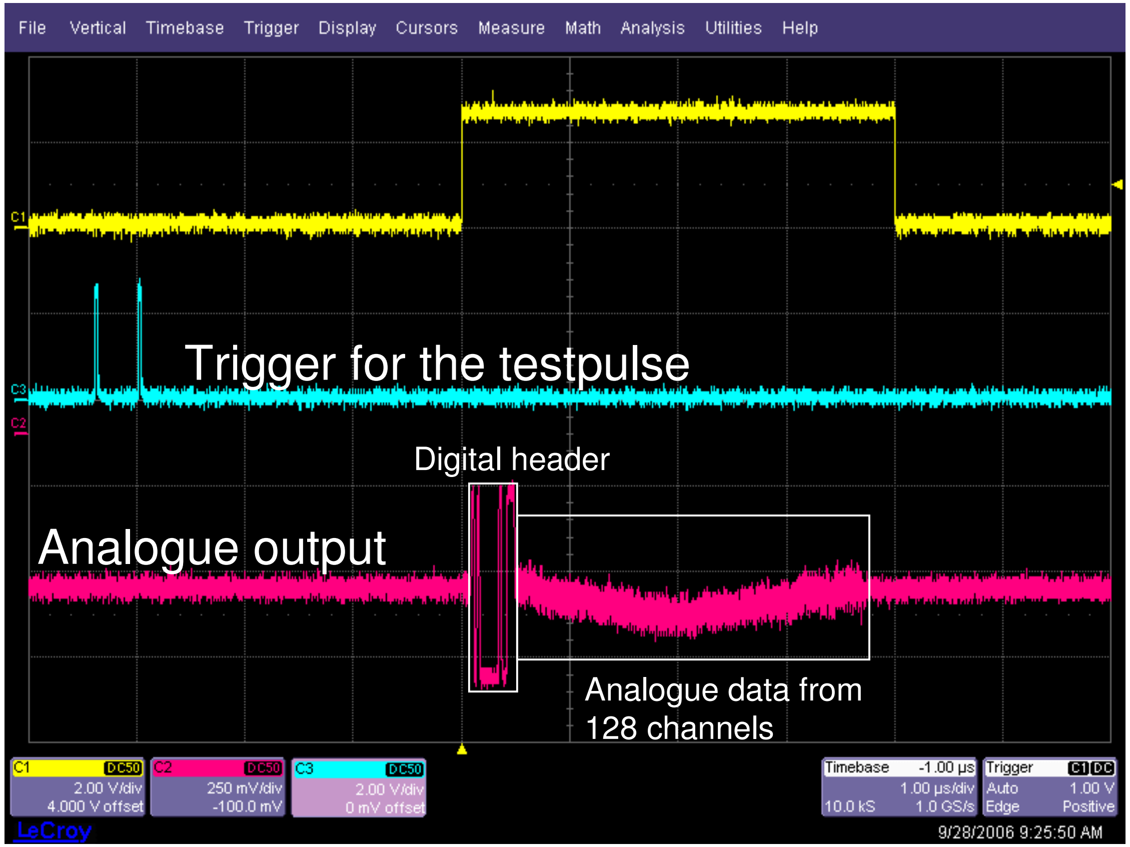
- The beetle is the front-end chip for our silicon strips
- It integrates 128 channels
- The input signals are amplified and shaped
- All 128 were multiplexed into one analogue output signal in our case(other modes exist)
- The chip provides an internal test pulse


VME crate
Crate controller CPU
Control board
Power supplies
Scope
PC for scope readout

# Detector and readout chip

- The assembly of silicon strips, testboard and readout chip were in an enclosed box to prevent damage to the silicon due to extreme currents caused by light
- A testboard was used to mount the strips and chip, and to supply control and voltage lines
  - One chip supply voltage regulator always was extremely hot, above 60 degrees

# Measurement instruments




- All data was taken using a LeCroy digital scope
- The output of the beetle chip basically is one analogue amplitude from one single point of time for 128 channels sent sequentially (plus a digital header in front)

- The scope was read out via Ethernet using a PC and LabView; **Data taking was done manually**
- The data was saved in text files using a simple “point-in-time amplitude” format for analysis and plotting
- Clear separation of the channels, and thus determination of the output amplitude of a given channel was a critical task with our data taking method, and not always 100% stable
  - The time<-> channel relation in the data files is established by a trigger of the scope and the position of this trigger in the scope memory

# Control

- The beetle chip was controlled via an I2C interface from a control board in the VME crate
- External triggers were generated by a VME board
- Both these boards were addressed by the crate controller CPU over VME

# Analysis

- Quick analysis was done using MS Excel for simple tasks and plots
- Root was used for more demanding tasks

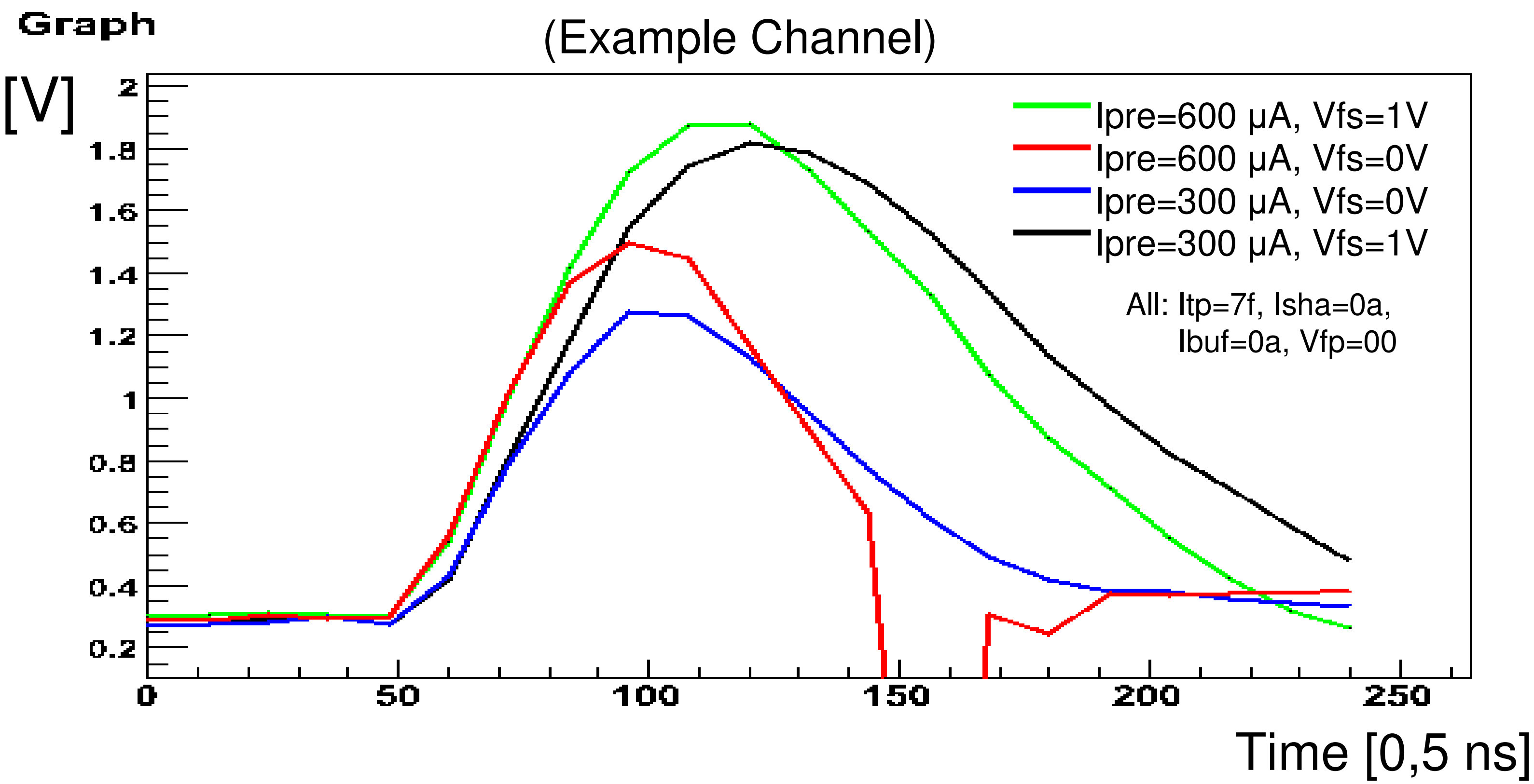
# Beetle testpulse

- Test pulses could be injected directly into the preamplifier of the chip
  - The chip sees the silicon during this measurements through the inputs, but its more or less “dead”
- The readout pointer(in an internal readout buffer) could be set in respect to an external trigger in steps of 25 ns
- The trigger to testpulse relation could be set in 0.5ns steps
- We “walked” the pulse by changing the trigger-pulse timing in 6ns steps, at each step taking one set of data; thus measuring the shape of the testpulse for all channels simultaneously

# Shaper

- For our measurements the following shaper values/registers were changed:
  - **Ipre** sets the preamplifier bias current; Higher Current -> decrease in risetime
  - **Vfs** controls the shaper feedback resistance; higher values -> enlarged peaking time and voltage

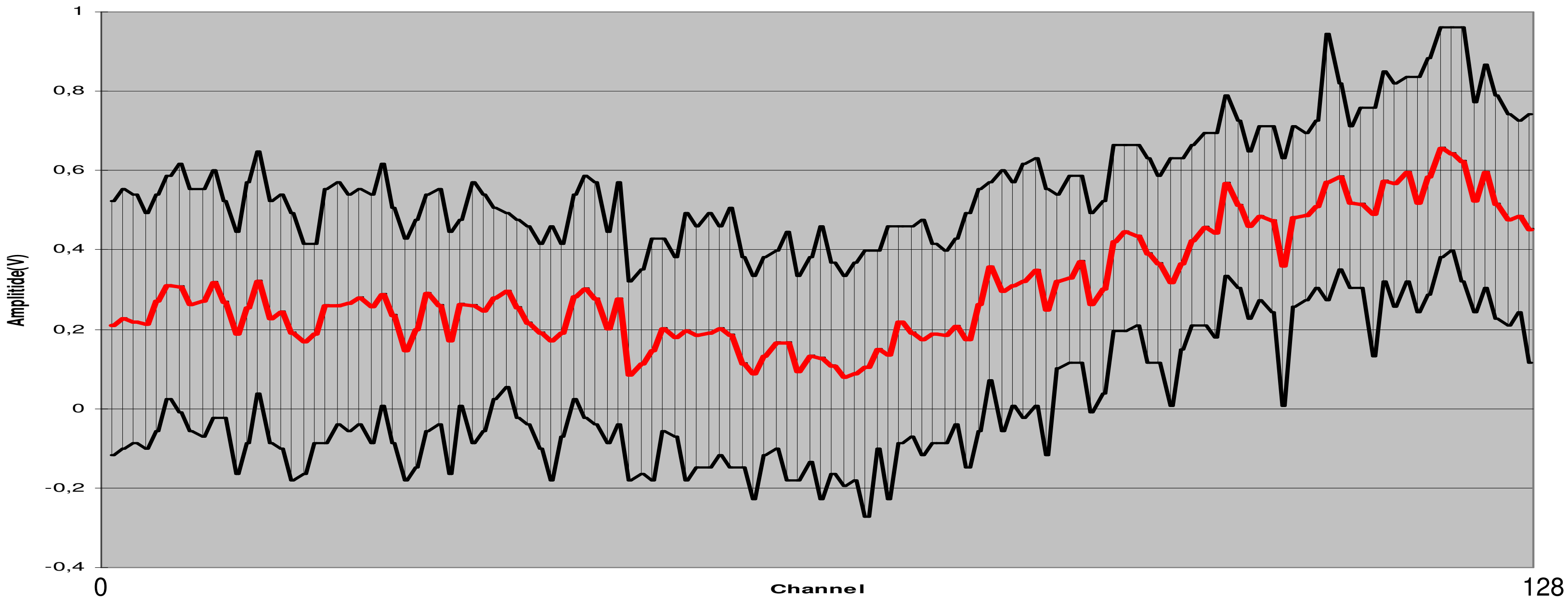
- Beetle testpulse and shaper
- Noise and pedestals
- Depletion Depth/external bias Voltage
- Cosmics(?) and source




- The effect in the red curve is probably a timing glitch, data points around(or after) 75ns probably coming from a neighbouring channel (the testpulse is inverted on injection for neighbouring channels)

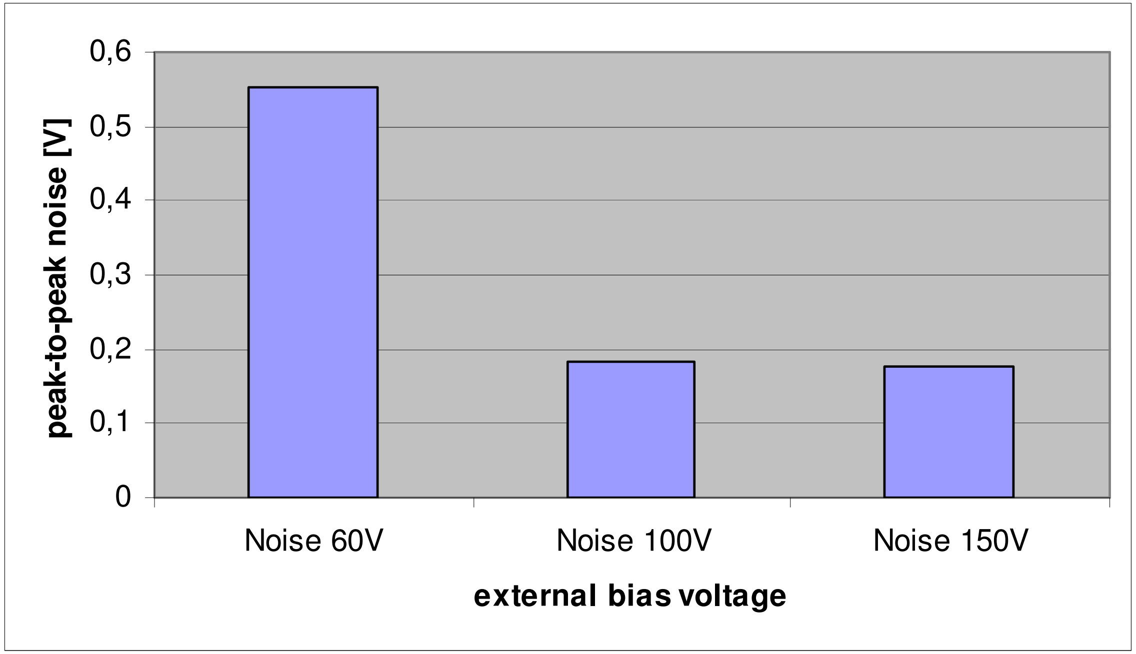
# Noise and pedestals

- The average and envelope of the analogue data over many (of the order of 1000) measurements was taken

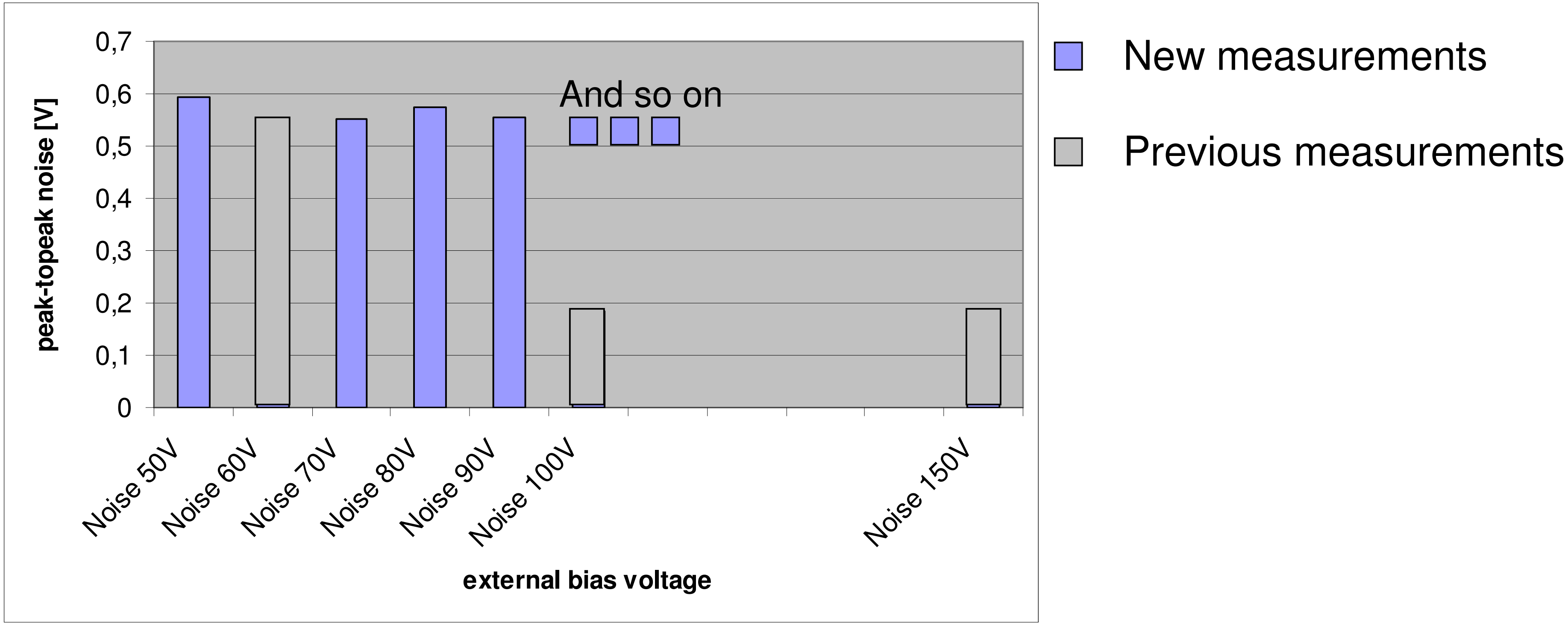


# Depletion Depth

- Our first approach was to exploit the expectation that the noise is inverse proportional to the depletion depth
- The depletion depth should be roughly proportional to the square-root of the external bias voltage
- Thus by changing the external bias voltage and measuring noise characteristics we tried to measure the depletion depths and find the point of full depletion




- First results look promising -> supposedly full depletion is reached before 100V external bias voltage
  - Decision on more data points was taken

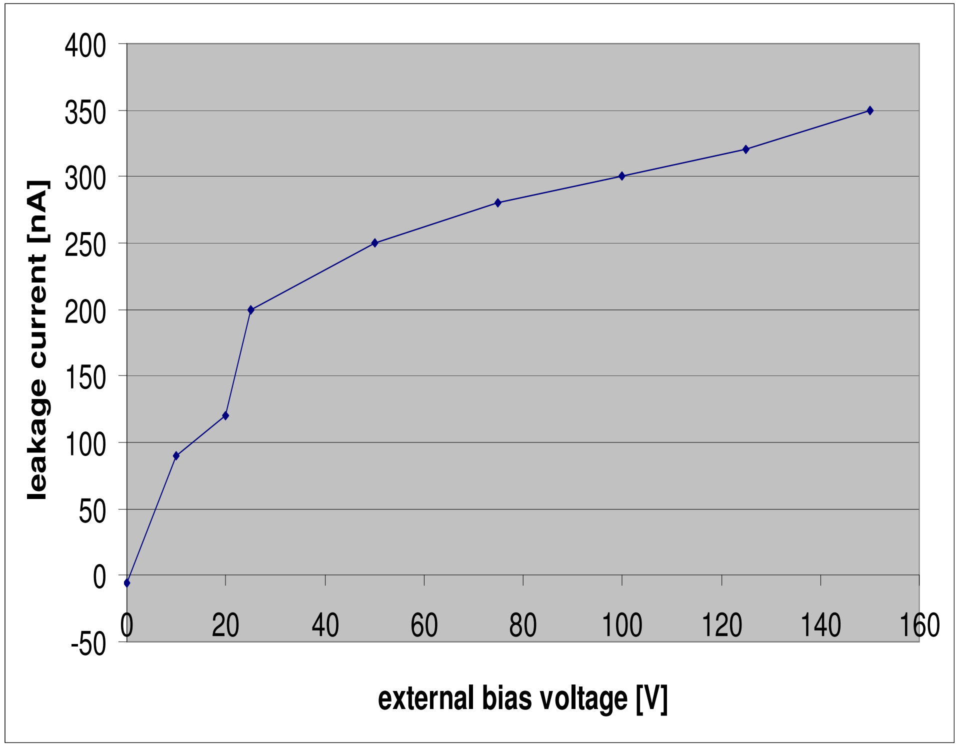



- No relation of external bias voltage to noise could be seen anymore

# Interpretation

- Due to the DC-coupling of detector to the chip it could be that the noise/depletion depths relation can not be measured
- The assembly was quite warm due to the hot voltage regulator and enclosed box, thus the thermal noise probably dominated the later noise measurements

# Leakage current



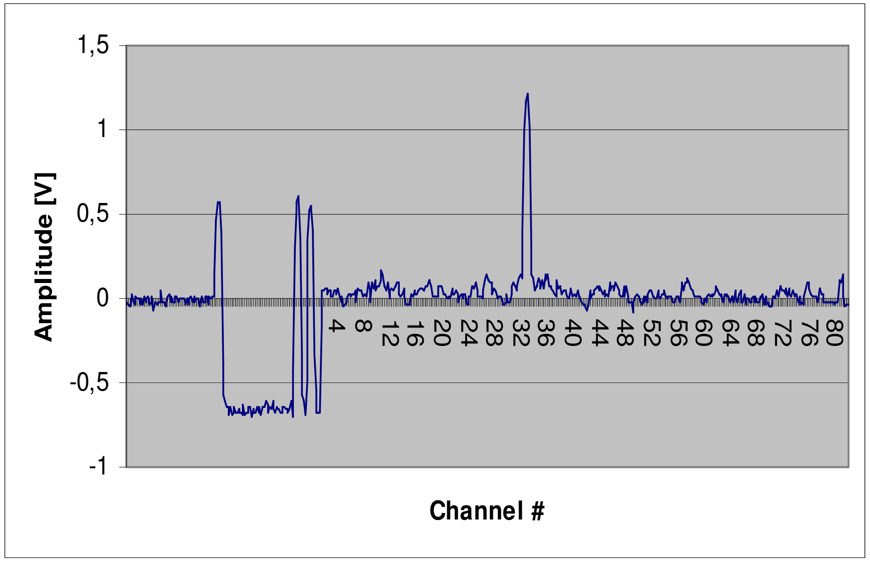

- To check if the external bias voltage had any effect on the silicon strip characteristics we measured the bias voltage
- -> The assembly still worked

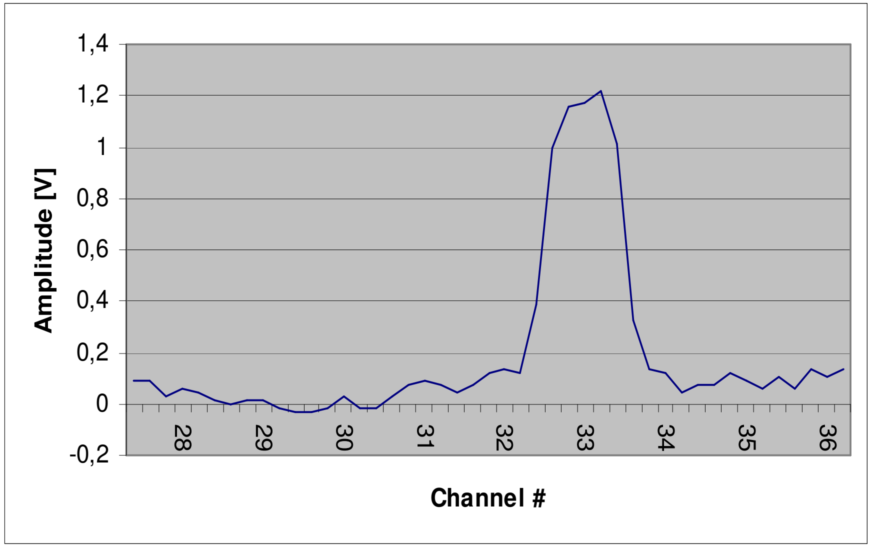
# Cosmics?

- We tried to measure some cosmics signals, but did not succeed
  – The large noise (temperature of 30° in comparison to normal operation at -10°) did, if maybe not being the main reason for failure, surely impede the measurement

# Using a beta-source

- We inserted a strontium-90 source into the box, right underneath our strips



# Conclusions

- Our operation conditions were suboptimal, mainly concerning the operation temperature and thus noise
  - The system was also not fully stable over time
- But still some nice measurements could be made
- The learning factor was quite large for all of us