

# ATLAS and its Trigger System

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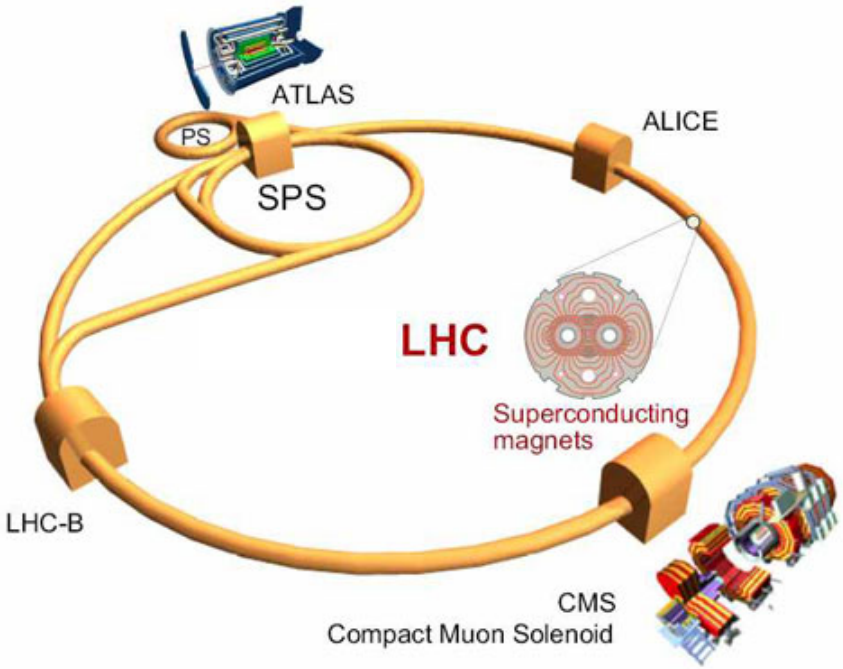
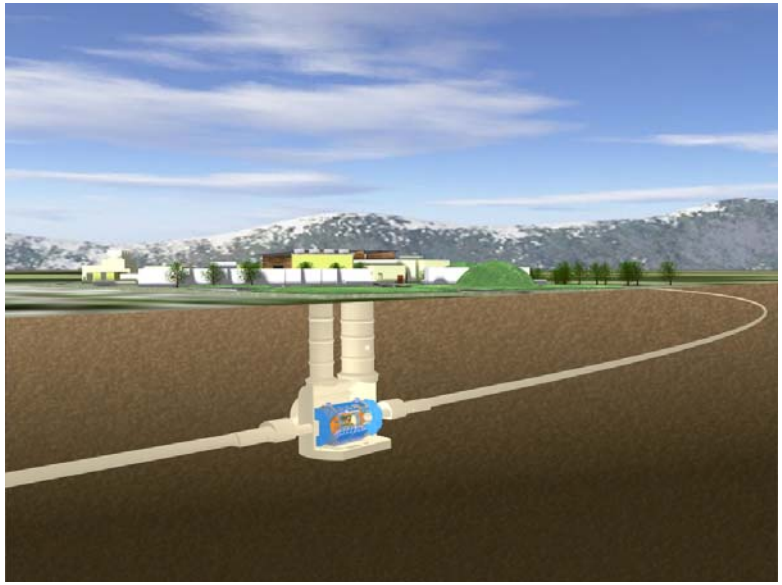
Deutsche Forschungsgemeinschaft DFG

International Research Training Group
Development and Application of Intelligent Detectors

## Large Hadron Collider

- two counter rotating beams of protons
- proton-proton collisions every 25 ns
- $E_{kin,beam}$=7 TeV, $E_{cms}$=14 TeV

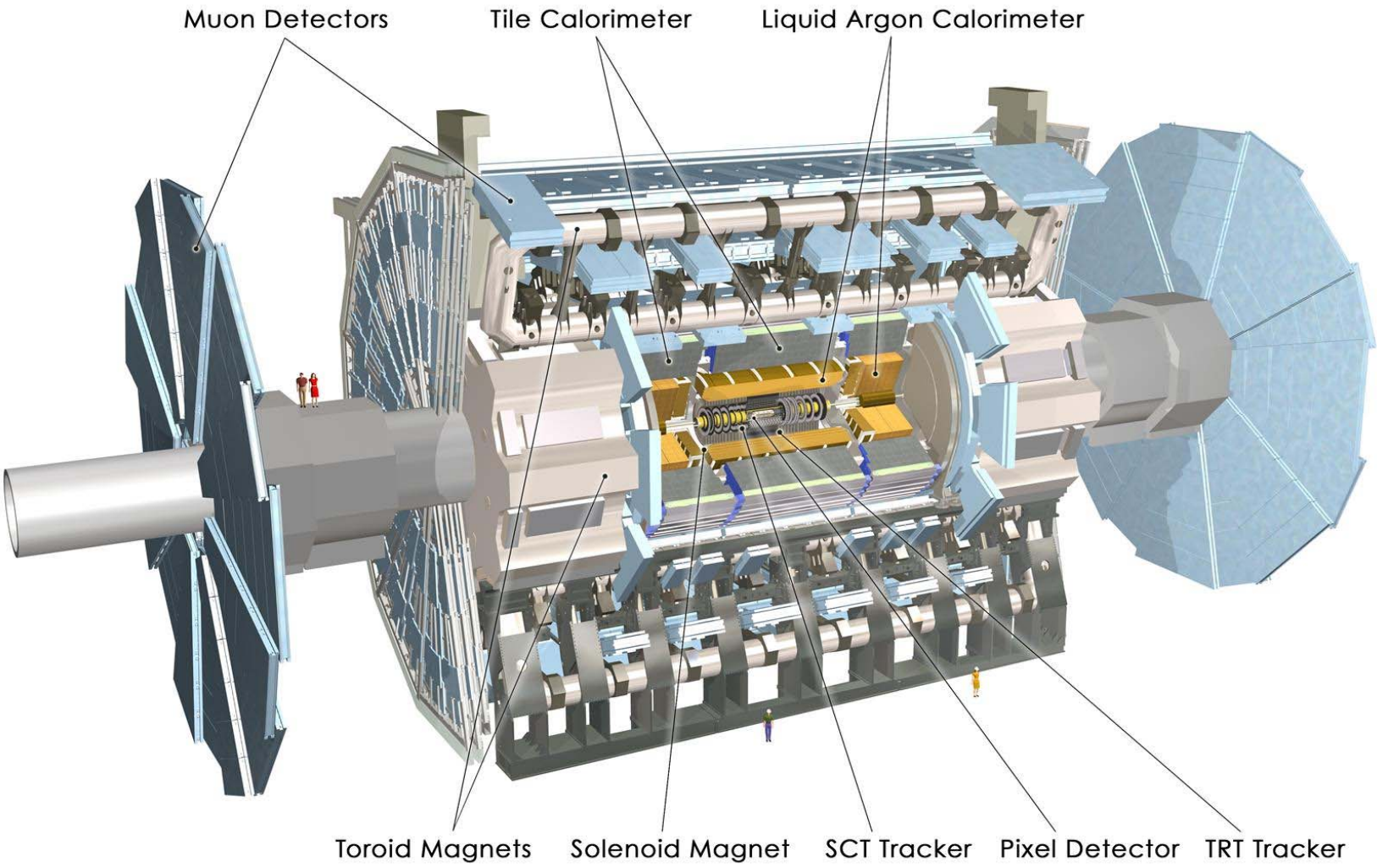


## A Toroidal LHC ApparatuS

- general-purpose experiment
- large collaboration:
  - 169 institutes & universities from 37 countries
  - 2500 physicists (~30% students)

# ATLAS Detector




Length ~ 45 m  Height ~ 24 m  Weight ~ 7000 tons

# Data Reduction

- interesting signatures: detection efficiency threatened by *background*

- ~ $10^8$ detector readout channels
- bunch crossing rate: 40 MHz
- average event size (ATLAS): 1.5 MByte

storage rate ~ 60 TBytes/sec

↓

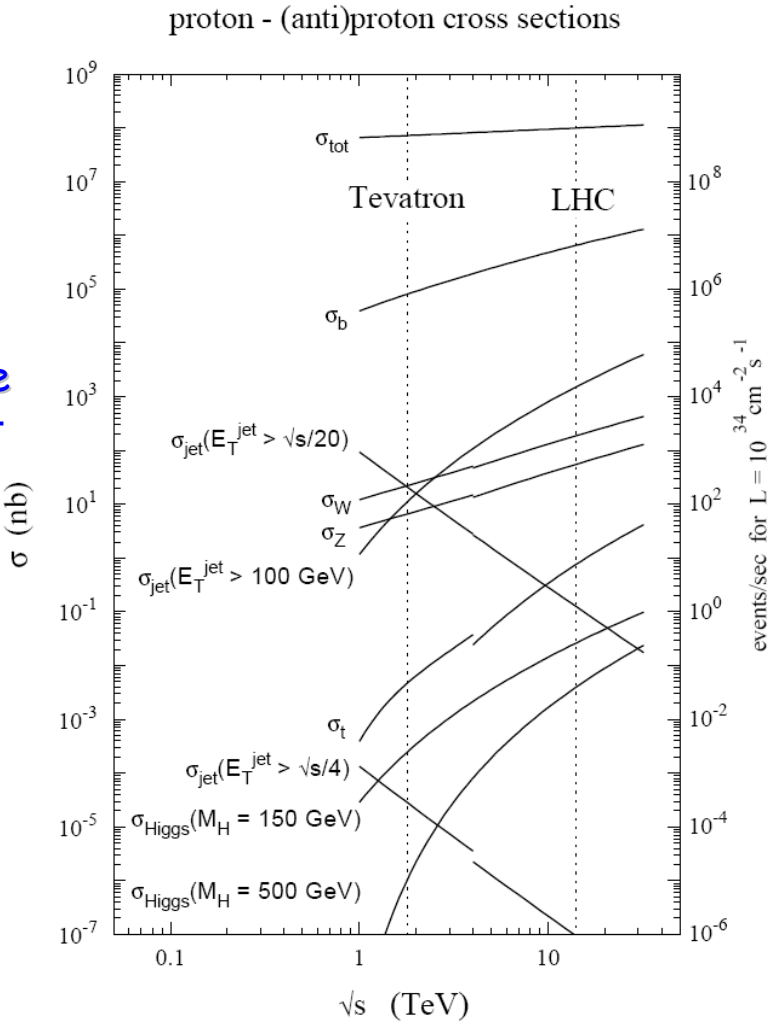
~ $10^5$ CDs/sec

↓

~ 100m CD stack/sec

↓

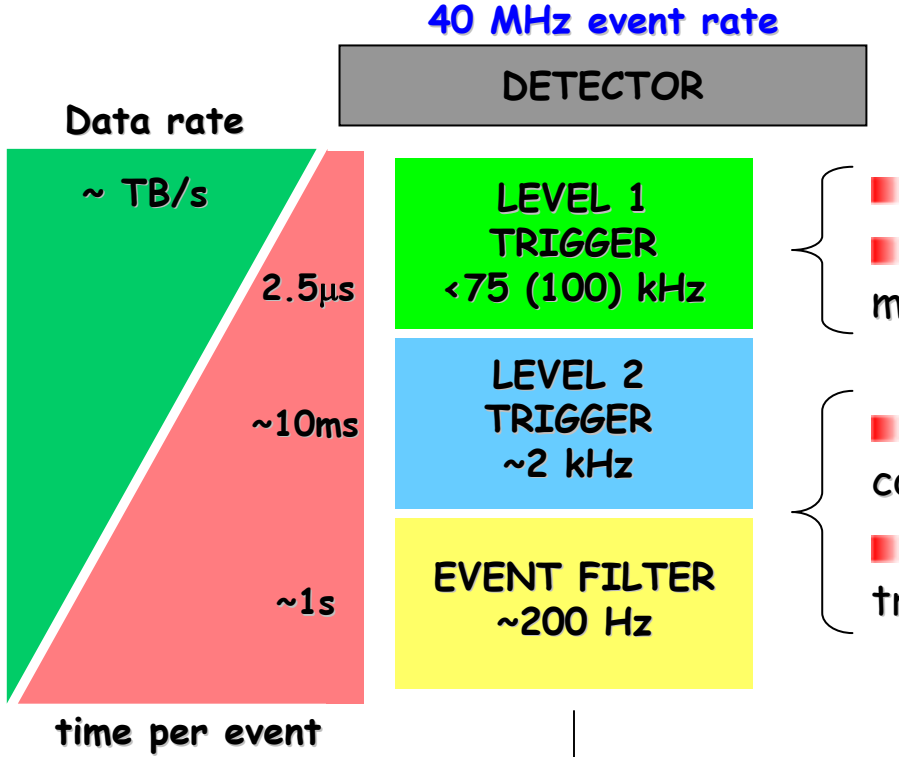
~ 2x distance to Moon/year !!!




**Therefore …**

Reduce the event rate to the amount compatible with the offline computing power and the storage capacity, while selecting the interesting physics with high efficiency → **TRIGGER !**

# The ATLAS Trigger System

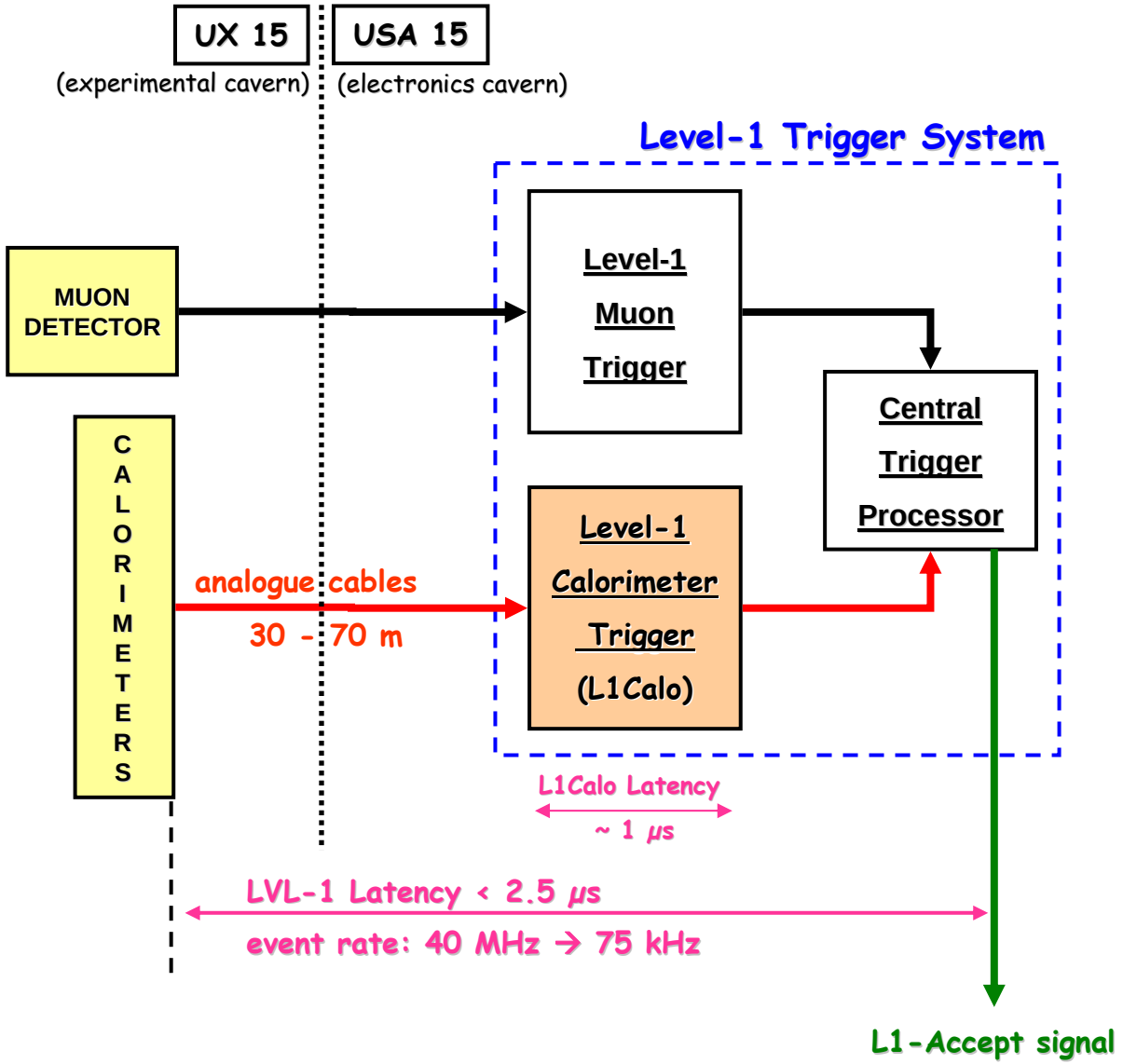



- hardware based (ASIC, FPGA)
- coarse granularity calorimeter & muon $p_T$

- software algorithms (large computer farms)
- full granularity (including tracking)

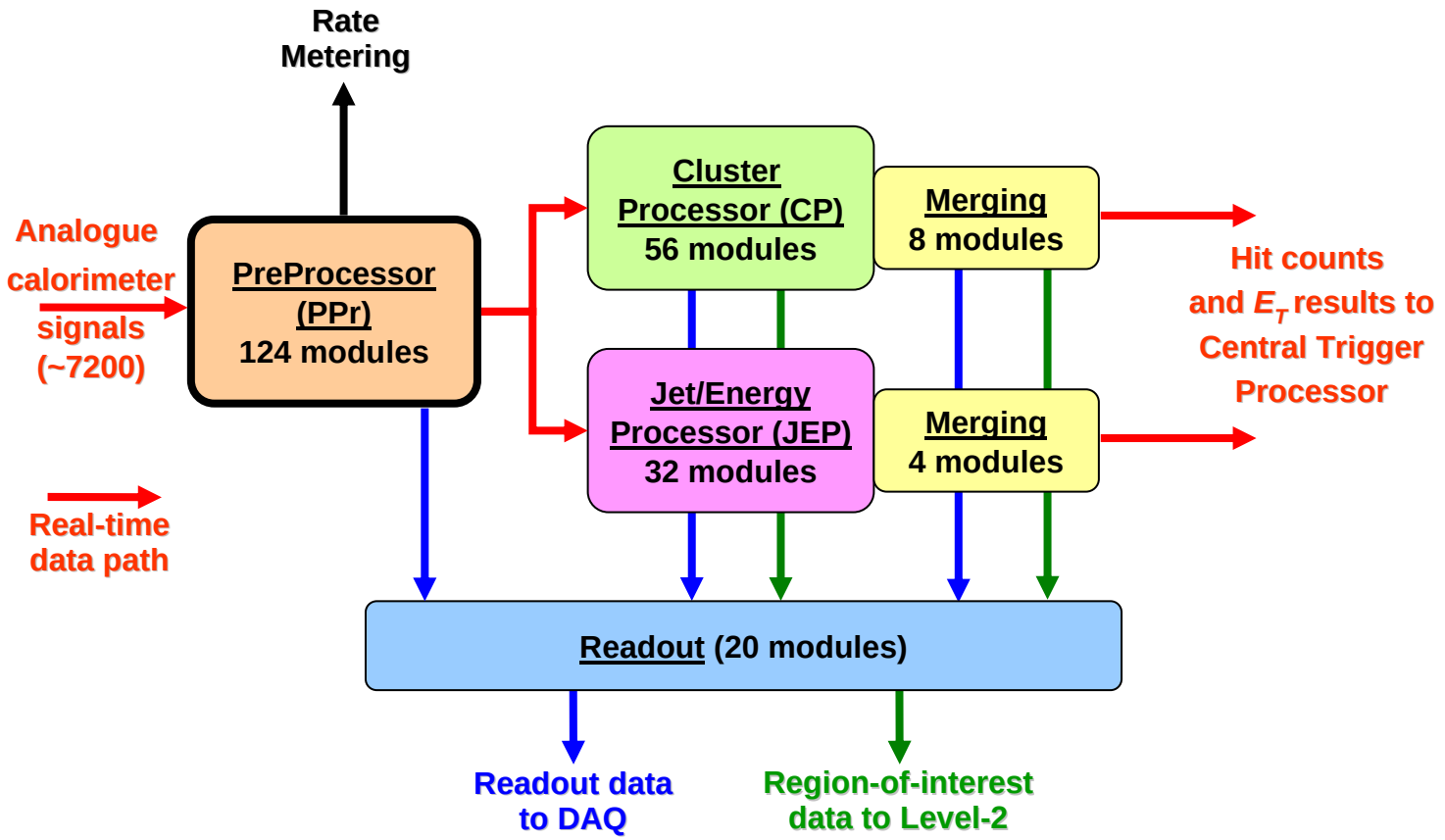
# The Level 1 Trigger System





# The L1Calo Trigger






L1Calo Collaboration

- University of Birmingham
- University of Heidelberg, KIP
- University of Mainz
- Queen Mary, University of London
- STFC Rutherford Appleton Laboratory
- Stockholm University

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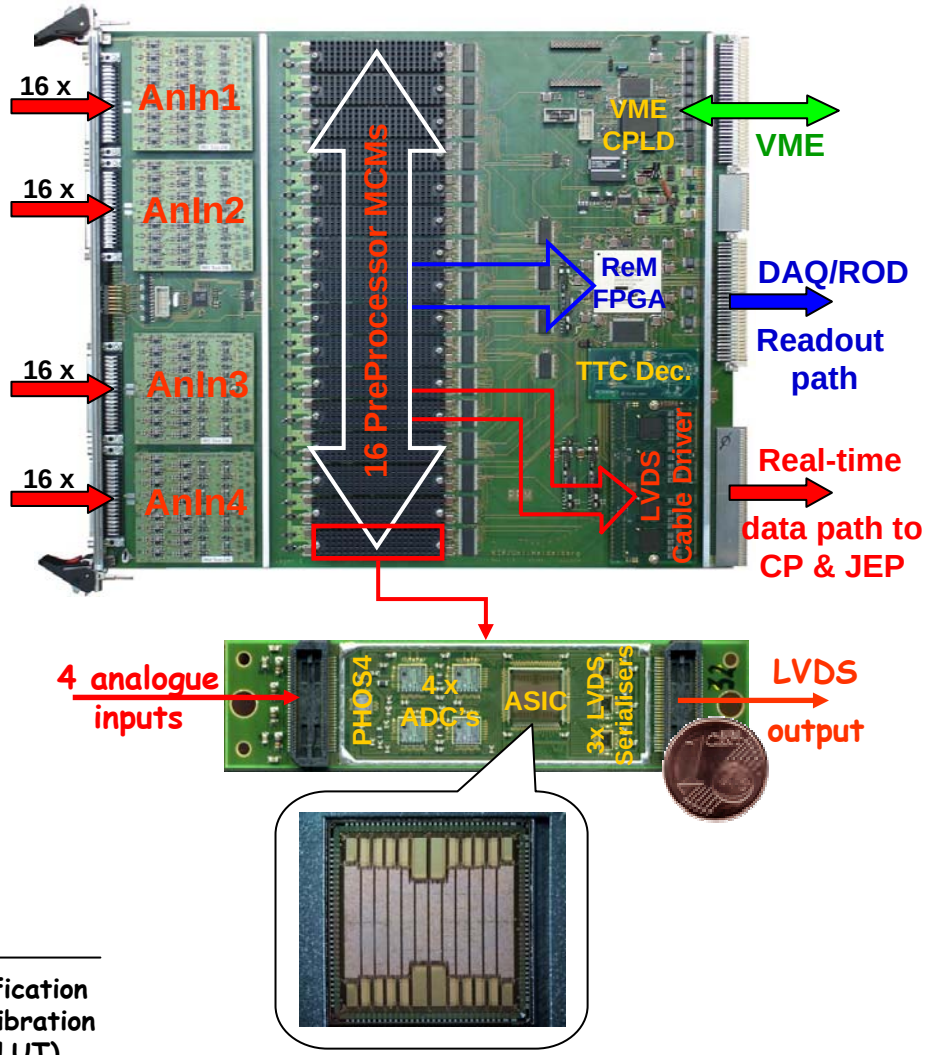
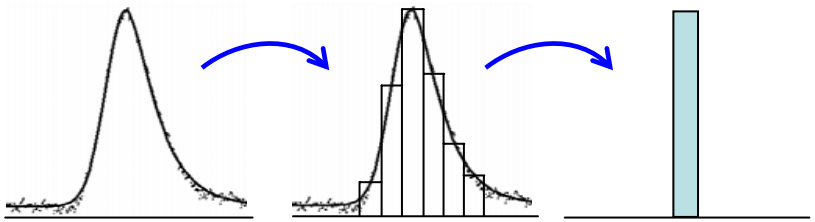
# The PreProcessor Module

- main component of the PreProcessor System
- **124** hardware identical modules which fit into **8** VME crates
  - input: **64** analogue calorimeter signals
  - processing in custom ASIC (designed @KIP Heidelberg)
  - output: real-time calorimeter data (to CP & JEP)

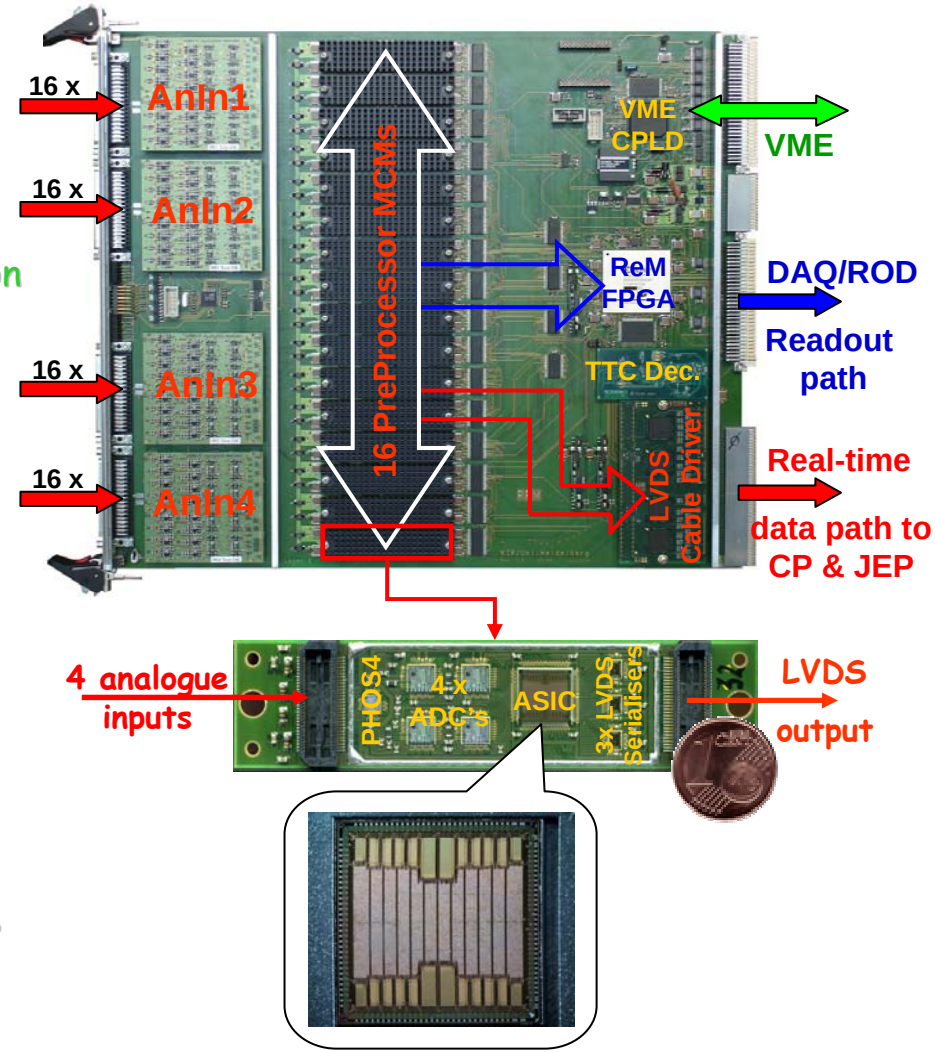


# The PreProcessor Module (cont'd)

## Readout Merger (ReM) FPGA

- Tasks:
  - collects, assembles and sends event data (readout)
  - intermediates board configuration & control
  - collects and provides monitoring data (e.g. rates)
- Xilinx Virtex XCV1000E
- hardware description language: Verilog
- design is using less than 50% of the FPGA resources, e.g.:
  - number of Slice Flip-Flops: ~40%
  - total numer of 4 input LUTs: ~42%



# PPM Production Tests @KIP Heidelberg



- PPM yield:
  - **124** modules needed by the full-coverage of the experiment
  - **36** spare modules
- Strategy: test all modules in Heidelberg before sending to CERN
- Single Board Tests (bring each module into operation)
  - **Initial preparation** (optical inspection, power up tests w/o daughterboards, etc)
  - **Operational tests** (check conditioning & digitisation, verify ASIC algorithms, etc)
  - **Readout data tests** (check buffer content & formation)
  - **Real-time (LVDS) data tests** (check transmission over long LVDS cables)

# PPM Production Tests @KIP Heidelberg (cont'd)



- Full Crate Tests
  - long term tests for the PPMs that have completed the Single Board Tests
  - standard PreProcessor crate fully equipped with 16 PPMs
  - repeat all functional tests performed during the Single Board Tests
  - successfully tested PPMs are sent to CERN

# L1Calo @CERN

Receivers & PreProcessors

Cluster & Jet\Energy Processors

Readout Drivers

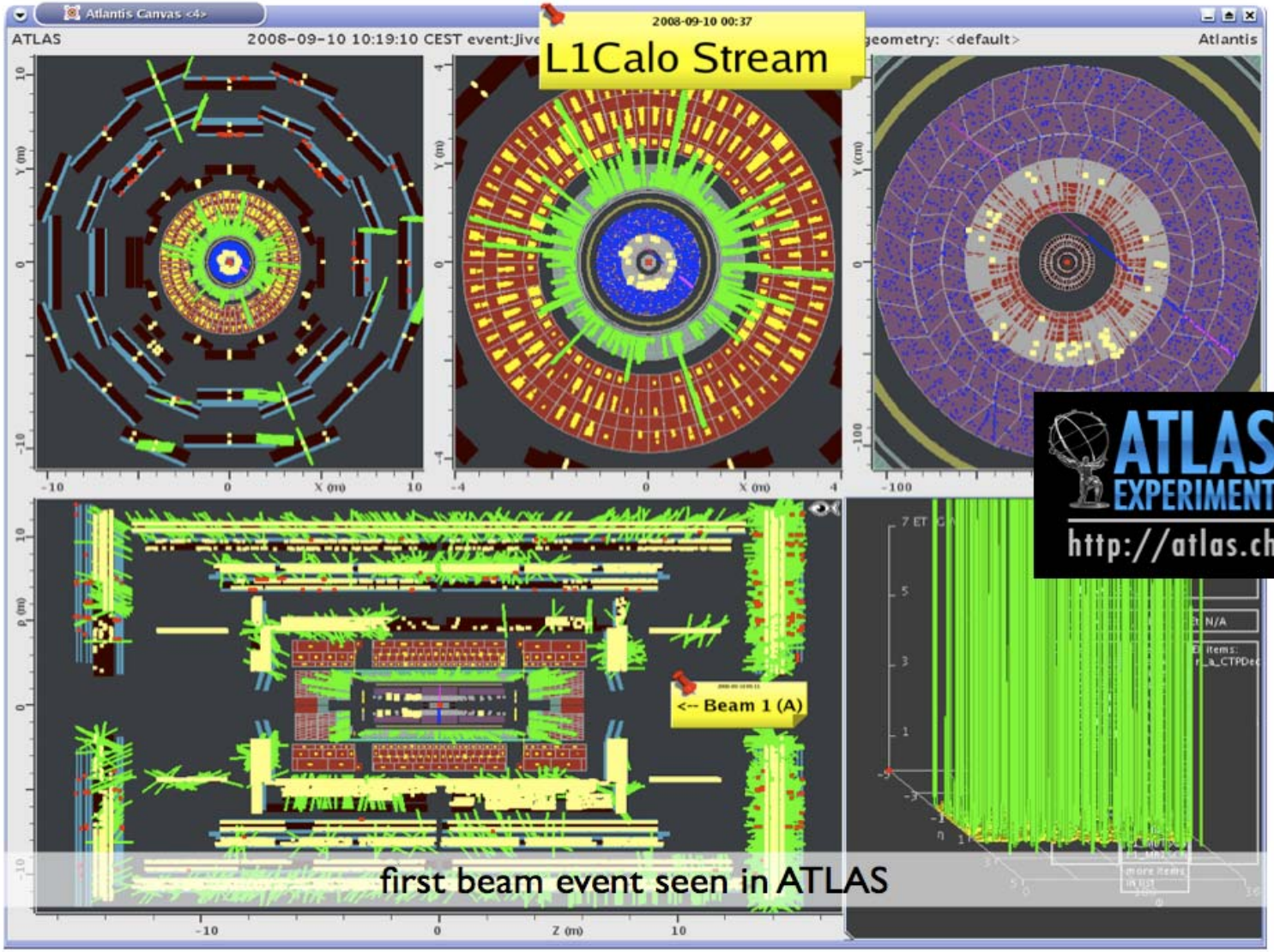
* Hardware installation finished since December 2007
* 2008: L1Calo successfully integrated with the other ATLAS sub-detectors in dedicated combined runs

# The Day of the First Beam



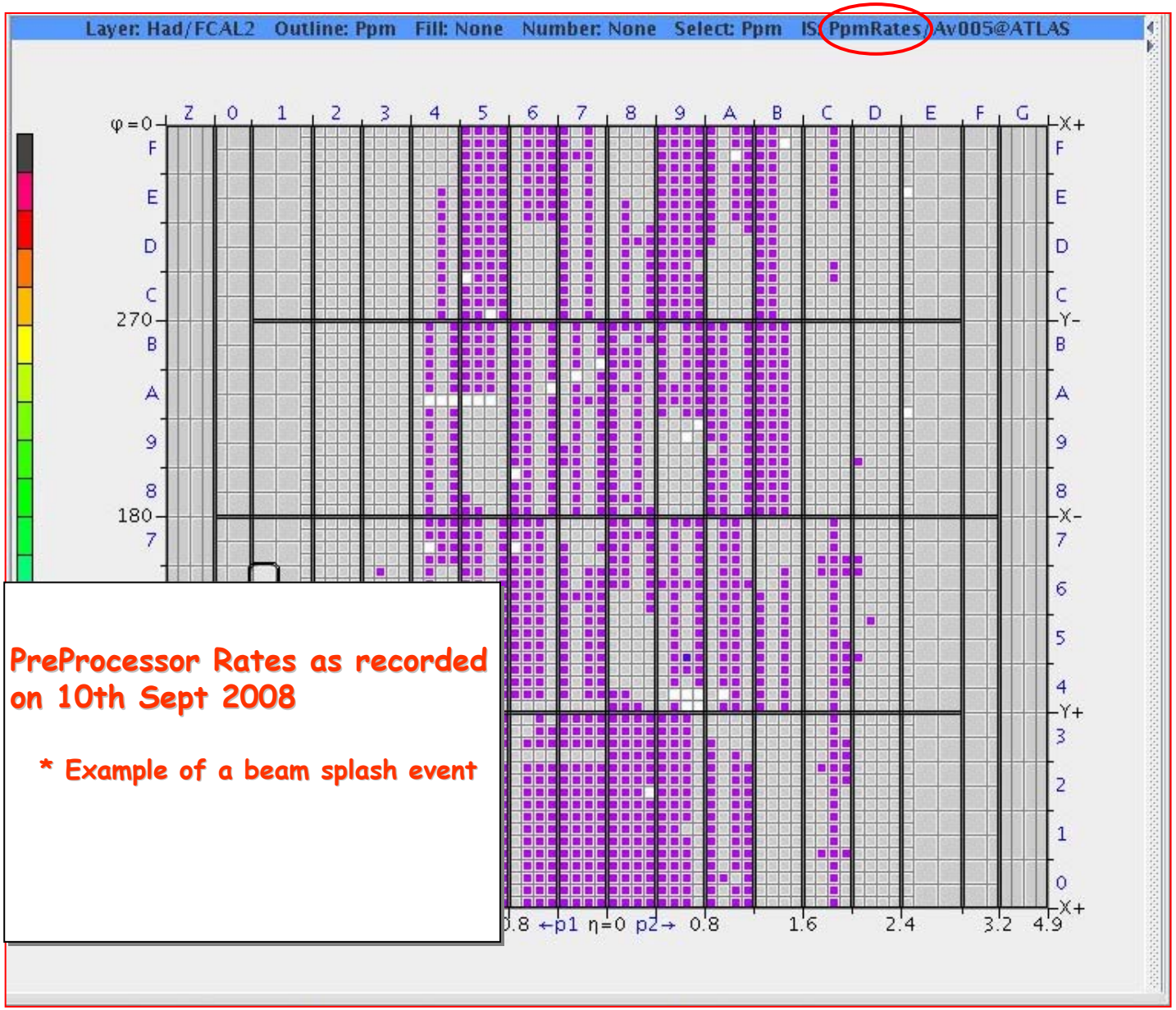

L1Calo Shift Desk

# The First Event



# The PreProcessor Rates






**PreProcessor Rates as recorded on 10th Sept 2008**

* Example of a beam splash event

# Summary

- PPM central module in L1Calo Trigger
- 124 PPMs @CERN after intensive testing & programming
- first beam event seen by the trigger