Basics of Dynamic Reconfiguration

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Introduction to FPGAs

- FPGA = Logic + Memory + Routing + support infrastructure

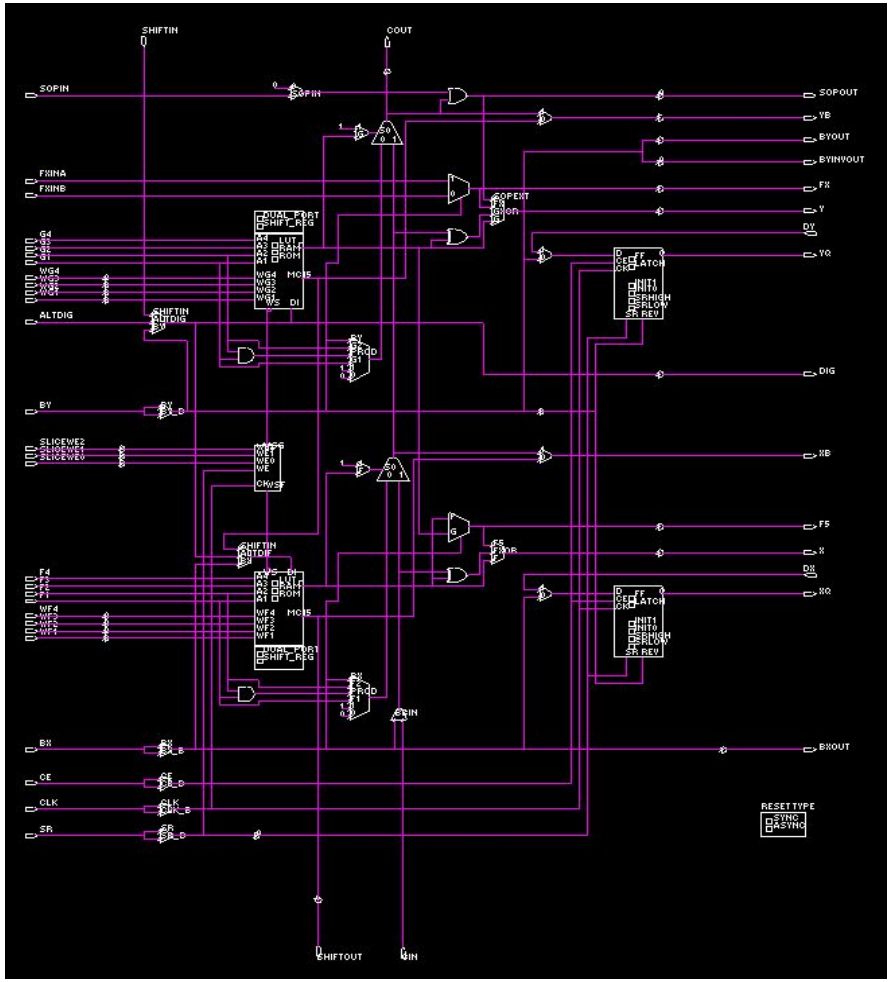
- Logic: LUTs (lookup-tables)
- Memory: flip-flops
- Routing: multiplexers (local routing), interconnect structures
- Support: global clock trees, I/O pads, power

- Major Players: Actel, Altera, Xilinx

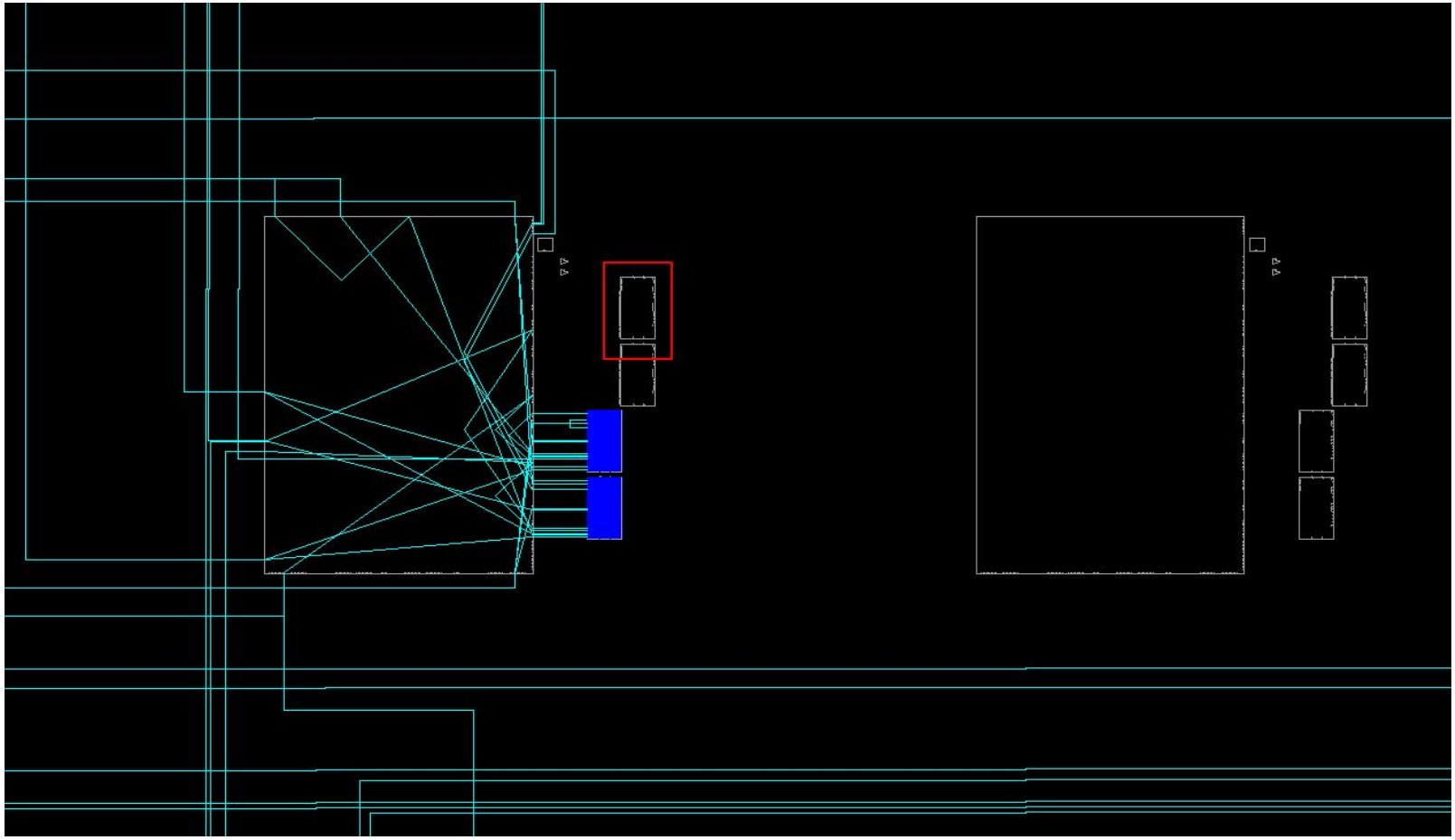
FPGA fabric

- Most common LUT: 4 inputs, 1 output (+inverted)
- Flip-Flops: configurable to different modes (D, JK; reset modes; clock edge selection; …)
- LUT + FF + local routing = “LE” (logic element, Altera), “Slice” (Xilinx, 2 LUTs + 2 FFs)
- 4 Slices + global interconnect = “CLB” (configurable logic block)

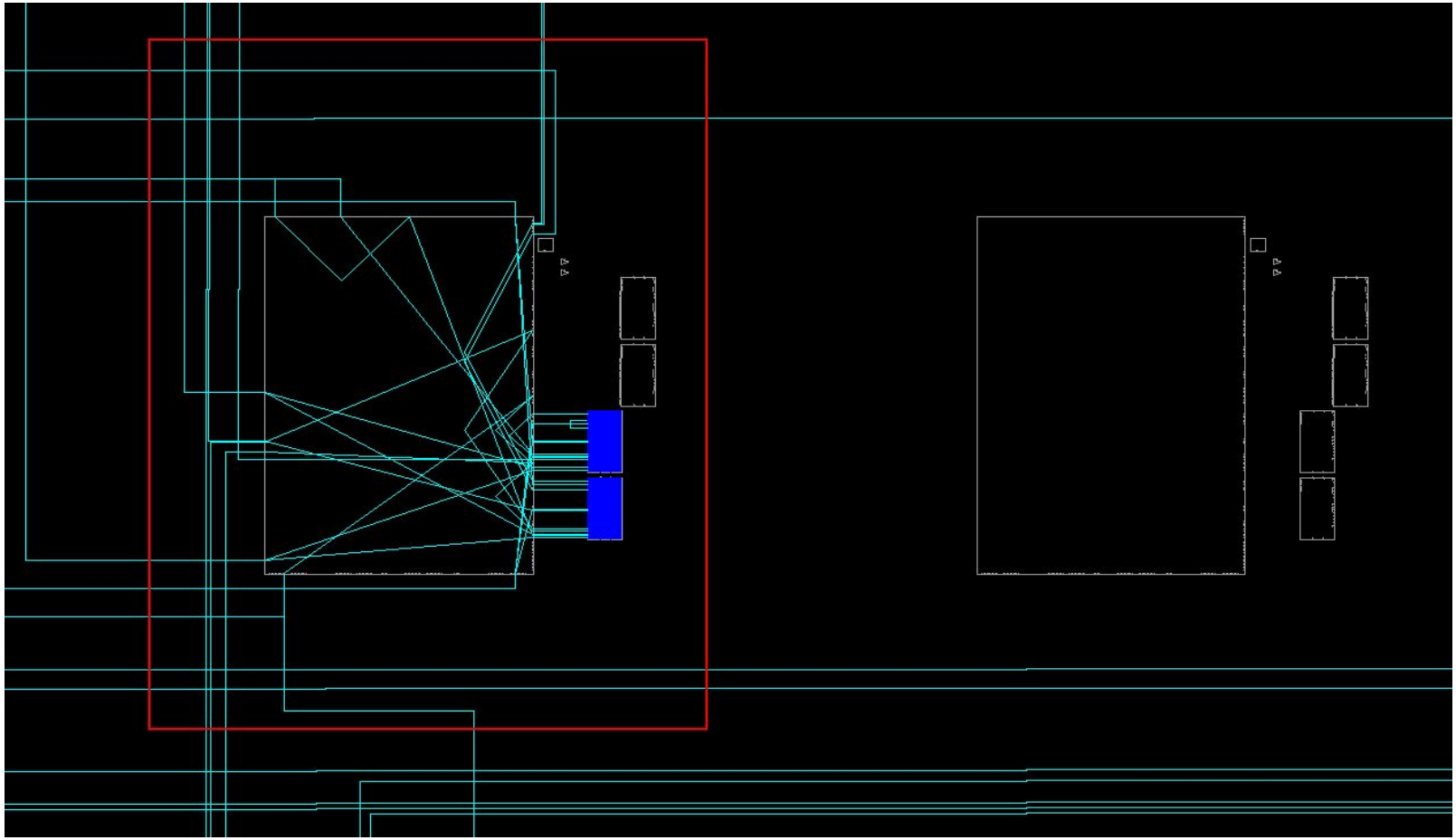
FPGA fabric: Slice



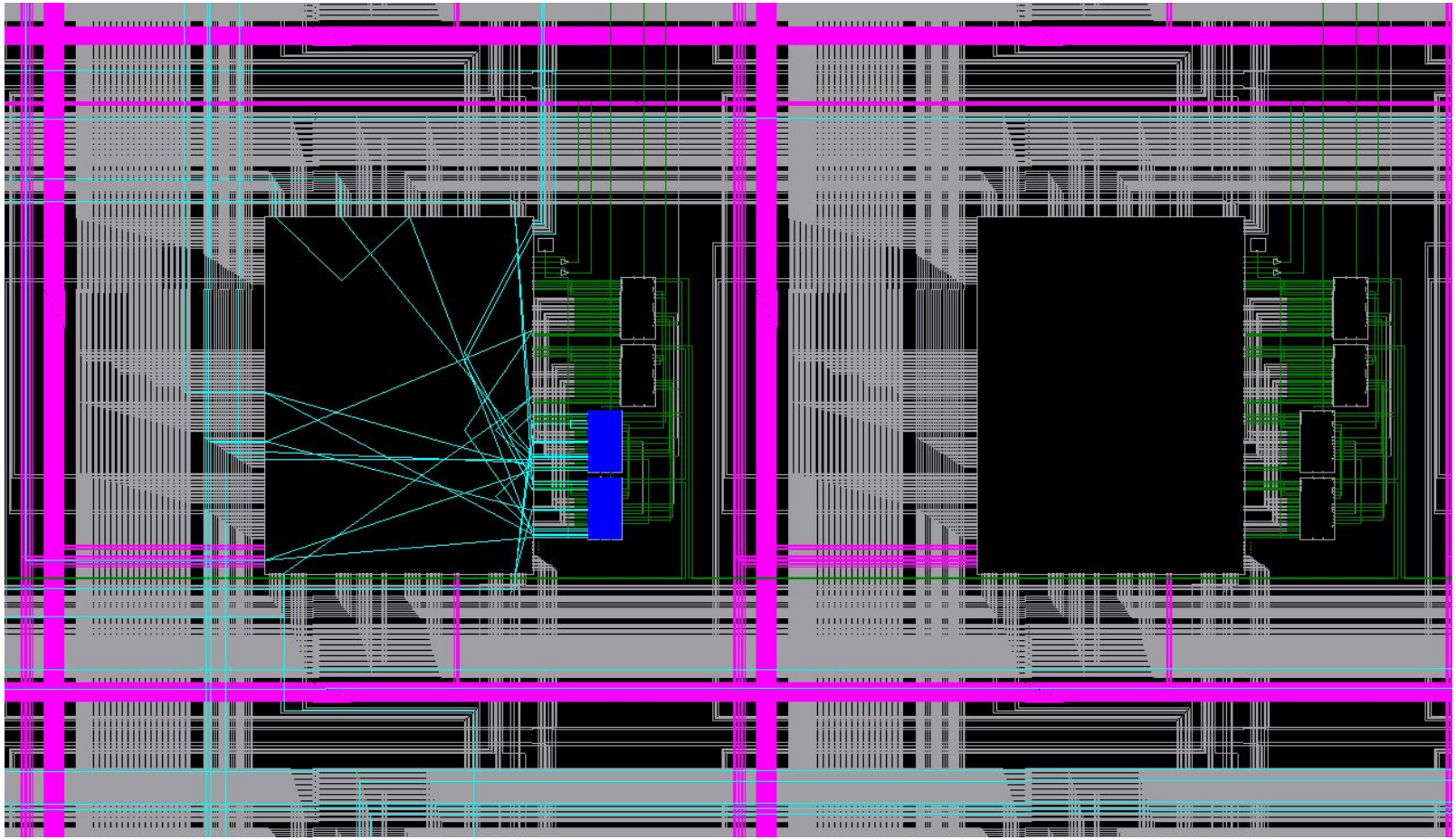
FPGA fabric: CLB



FPGA fabric: CLB



FPGA fabric: Routing



FPGA fabric

- All of the technology above is 20+ years old,
  - +/− tuning of parameters
- What are the innovative parts?

Special Features

- Clock Management: PLLs/DLLs, distribution
- Fixed Units:
  - Block RAMs
  - Multipliers (for DSP applications)
  - (De)Serializers (Multi-Gigabit Transceivers)
  - Processors (PowerPC, Arm)
  - near future: Ethernet MAC
- Others: I/O flexibility, radiation hardening
- Partial Reconfigurability

Reconfiguration

- Most commonly: full configuration only, device reset
- A couple years ago: multiple configuration planes, memory-mapped [out of production], swappable
- Active Partial Reconfiguration: ca. 6-8 years, since Virtex series, uninterrupted operation
- has spawned (or re-awakened) a dedicated field of research: “Dynamic Reconfiguration”, “Reconfigurable Computing”

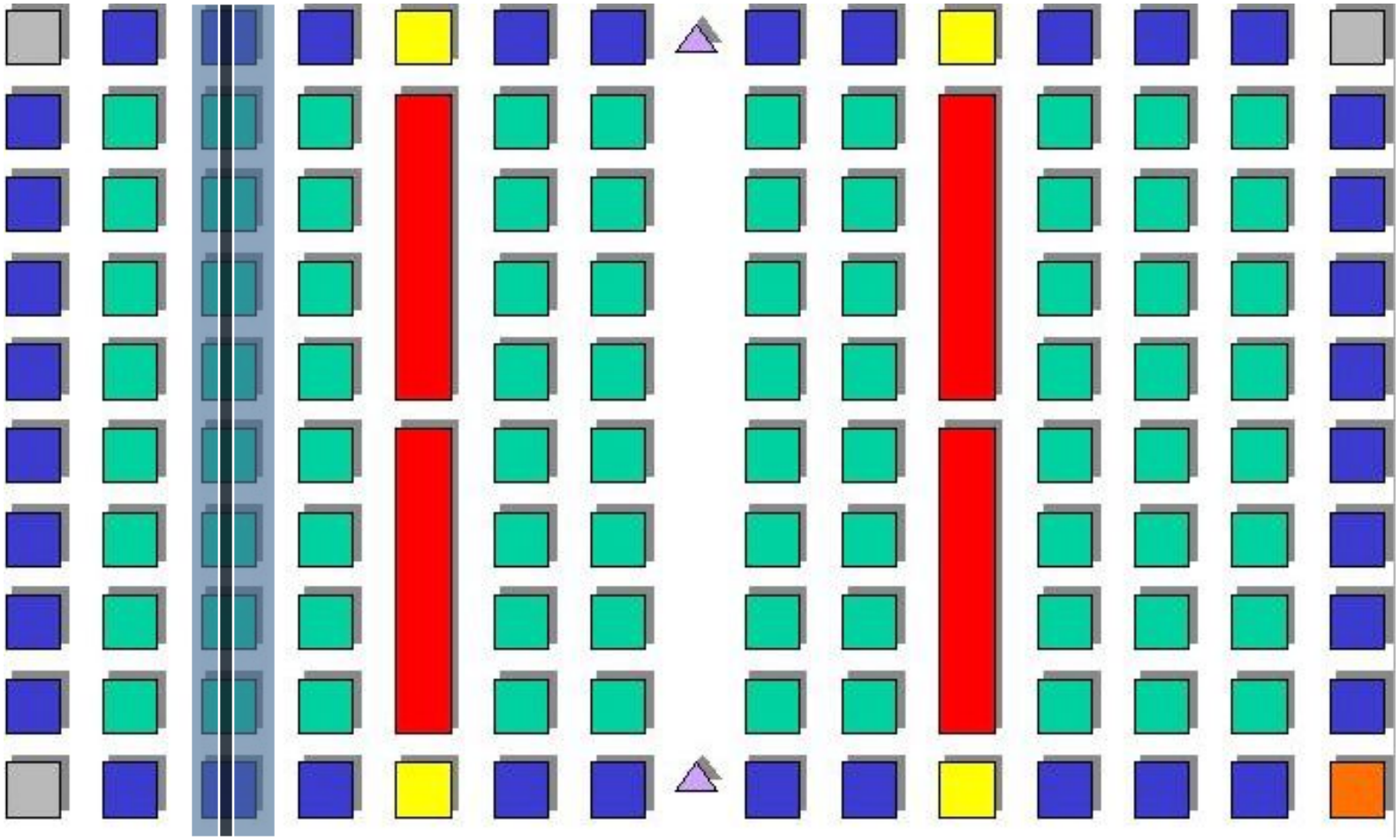
Active Partial Reconfiguration

- How does it work?

- Configuration Space divided into units, “frames” in Xilinx terminology
- ‘Partial’: frames are individually reconfigurable
- ‘Active’: without interrupting the device,

  glitch-free: no change → no signal flanks
- Configuration is ‘atomic operation’ (no bit shifting)

Configuration Frames



Benefits & Applications (1)

- **Functional Modules**
- **Flexibility in Time and Space**
  - **more functionality per device (time sharing)**
  - **several implementations for the same functionality (size/speed tradeoff) depending on avail. resources**
- **Can Use Smaller Devices**
  - **power & cost issues**
  - **HE physics and space applications: material budget, heat dissipation**

Benefits & Applications (2)

- More Flexibility for the Designs
  - replaceable functional modules
  - additional degrees of freedom for the algorithms

- Faster Design Space Exploration
  - for example when using genetic algorithms

Benefits & Applications (3)

- Routing

- Fact: FPGA = 90% routing, 10% logic
- Routing is a reconfigurable resource, too
- Can it be used, somehow?

- Difficulty: few appropriate models for datapath oriented programming

Benefits & Applications (4)

- **Fault Tolerance**
  - work around damaged cells
  - radiation tolerance
- **Alternative Path to Access Data**
  - for relatively slow data, like command & control, monitoring
  - saves a few FPGA pins
  - does not require special controller or busses inside the FPGA

App. In Intelligent Detectors

- Radiation Tolerance
  - Scrubbing
  - Identification of Radiation Sensitive Parts
- Routing
  - Potentially using the FPGA as a Delay Cell
- Command & Control, Monitoring
  - Combining all Devices of a System using the FPGA File System over the Network
- Functional Modules
  - triggers, filters

Problems

- Awareness
- Not fully developed, ready-to-use technology
- Design Methodology Issues
- Inherent Limitations

The End

Thanks for your attention.