Wafer test of the OTIS TDC-Chip for the LHCb Outer Tracker

~~19 May~~
~~28 July~~
~~02 June~~
23 June

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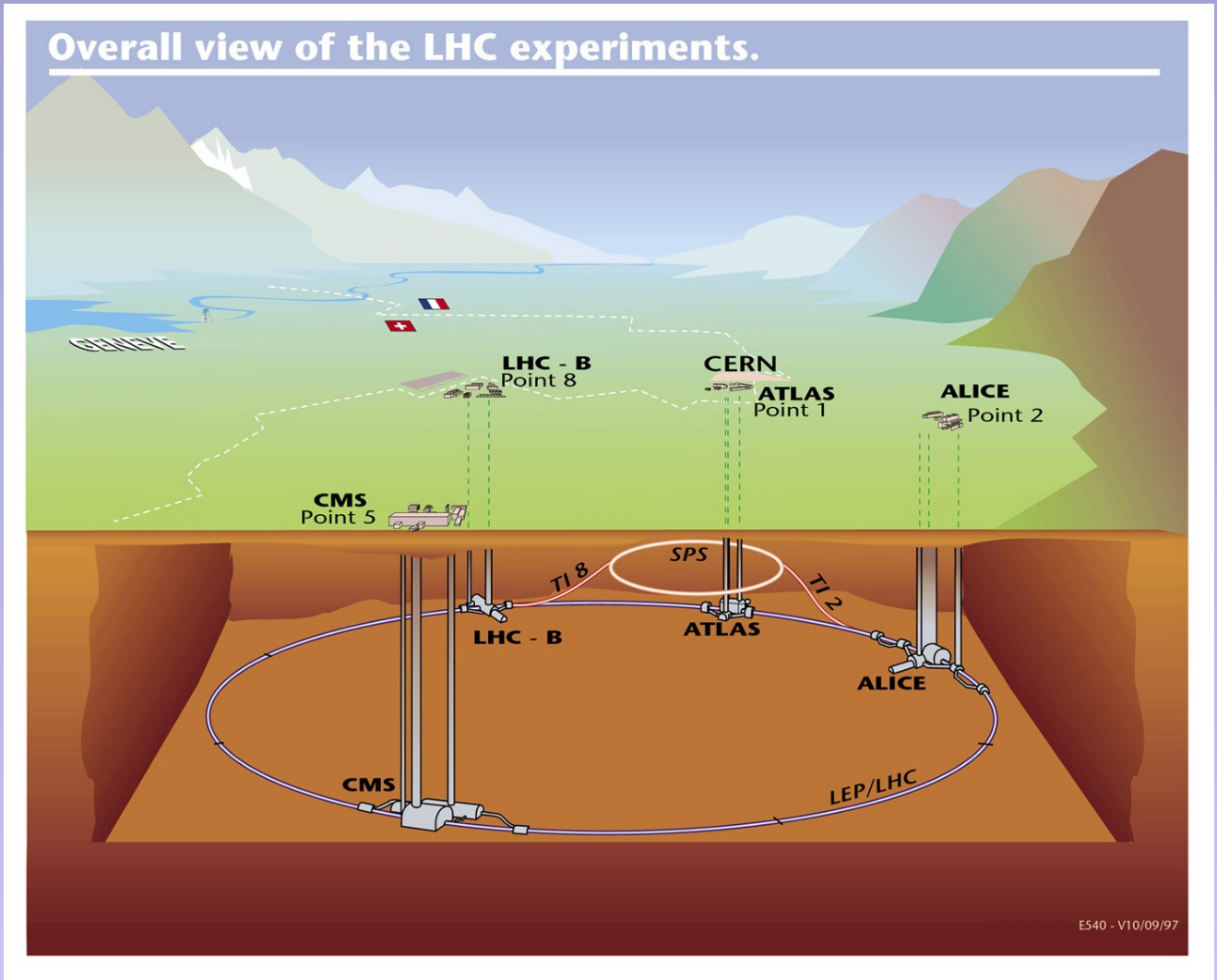
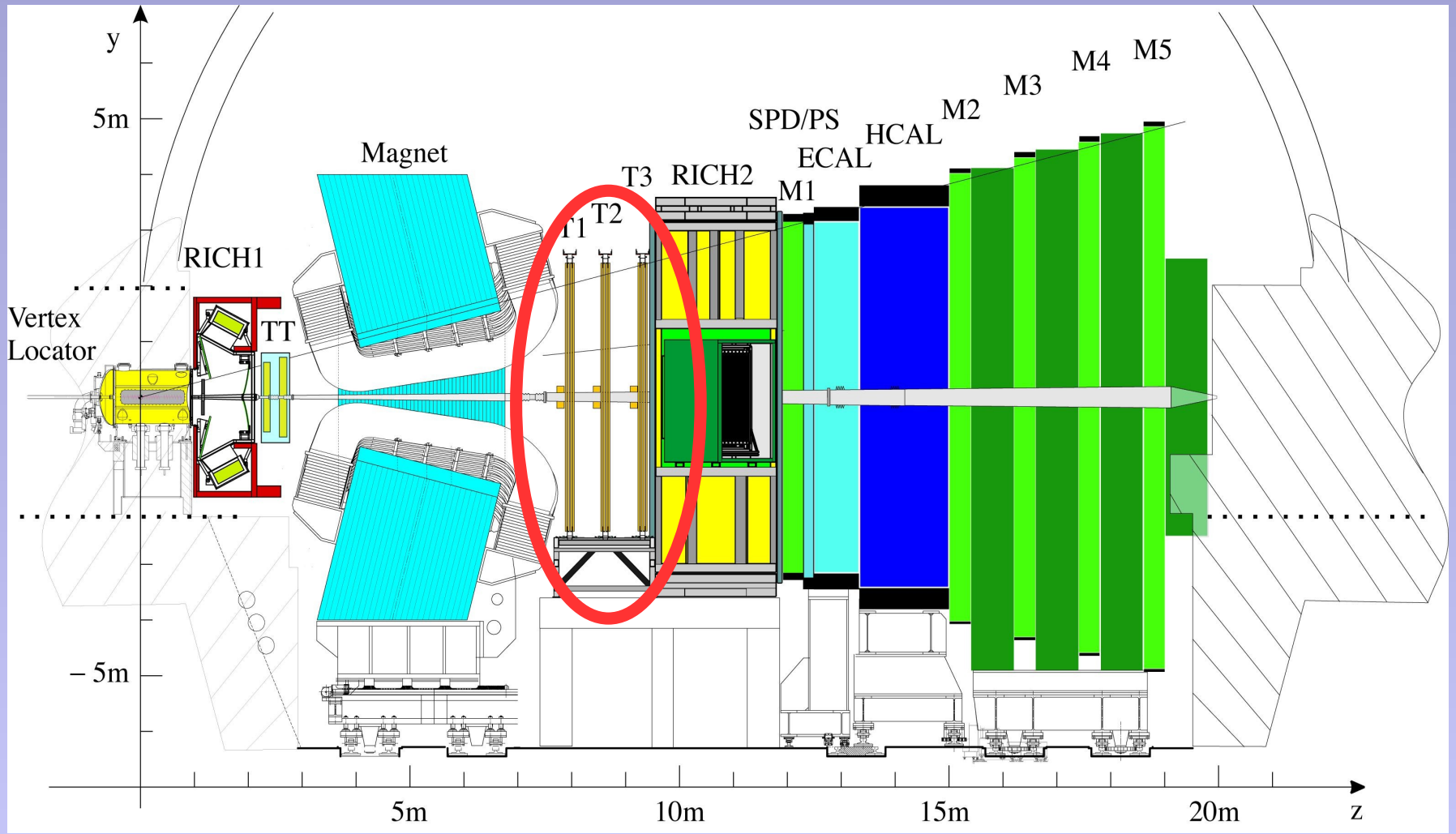
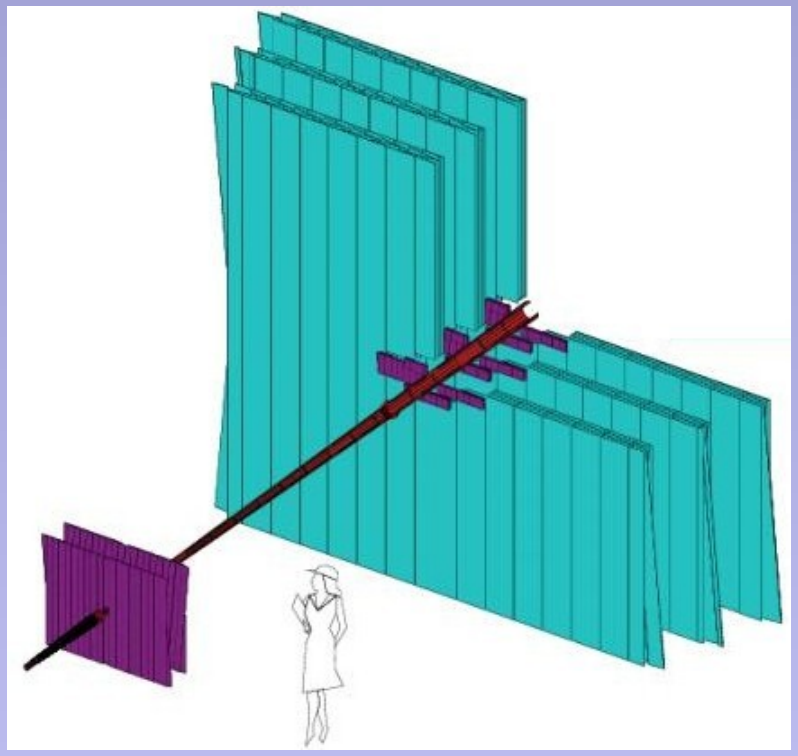
LHC


Overall view of the LHC experiments.
GENEVE
LHC - B
Point 8
CERN
ATLAS
Point 1
ALICE
Point 2
CMS
Point 5
SPS
TI 8
TI 2
LHC - B
ATLAS
ALICE
CMS
LEP/LHC
E540 - V10/09/97

LHCb detector

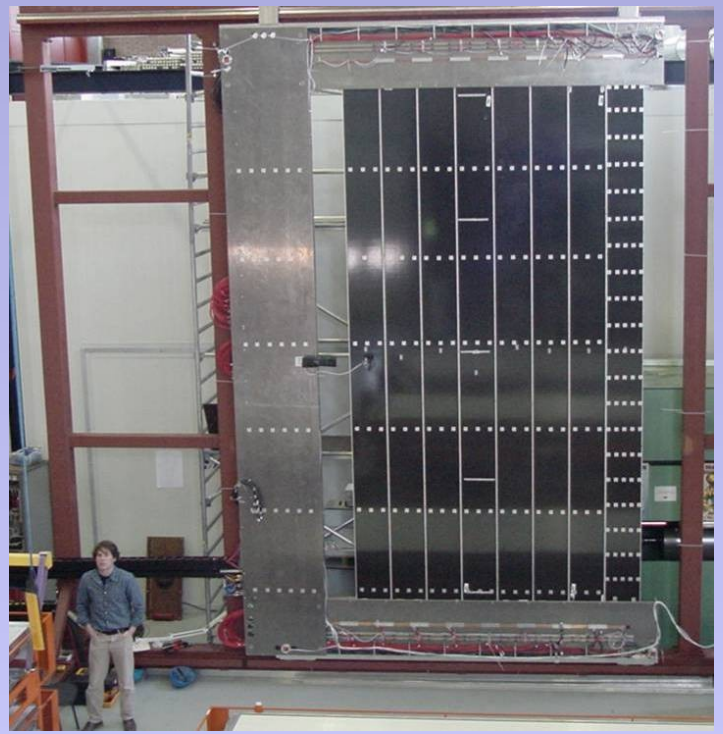


Outer Tracker

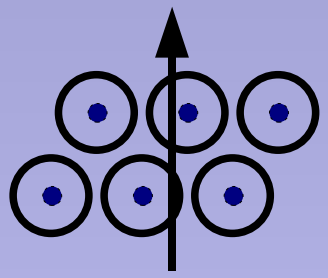


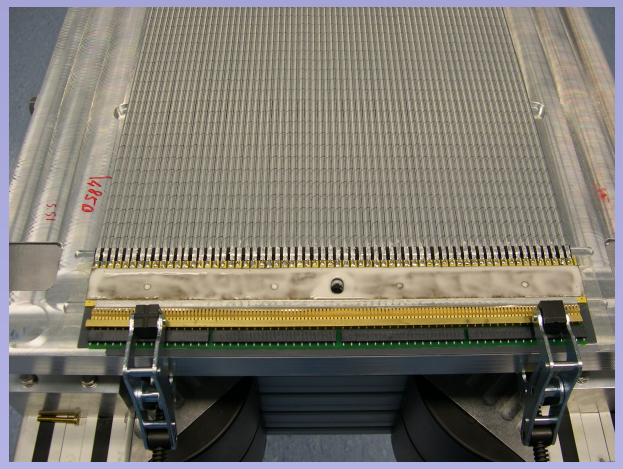
3 OT stations, each station houses 4 detector planes (X/U/V/X)

each plane comprises 1 double layer of straw tubes

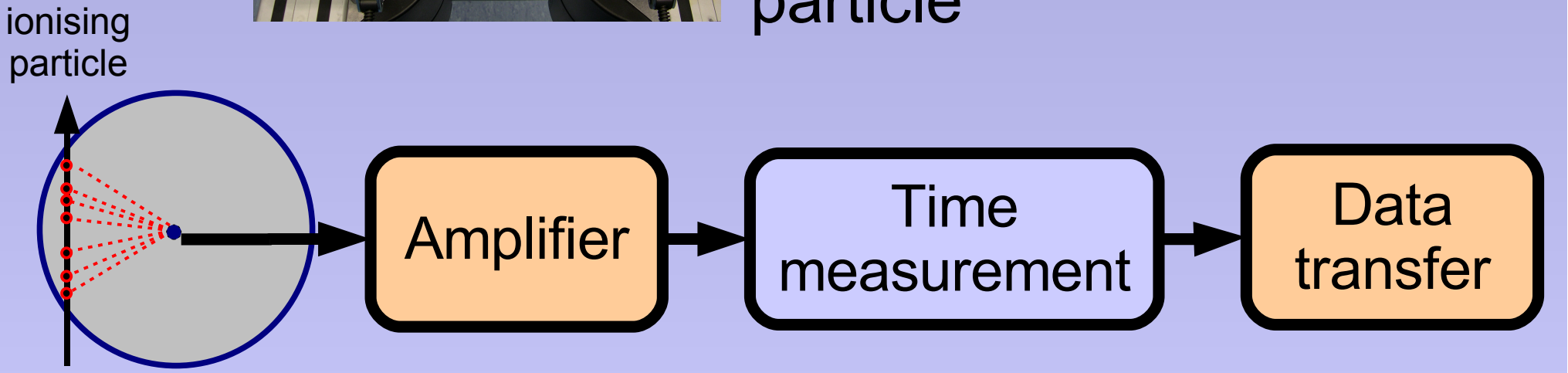


Outer Tracker (II)

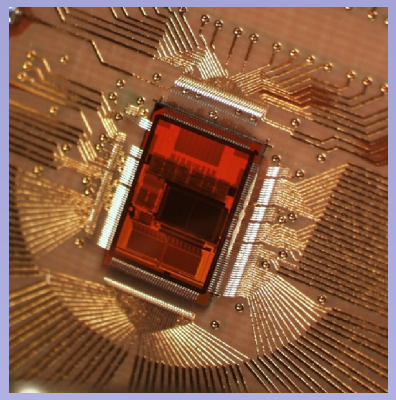




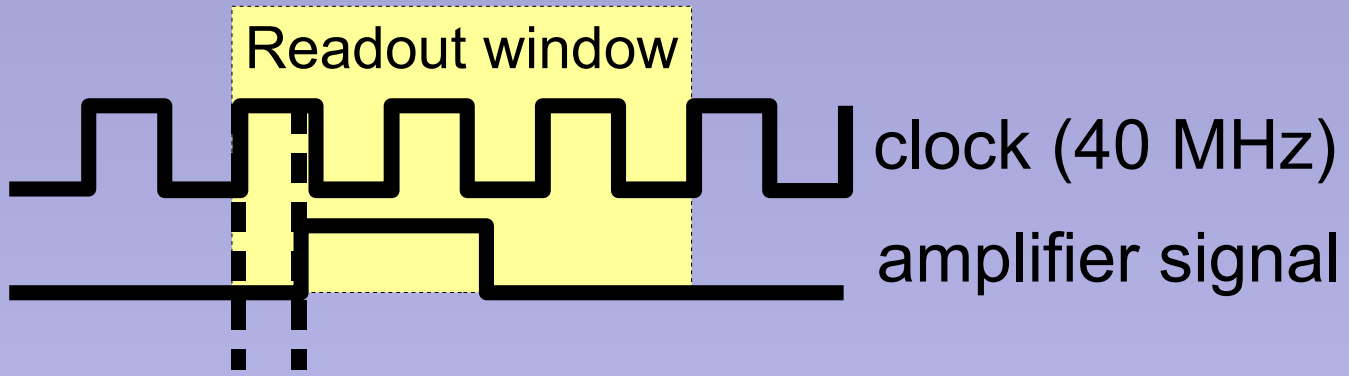
- Technology: drift tubes
- Measure: drift time
- Result: distance wire - particle



OTIS TDC

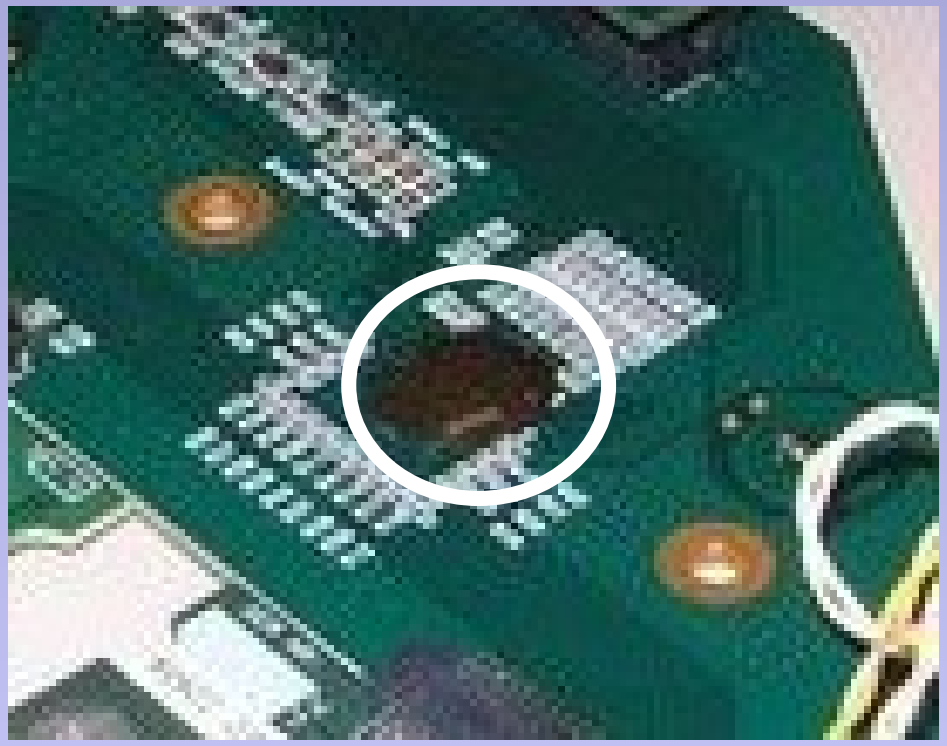


TDC = Time to Digital Converter



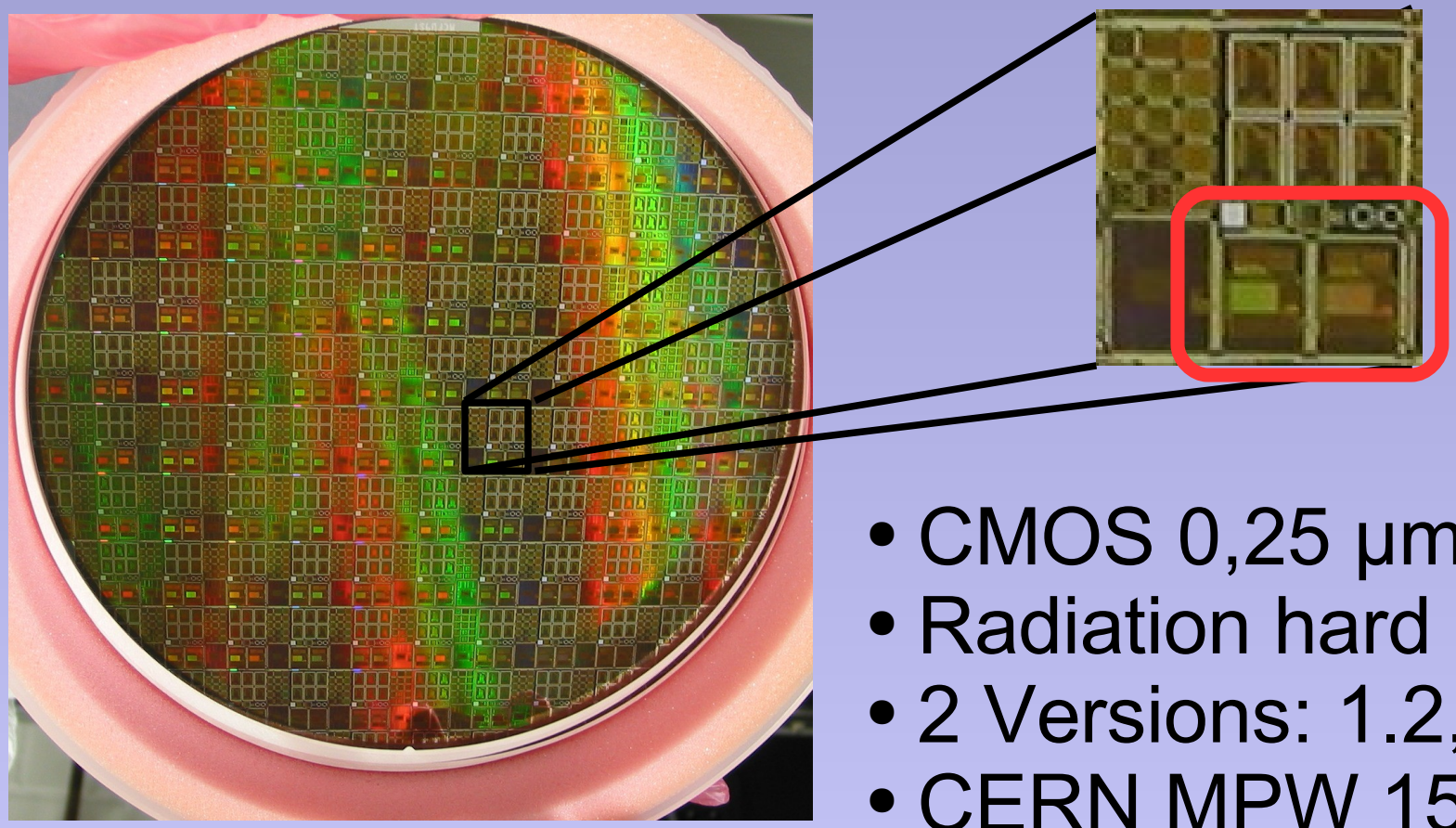
- Measures 32 channels simultaneously
- Time resolution 6 Bit (390ps @ 40 MHz)
- Readout window: 75ns
- ASIC Labor Heidelberg

OTIS TDC (II)



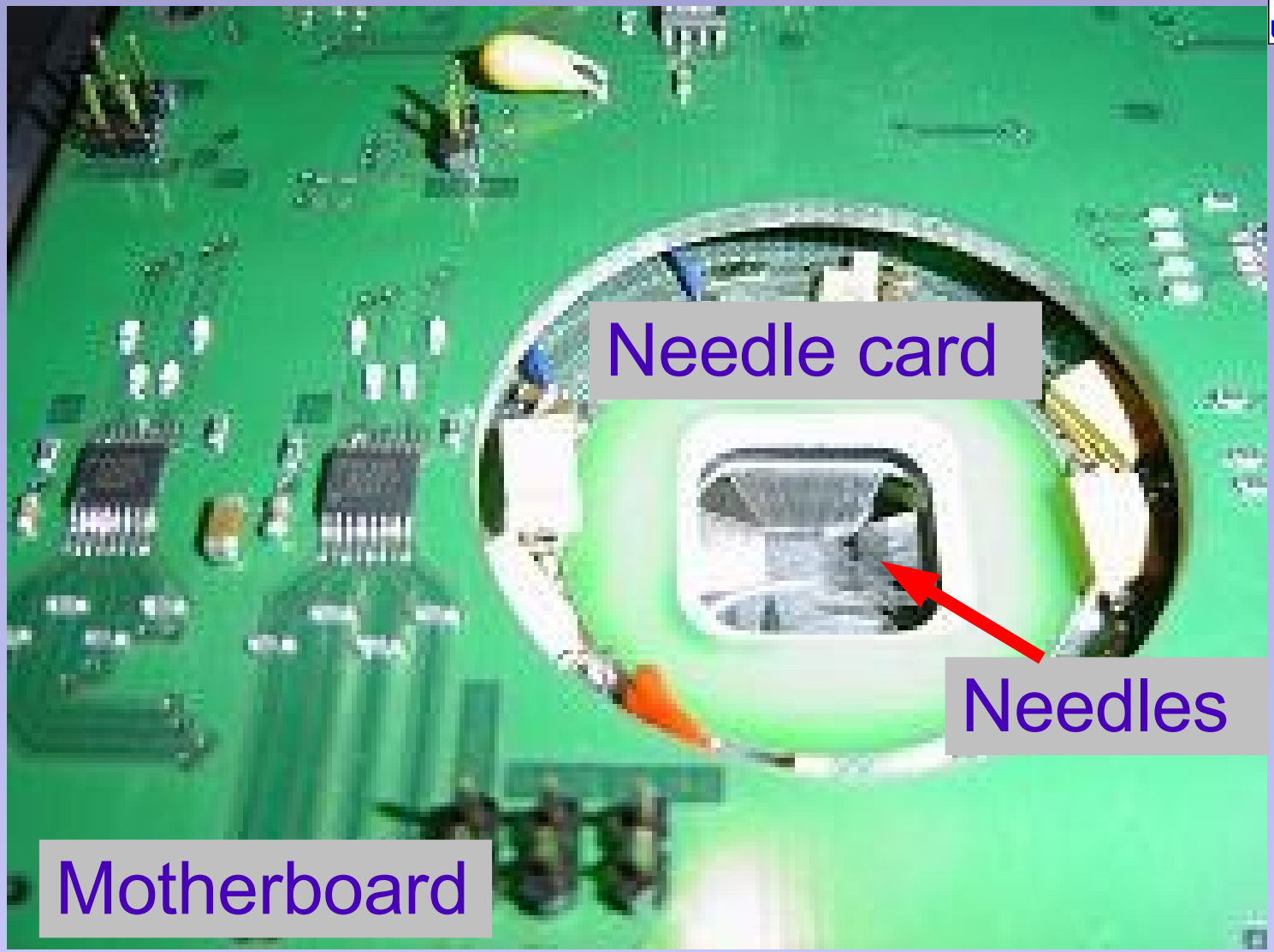
- Maximum readout rate: 1,11 MHz
- Sends data upon request (trigger)
- Data format:
  - 4 Byte Header
  - 32 Byte Data
- Slow control: I²C
- 4 analogue voltages

Wafer



- CMOS 0,25 µm Process
- Radiation hard
- 2 Versions: 1.2, 1.3
- CERN MPW 15

Needle card



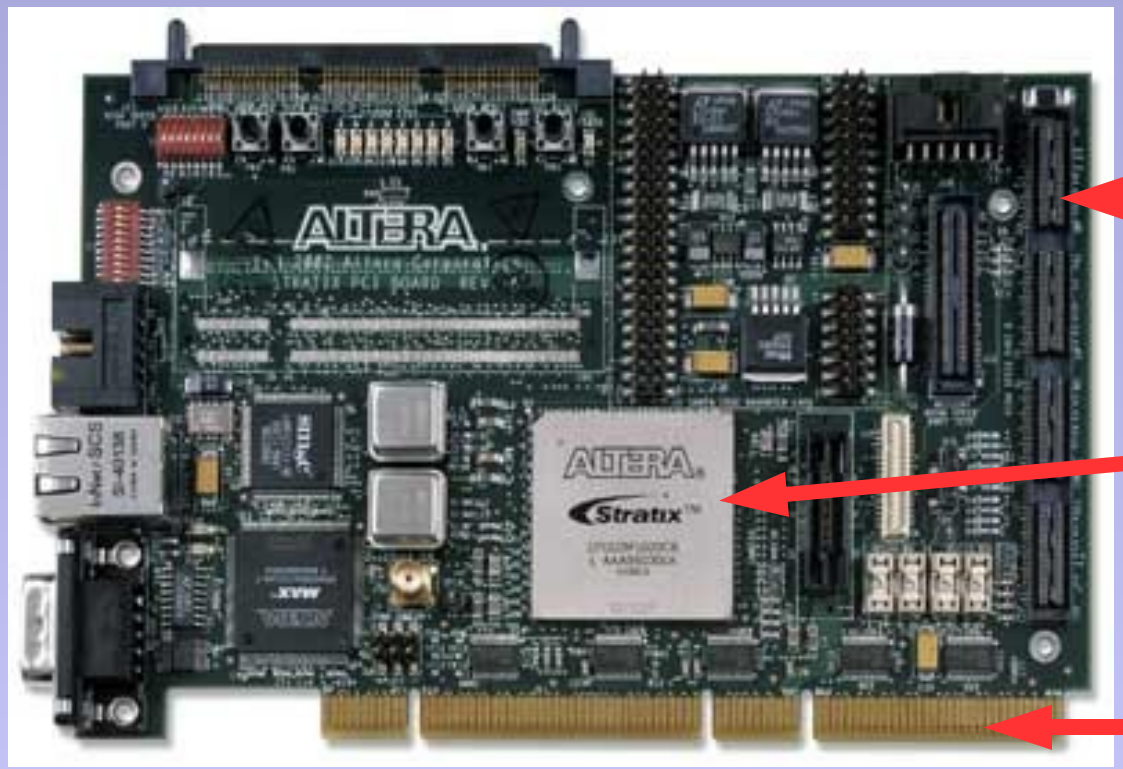
Boundary conditions

- Set all bits at least once to '0' and to '1'
- Time measurement: 10^6 data sets
- Test started: 15 November
- Test ended: 5 December
- Number of chips: 8413

=> time per Chip: ø 1 Min
=> use maximal readout rate, analyse data on a FPGA

FPGA card

Altera PCI Development Kit (Stratix Edition)

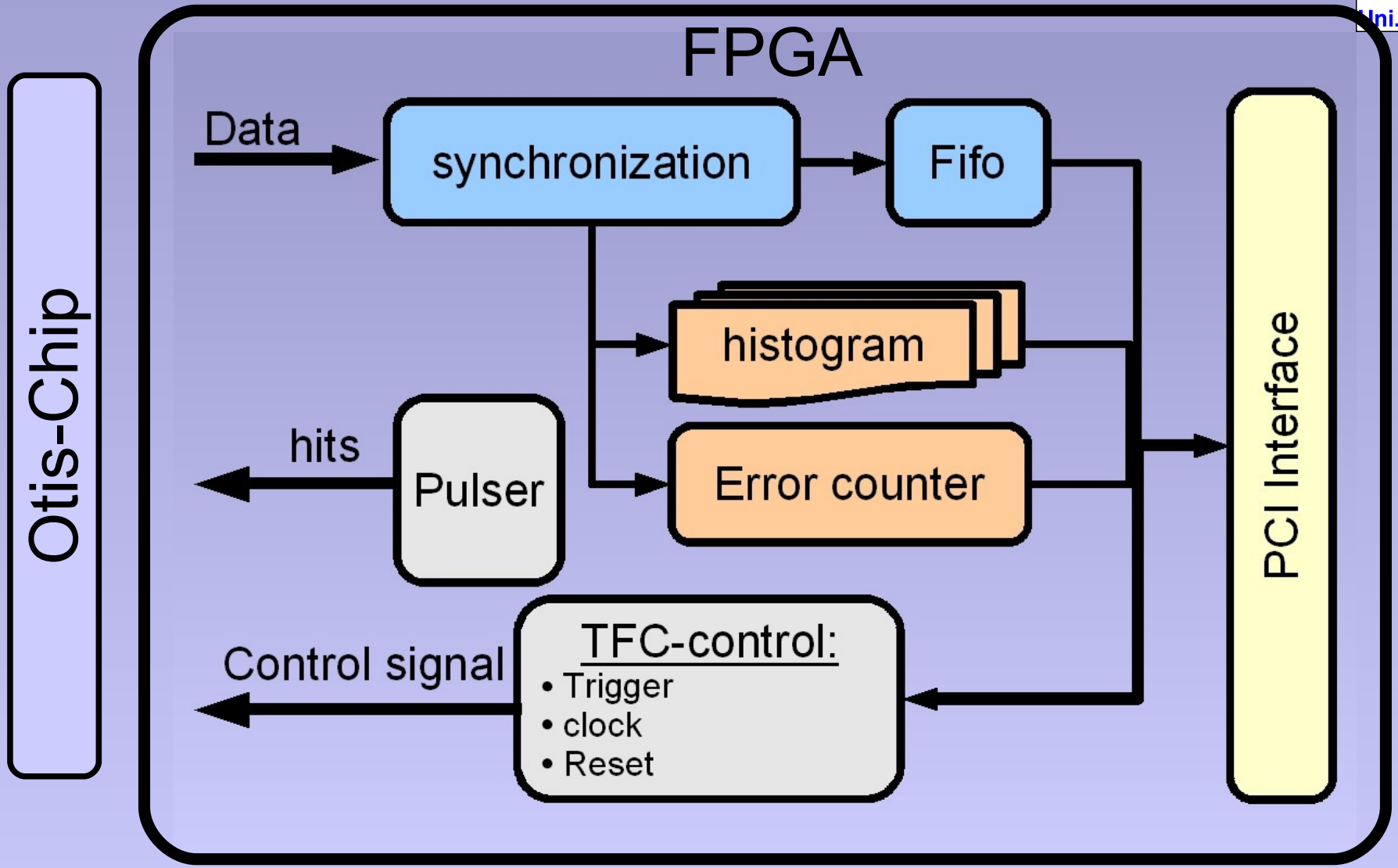


160 pin high speed connector

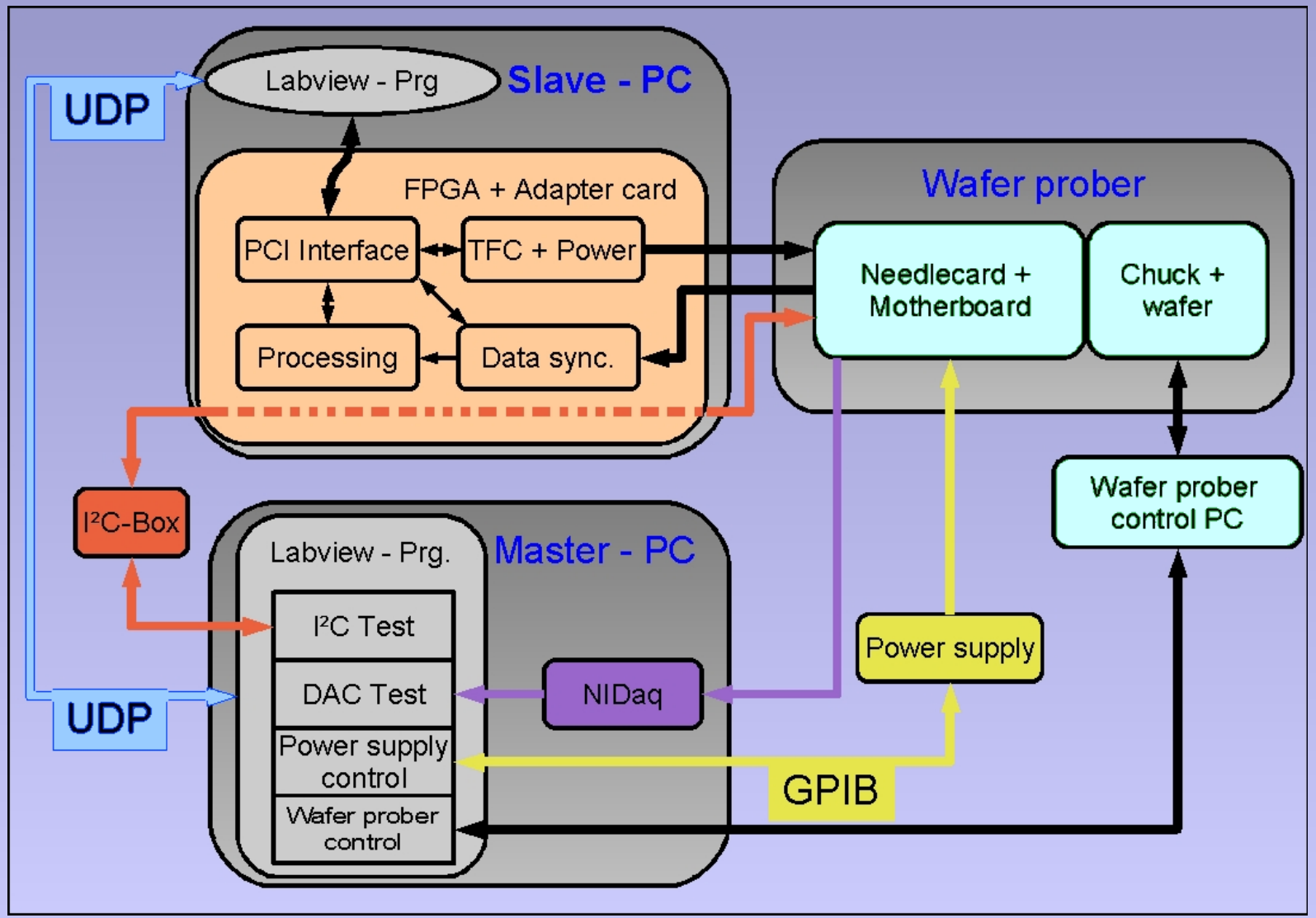
Stratix EP1S25F1020C5 (25000 LE)

PCI Bus

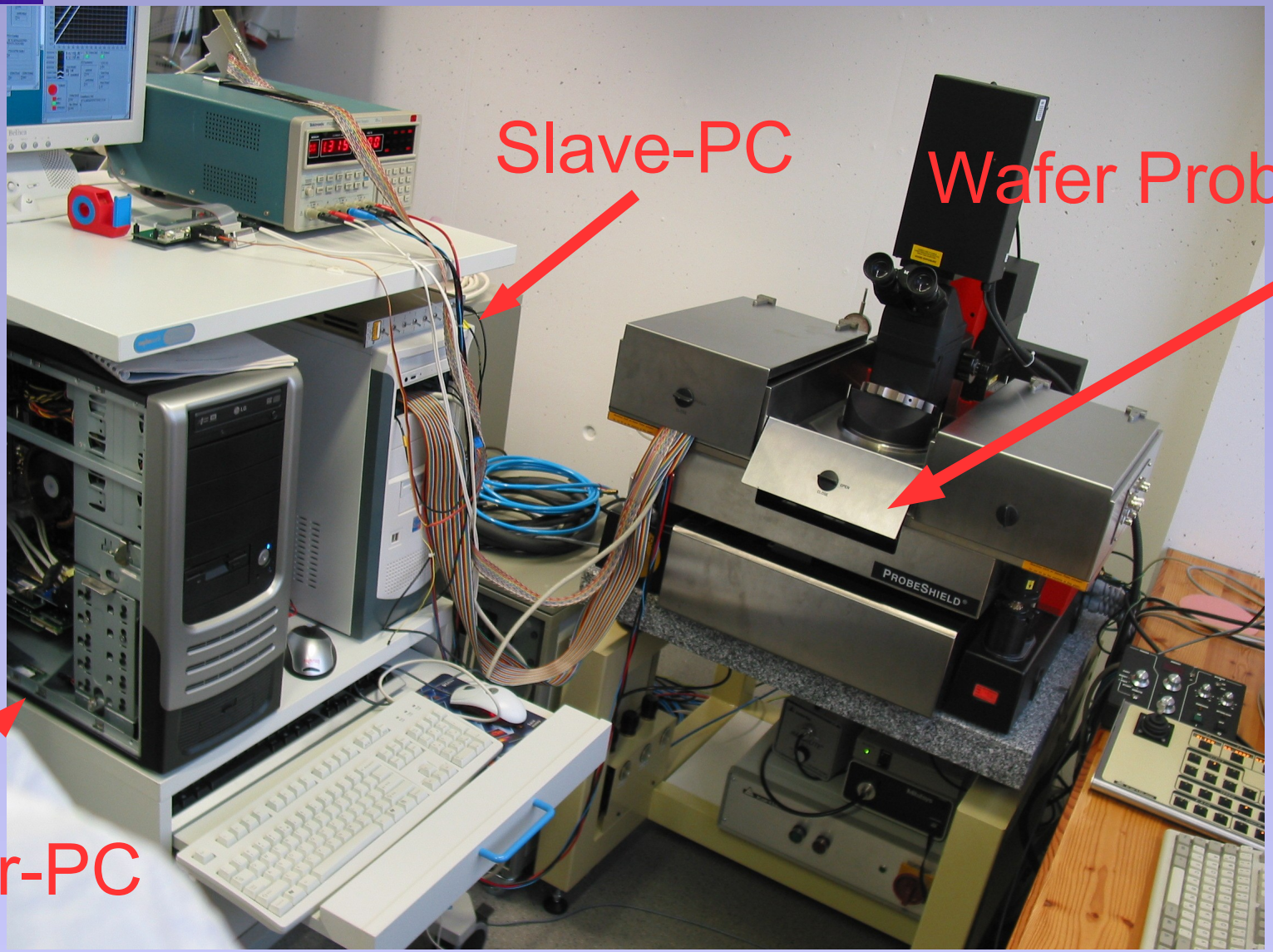
FPGA Firmware



Setup (schematic)

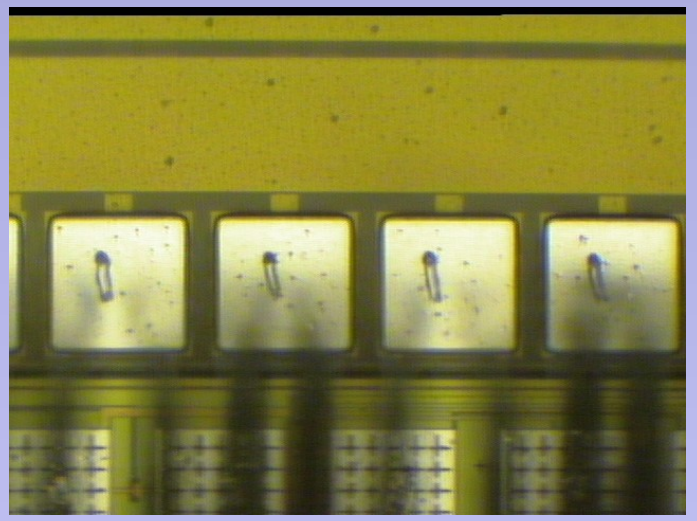


Setup



Test procedure

1) Go to next chip and attach needle card
2) Switch on power and initialize the chip
3) Measure current
4) Program register (Set I)
5) FPGA test procedure
6) Program register (Set II)
7) Measure threshold voltages



In case of failure: repeat once

FPGA Test

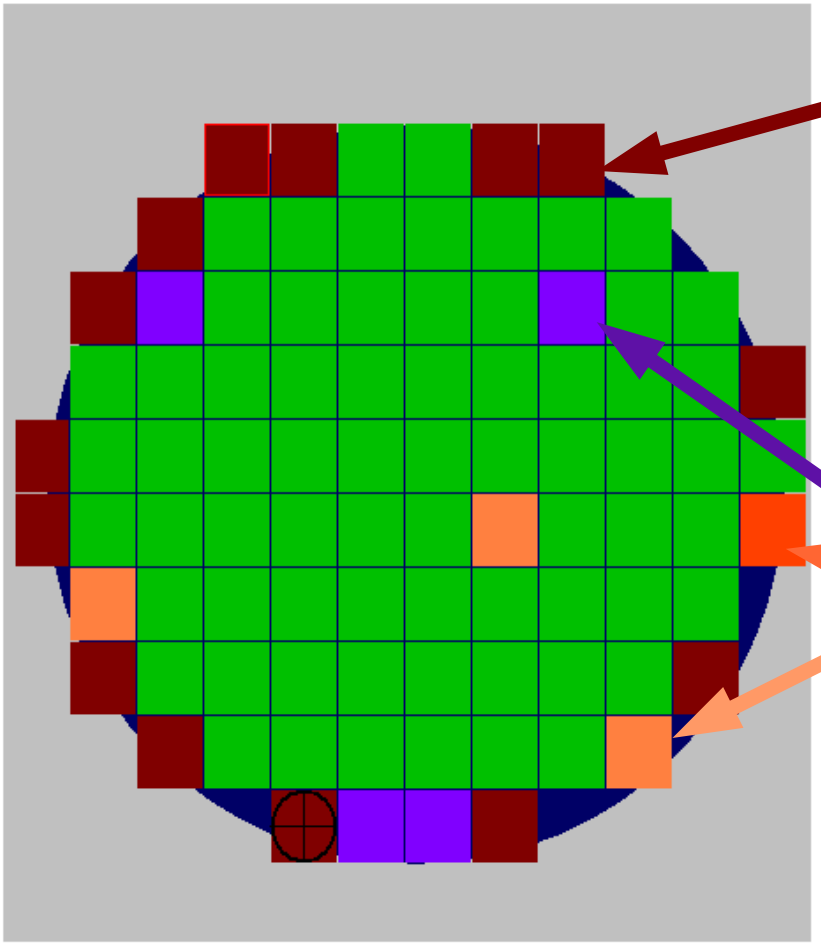
- Test procedure:
  - Test of the Header Bits with 2 different settings
  - Test of all channels
  - Time measurement on 4 channel
  - Force a buffer overflow

Data sets needed	
2x 1'000	
2x 100'000	
4x 1'000'000	
90	

Amount of data	= 144 MByte

Wafer map

Wafer MLFU9IT
OTIS 1.2
69 good chips
78 processed



Chips not processed

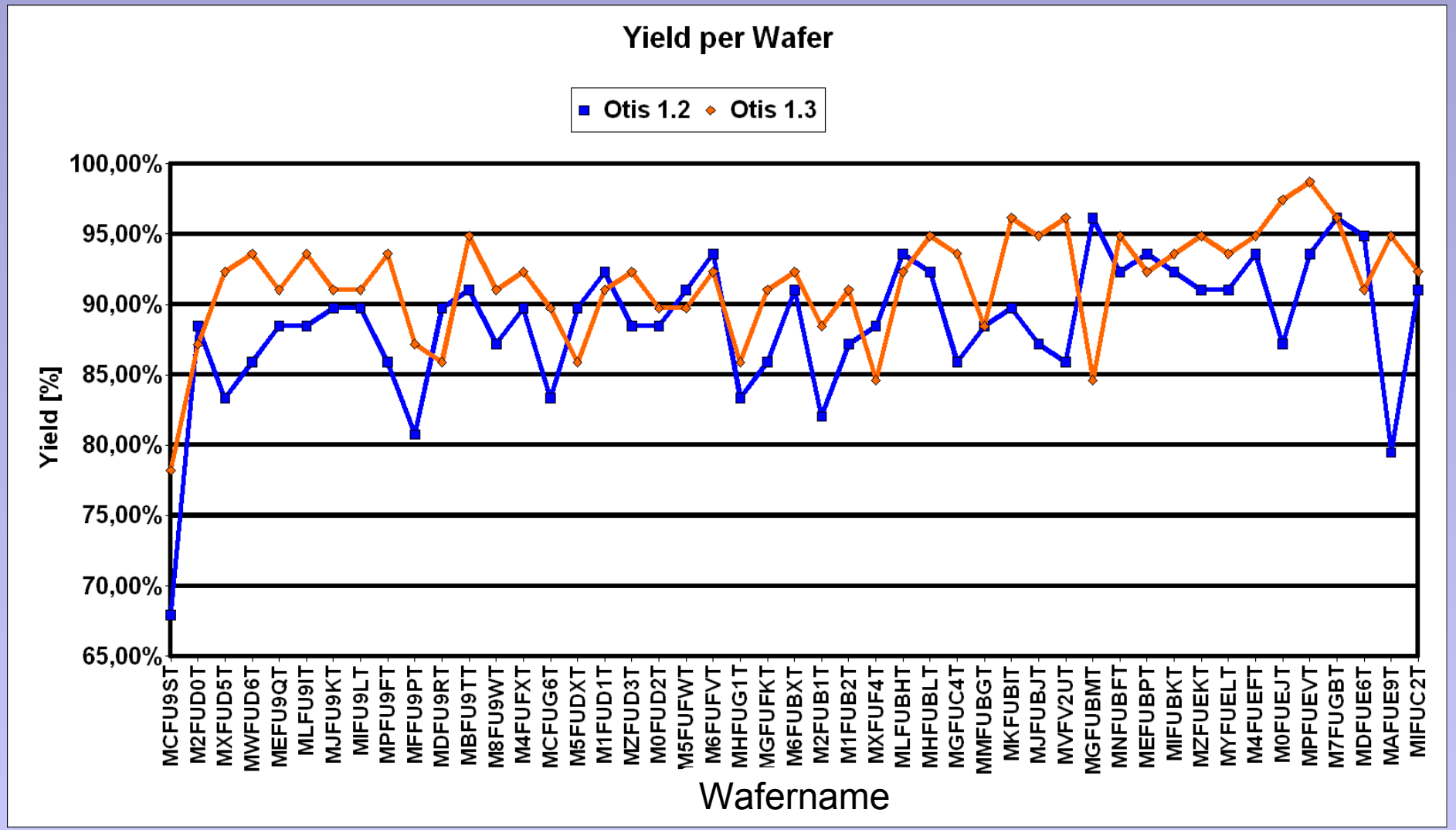
Colour code indicates the type of failure

Failure categories

	OTIS 1.2	OTIS 1.3
Time measurement	1,8%	1,9%
Threshold voltage	2,4%	0,8%
Dead channel	7,6%	4,5%
Digital errors	10,0%	7,2%
Power consumption	3,0%	1,3%

Mostly several errors at once

Yield per Wafer



Result

- Time needed to test a ...
  - ... good Chip: 25 s
  - ... bad Chip: 110 s
- Yield very high:
  - Otis 1.3: 3356 out of 3666 (≈ 92%)
  - Otis 1.2: 3250 out of 3666 (≈ 89%)
- The LHCb Outer Tracker is in need of about 2000 Chips.