IRTG Meeting

Experiment Control System of the Outer Tracker of LHCb and first results of a FPGA based TDC

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Outline

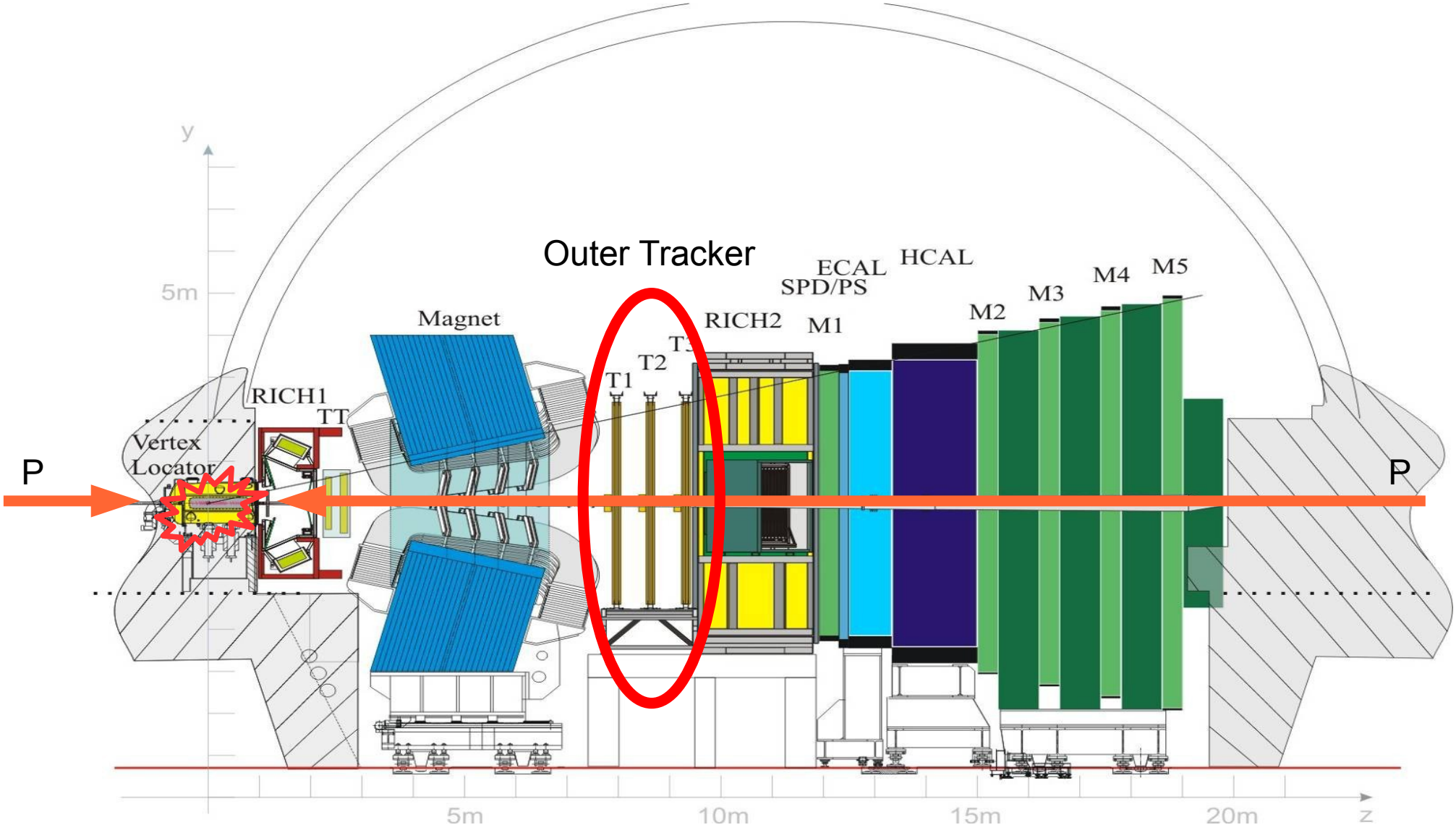
I : - Controlsystem

- Outer Tracker gas monitoring

II : - Upgrade of the Outer Tracker readout

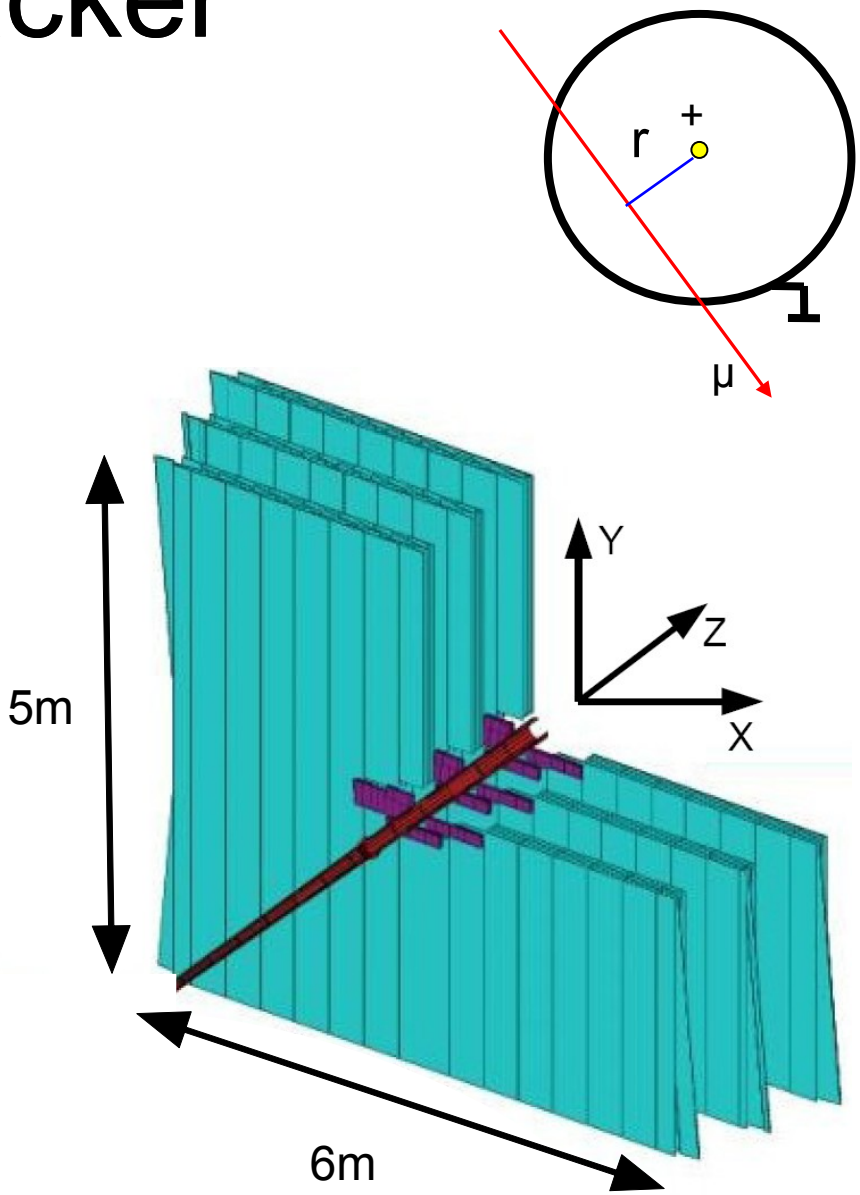
- First results of a FPGA based **T**ime to **D**igital **C**onverter (TDC)

The LHCb Detector



Outer Tracker

- Drift tube technology
- 3 stations each with 4 layers of modules
- Each module consists of 2 straw tube layers
- 53670 channels
- X coordinate resolution: 200 µm



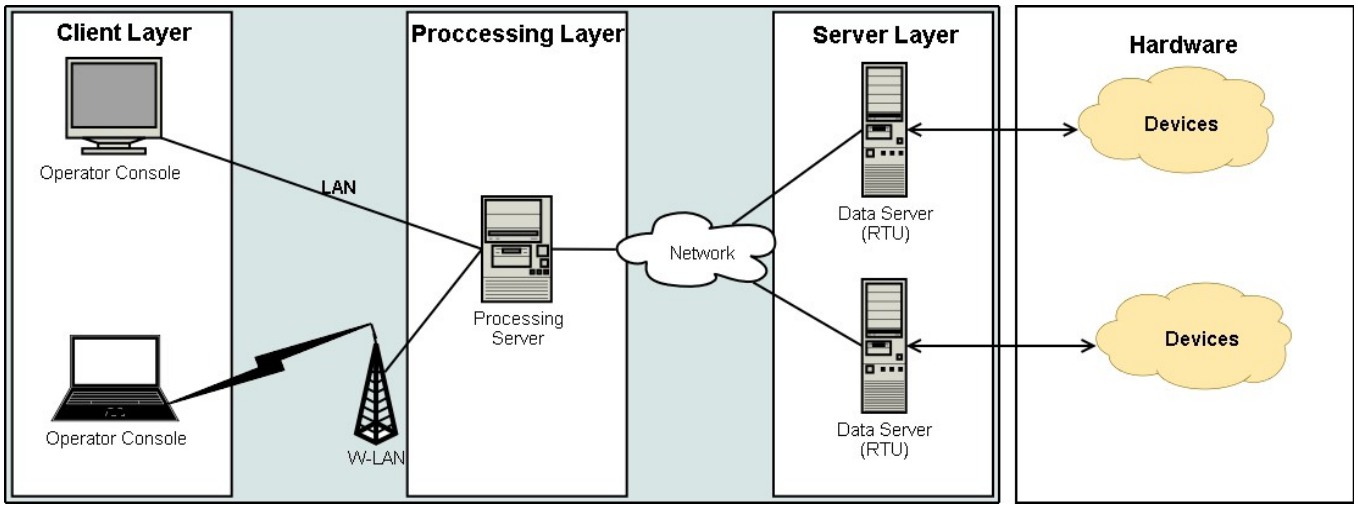
Part I

Controlsystem

- Outer Tracker gas monitoring

Controlsystem

- Supervisory Control and Data Acquisition Systems (SCADA)
  - Collecting data from hardware
  - Control over hardware
  - Works from remote
- SCADA architecture

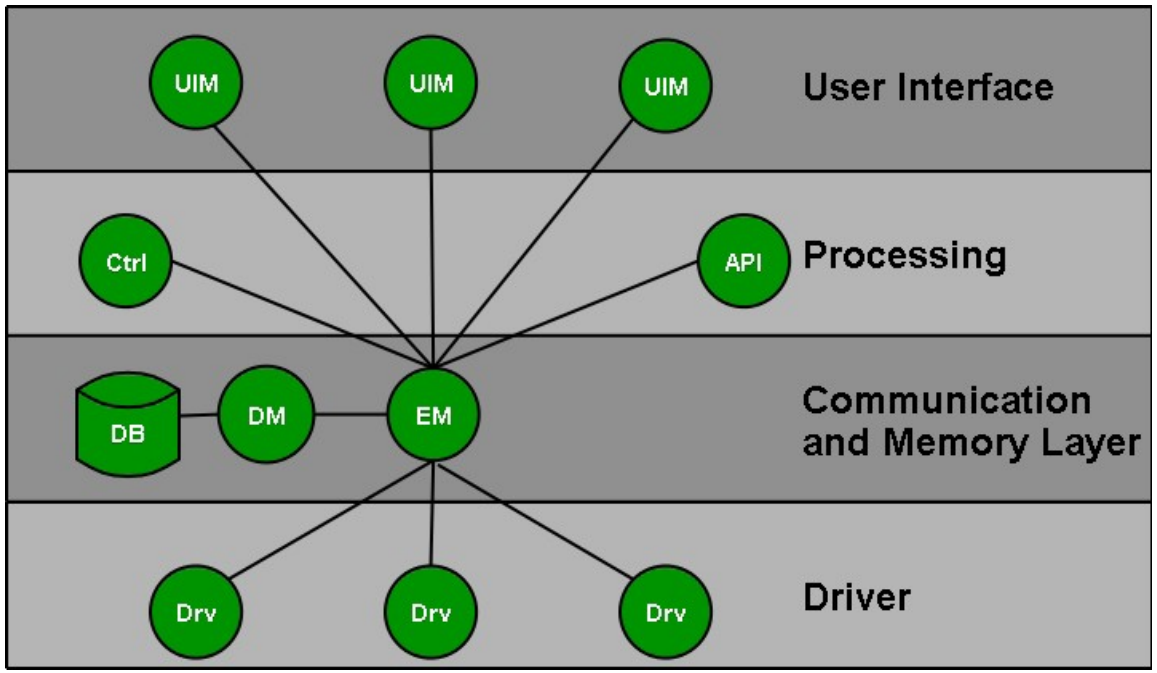


Process visualisation and control system (PVSS)

- Commercial software package chosen by CERN
- PVSS Manager Concept

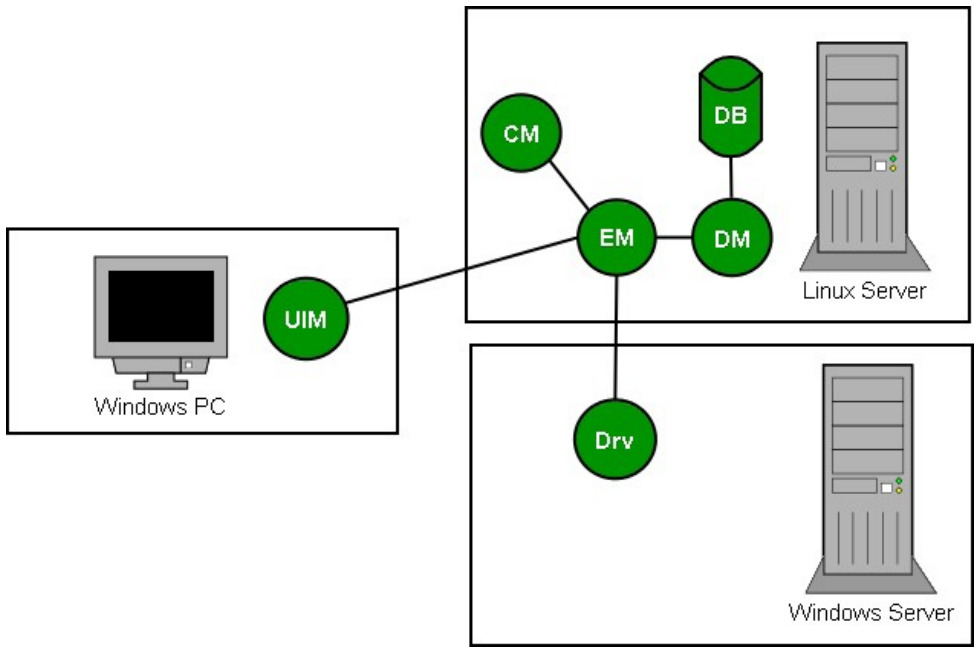
TCP/IP protocol

Event driven



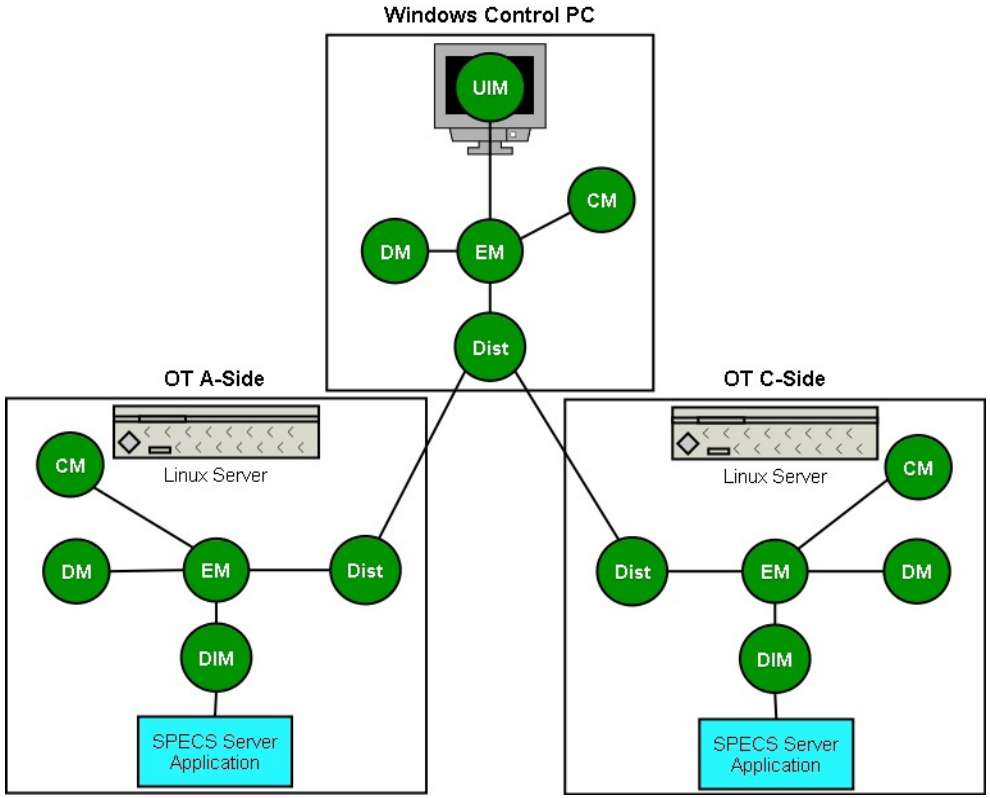
Distribution of a PVSS System

Scattered System

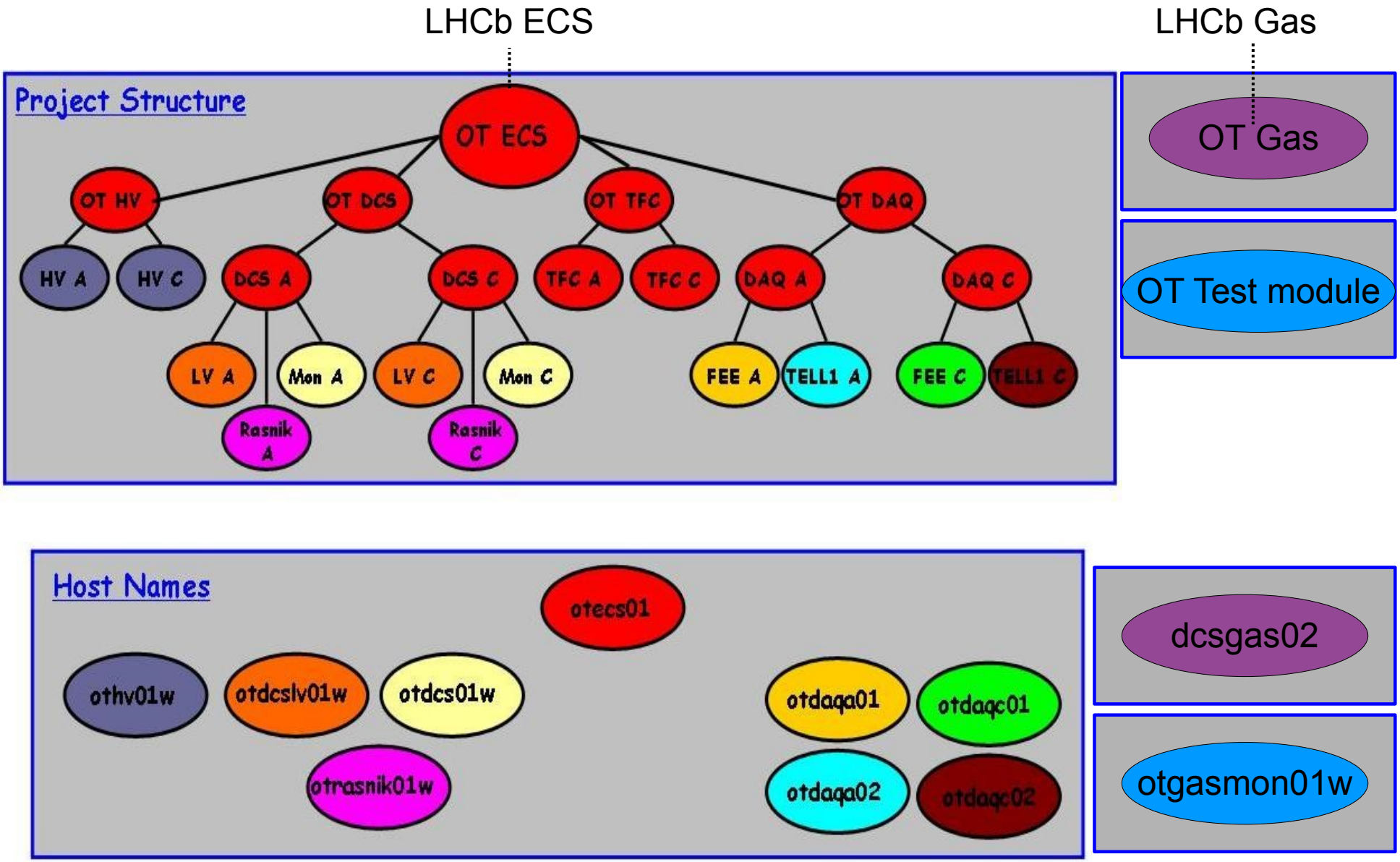


Distributed System

Outer Tracker electronics control scheme



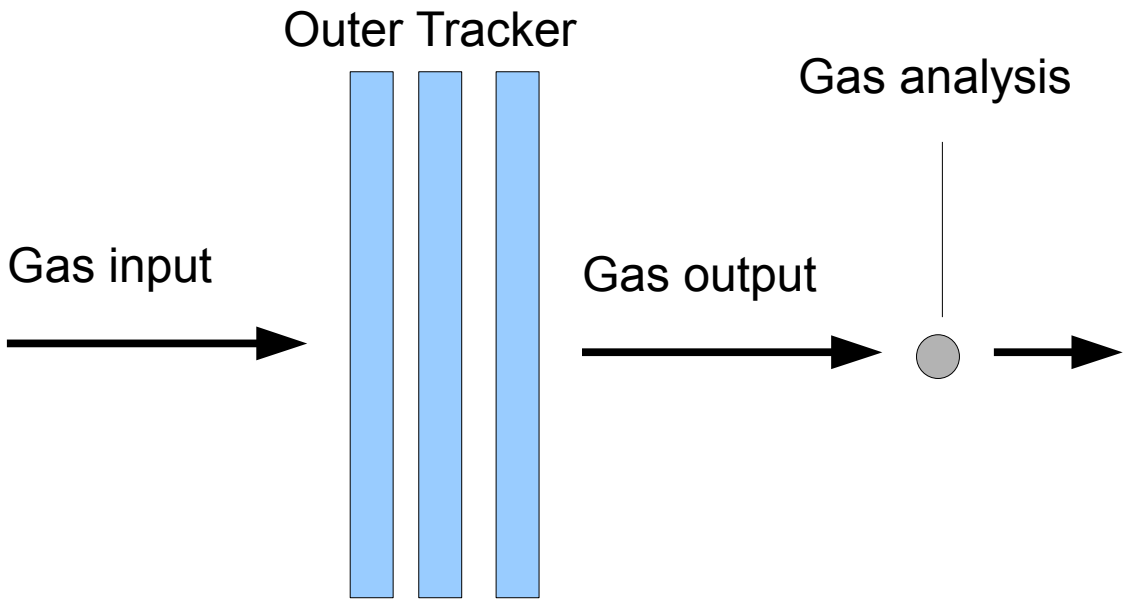
Overview: Experiment Control System



Gas Monitoring

To check

- Gasmixture
- Leaks
- Outgasing

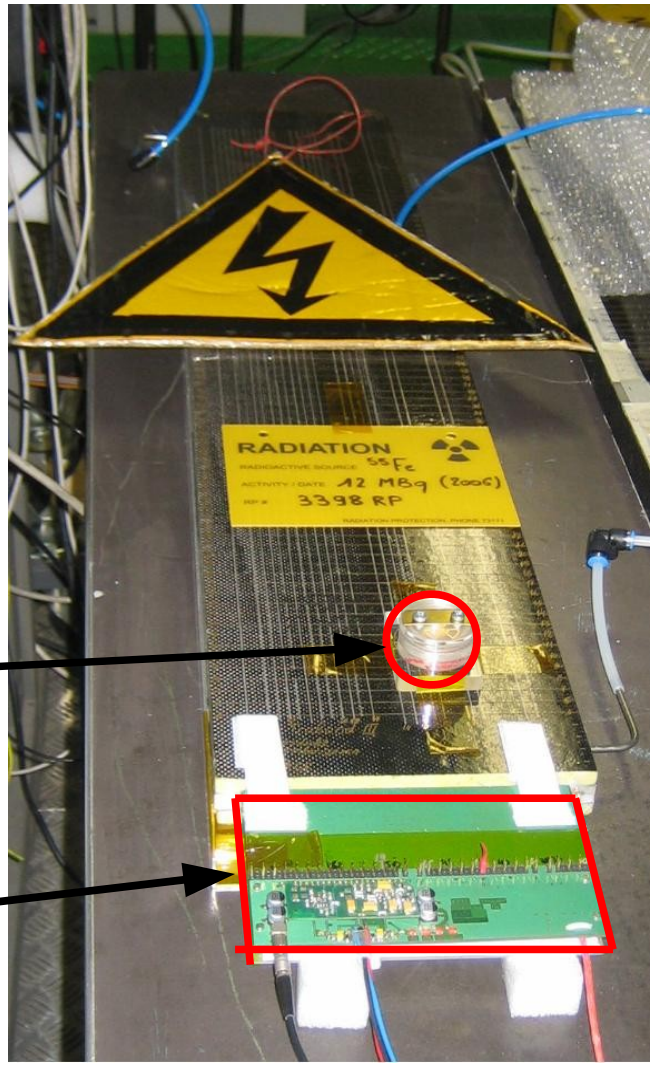


Possibilities

- Analysis rack: H_2O, O_2
- Test module ⟶ Possibility to monitor gas amplification

Test Module „TraBond“

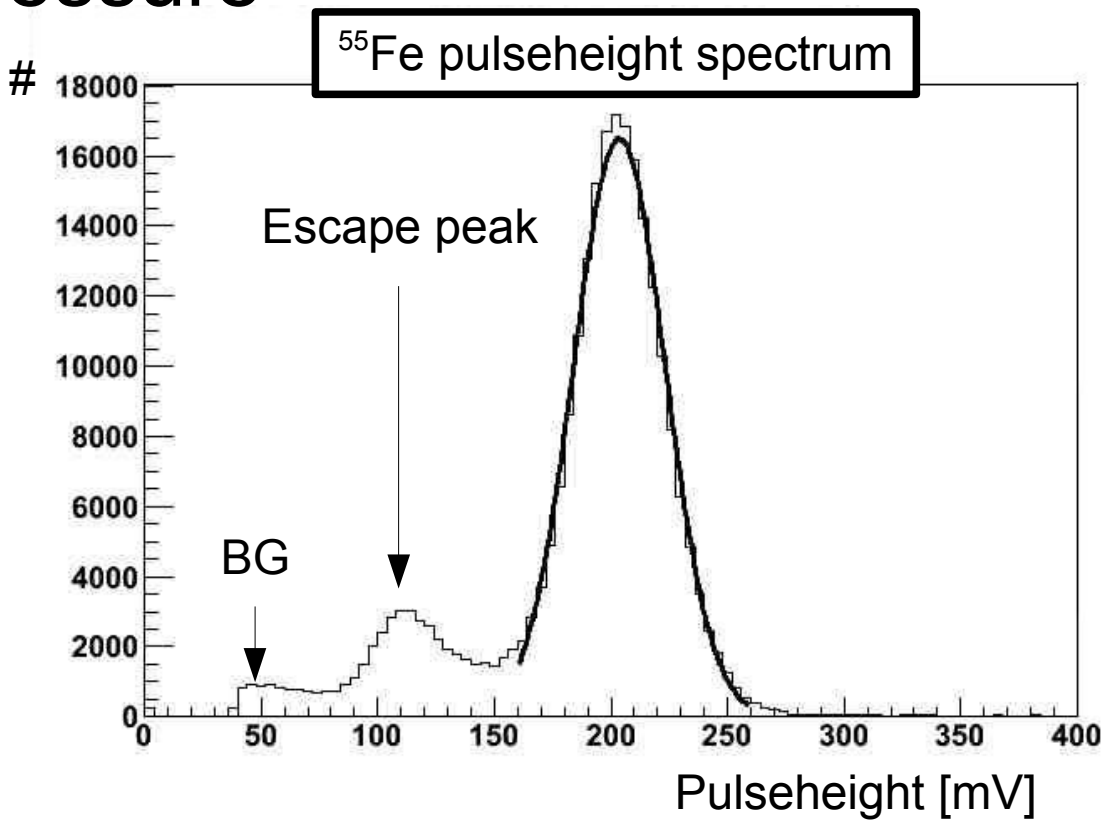
- Monitoring gas of Outer Tracker with test module
- HV = 1550V
- Irradiation with ^{55}Fe
- Preamplifier board



Measure relative Gas Amplification

- Take pulseheight spectrum with ADC
- Fit peak position
- Correction for air pressure

Gain ~ Peak position

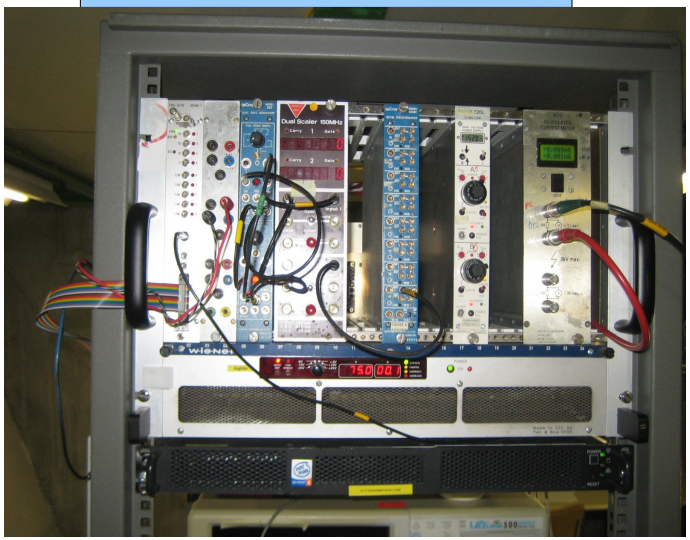


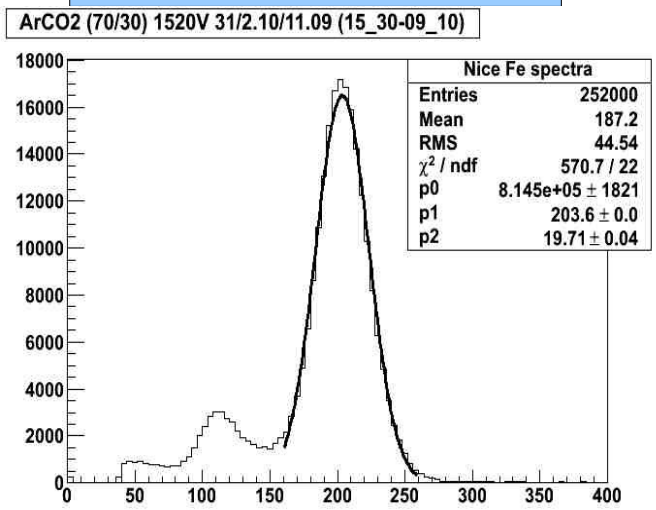
Data Flow

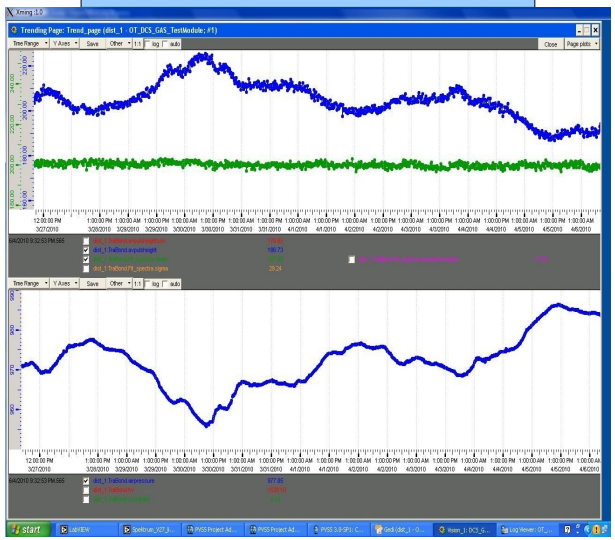
Pulseheight spectrum Measurement with ADC DAQ with LabView

Gaussian Fit ROOT

Monitoring/ Archiving PVSS

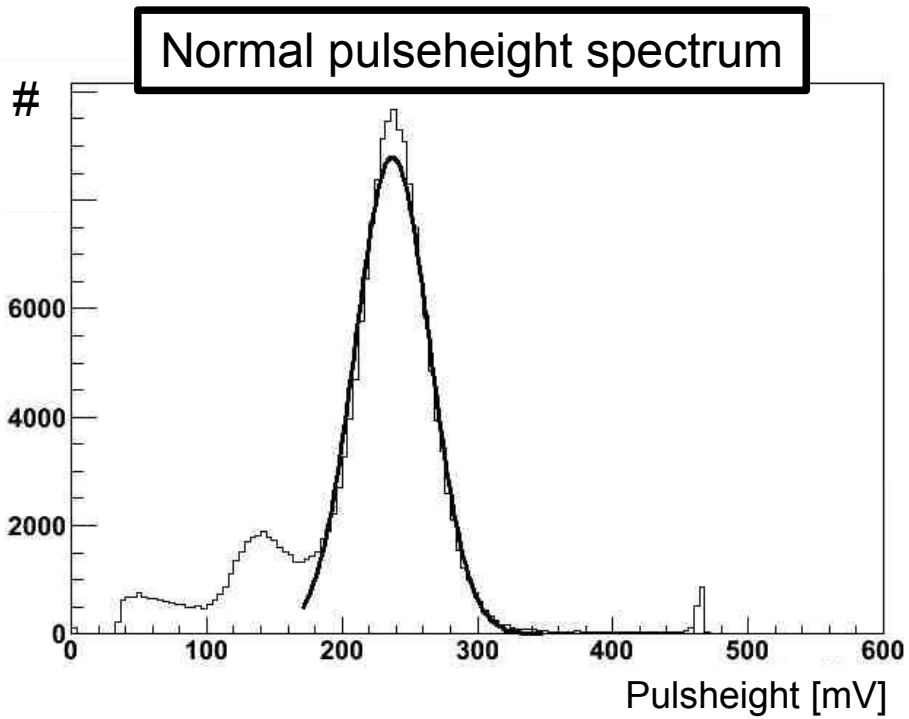


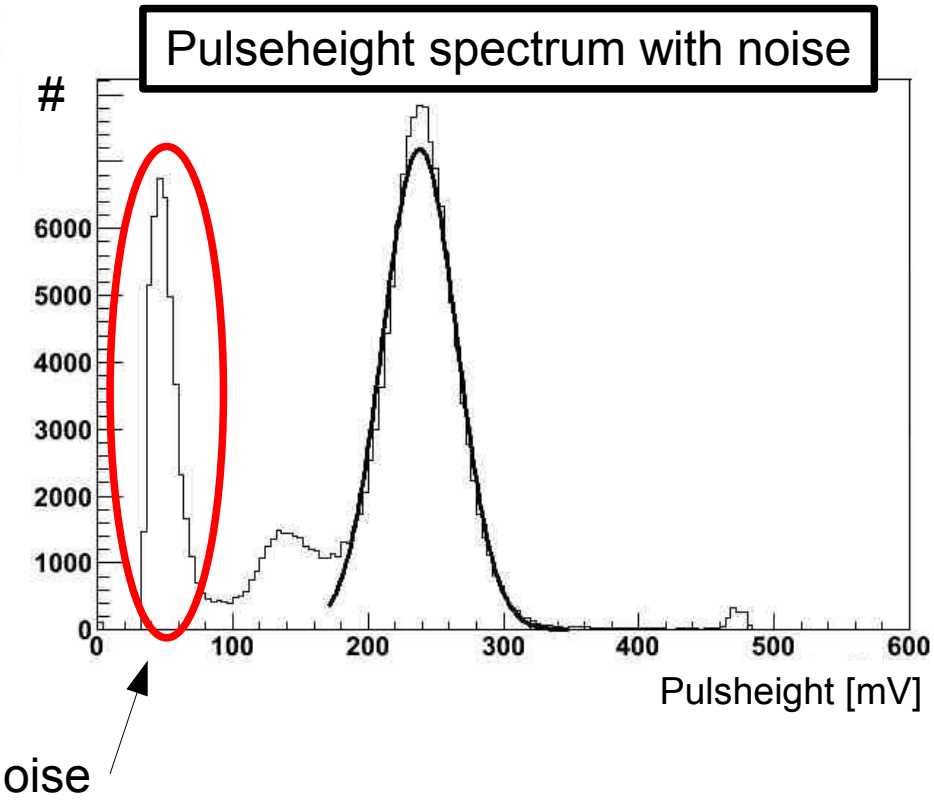




Why fitting?

- Average pulsheight only without noise ok
- Fit reduces influence of noise

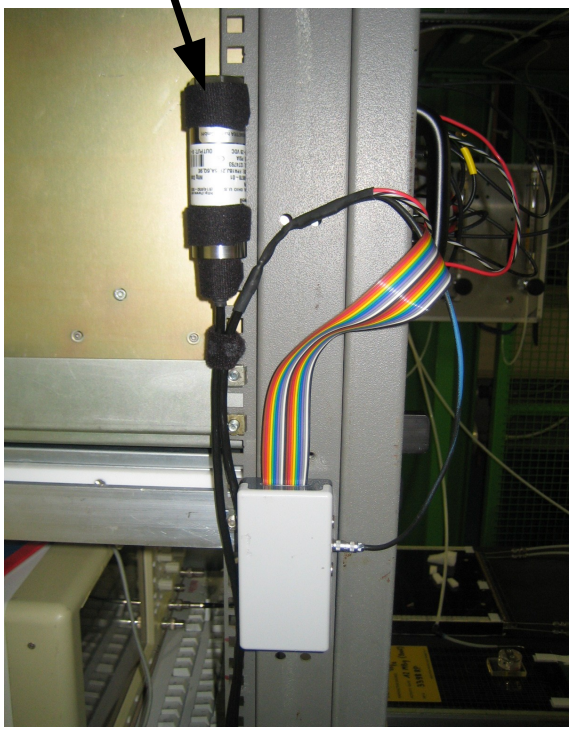


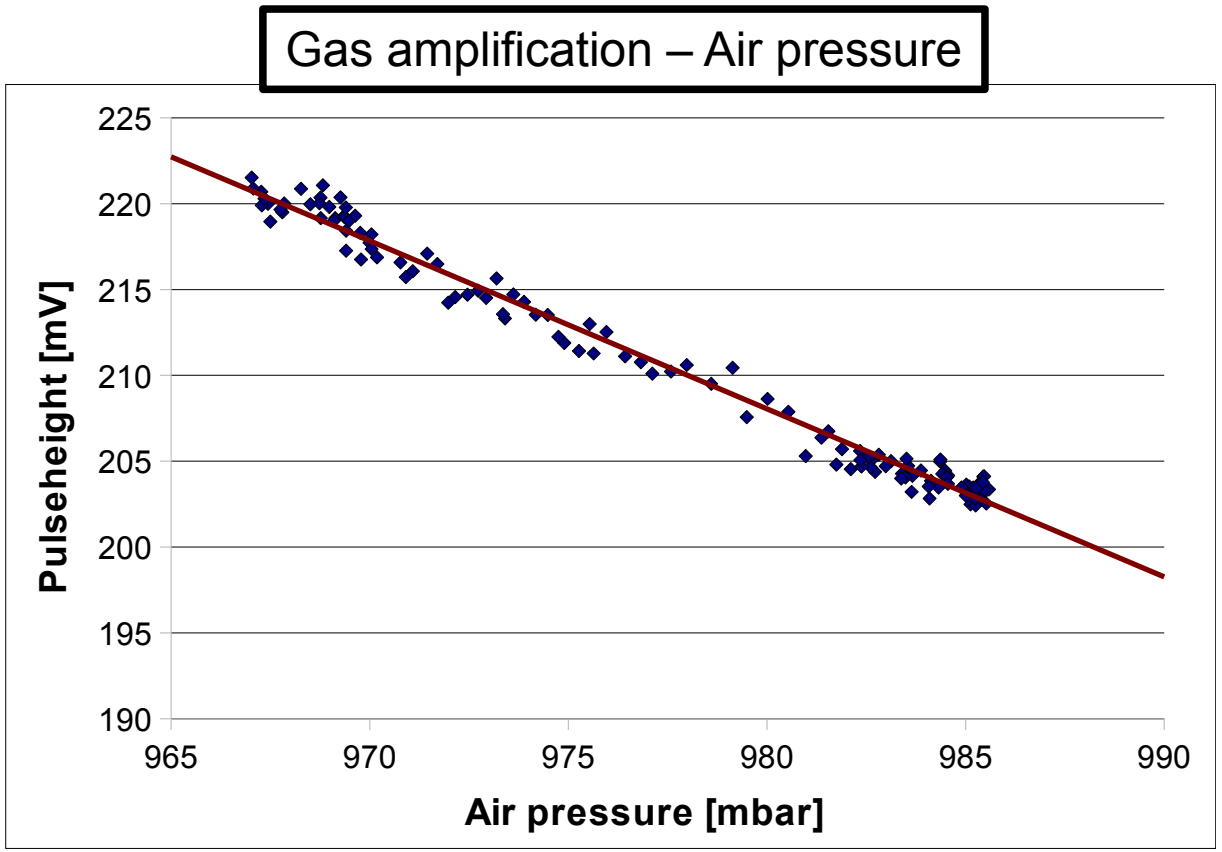


Air Pressure Correction

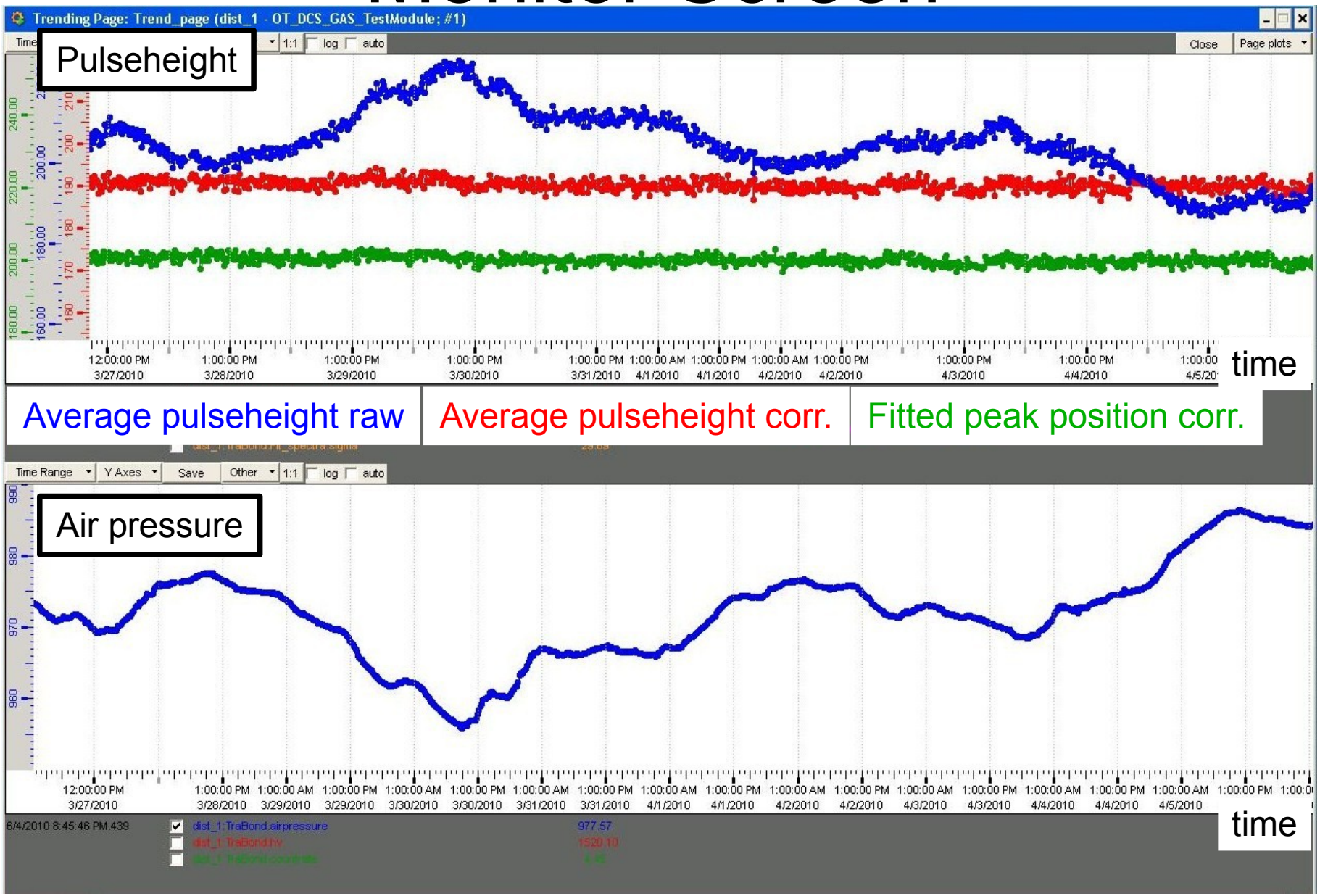
- Readout barometer for each pulse spectrum
  - More ideal: Measure counting gas pressure

Barometer





Monitor Screen



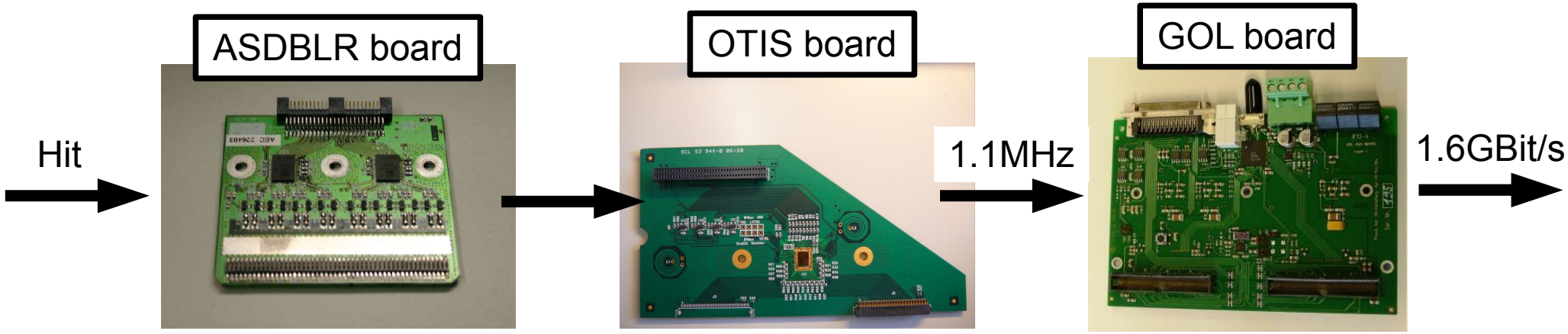
Summary Part I

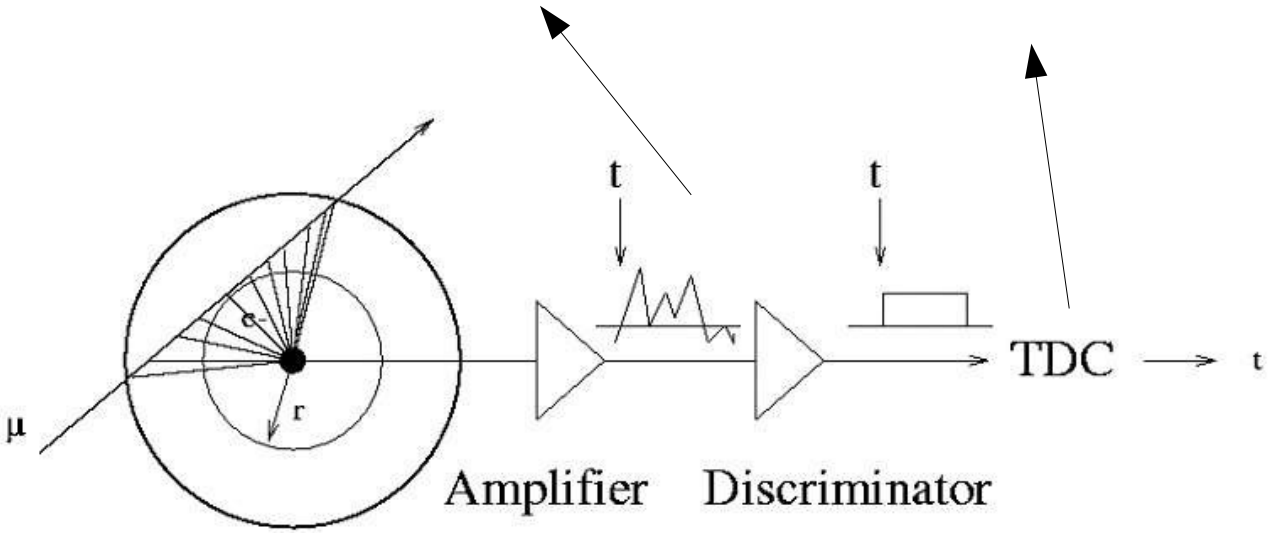
- Gas monitoring for the Outer Tracker is working well 24/7
- Alarm handling for the Front End Electronic works fine

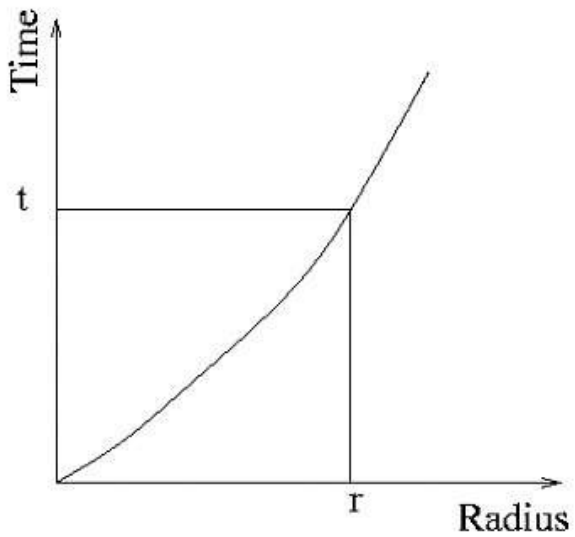
Part II

Feasibility study to use FPGA as TDC
for the 40MHz Upgrade of the
Outer Tracker readout

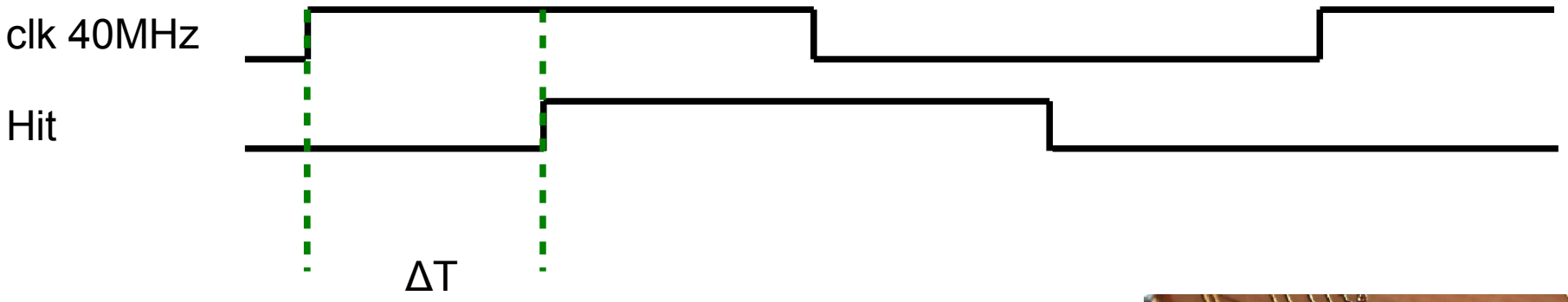
Outer Tracker Readout Today





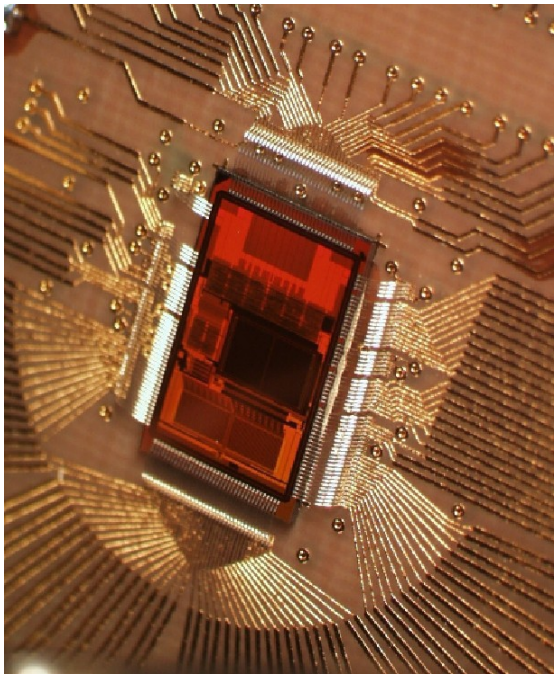


TDC „OTIS“

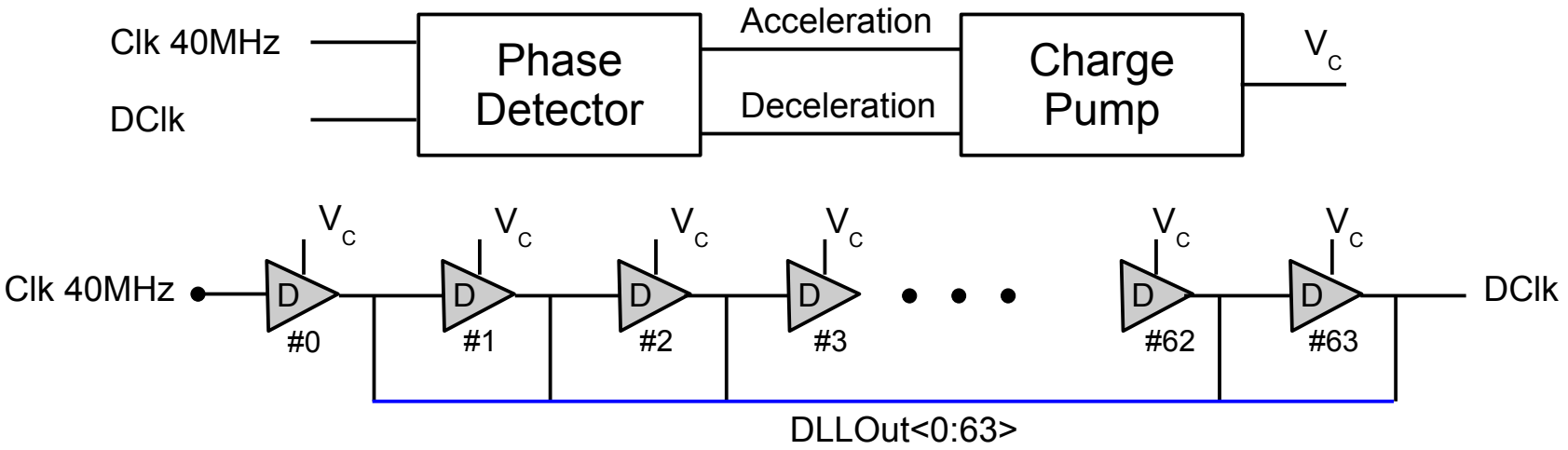


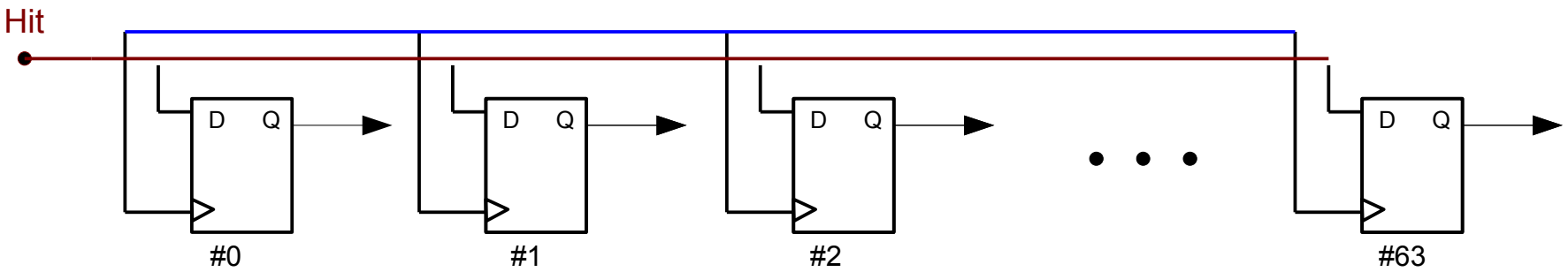
- 32 channels (simultaniously)
- Time resolution 6 Bit (390ps @ 40MHz)
- Max. readout rate 1.1MHz

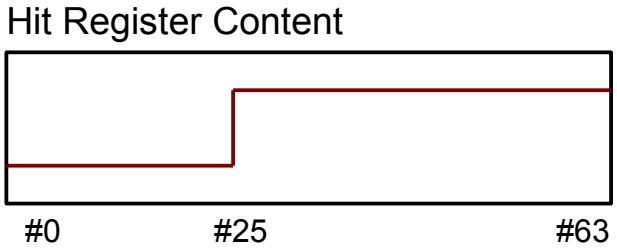
  (240bit*4*1.1MHz=1.2Gbit/s)



TDC Working Principle







Drift time extraction with 0-1 transition

LHCb 40MHz Upgrade

- Increase luminosity x10 for higher statistics
  - Current bandwidth limitation results in drop of trigger efficiency
  - Want to improve trigger efficiency for rare hadronic modes
- To increase trigger eff. with higher luminosity
  - No L0 trigger, only HLT (flexible)
  - Readout each subdetector with 40MHz (Bandwidth OT ≈ 10 TBit/s)

Consequence for the Outer Tracker Front End Electronic

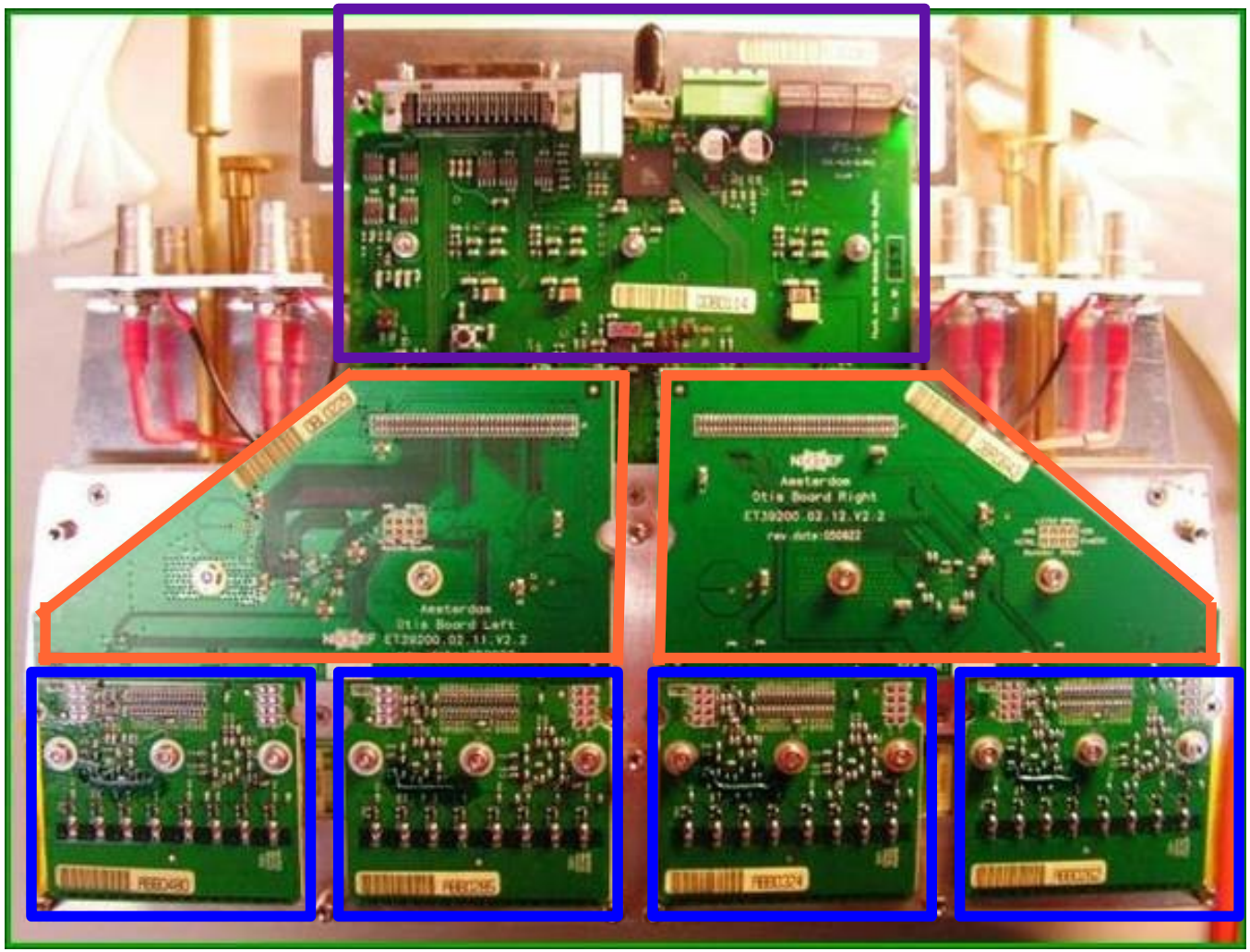
	Today	After upgrade
Readout	1.1MHz	40MHz
TDC bits	6bit	4bit – 6bit ?
Bandwidth/FE Box (128 Channels)	1.6GBit/s	20 – 30 Gbit/s ?

Outer Tracker Front End Electronic

GOL board
Max data rate
1.6GBit/s
Needs upgrade

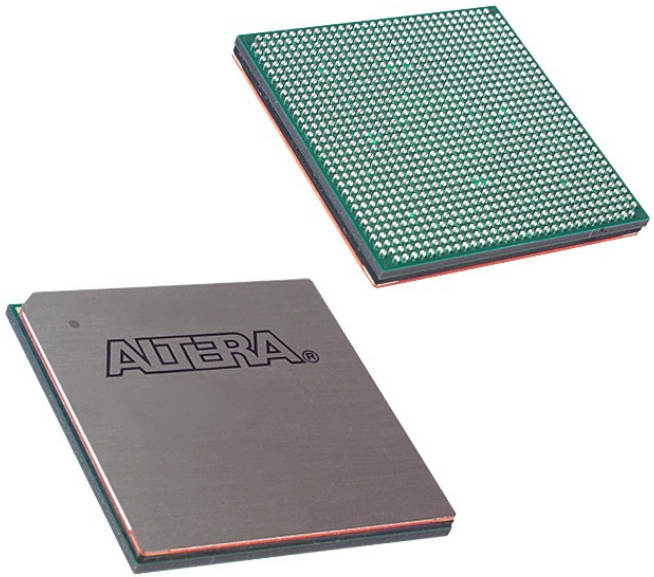
OTIS board
Max readout
1.1MHz
Needs upgrade

Preamplifier
Discriminator
ASDBLR



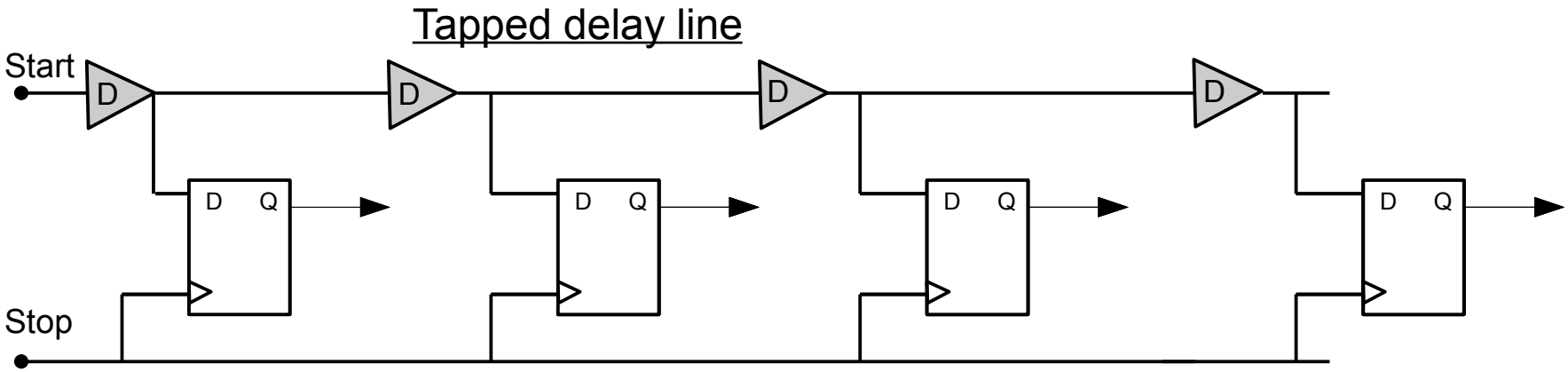
Prototype for future TDC

- Using a FPGA
  - Very flexible good for development
  - Test of 4 or 5 bit TDC
  - GBit transceiver
  - Fast realisation for test
- If necessary: convert the FPGA design into Asic



Time Measurement with FPGA

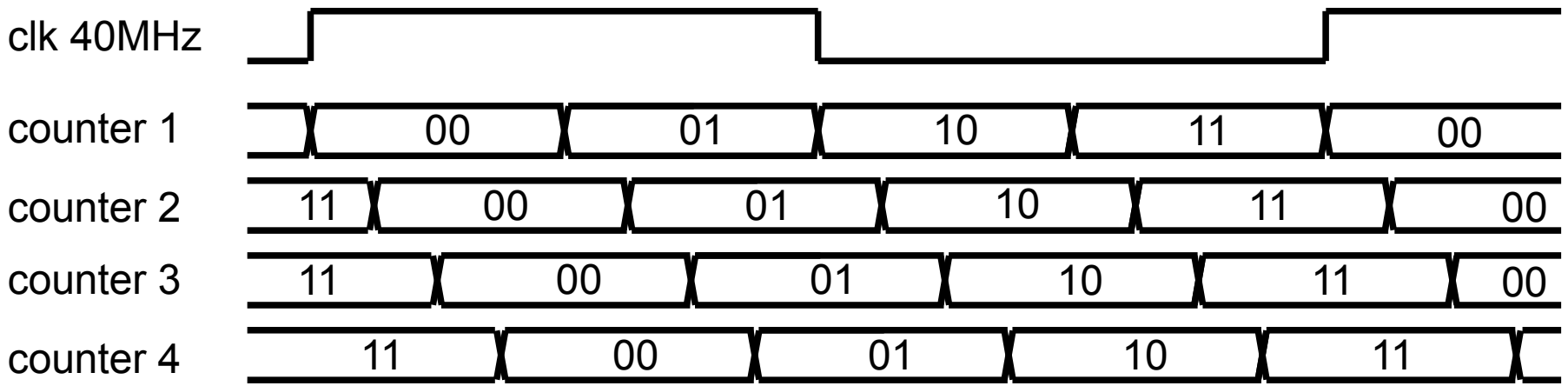
- Using delay lines
  - Calibration
  - Time resolution of < 100ps achievable



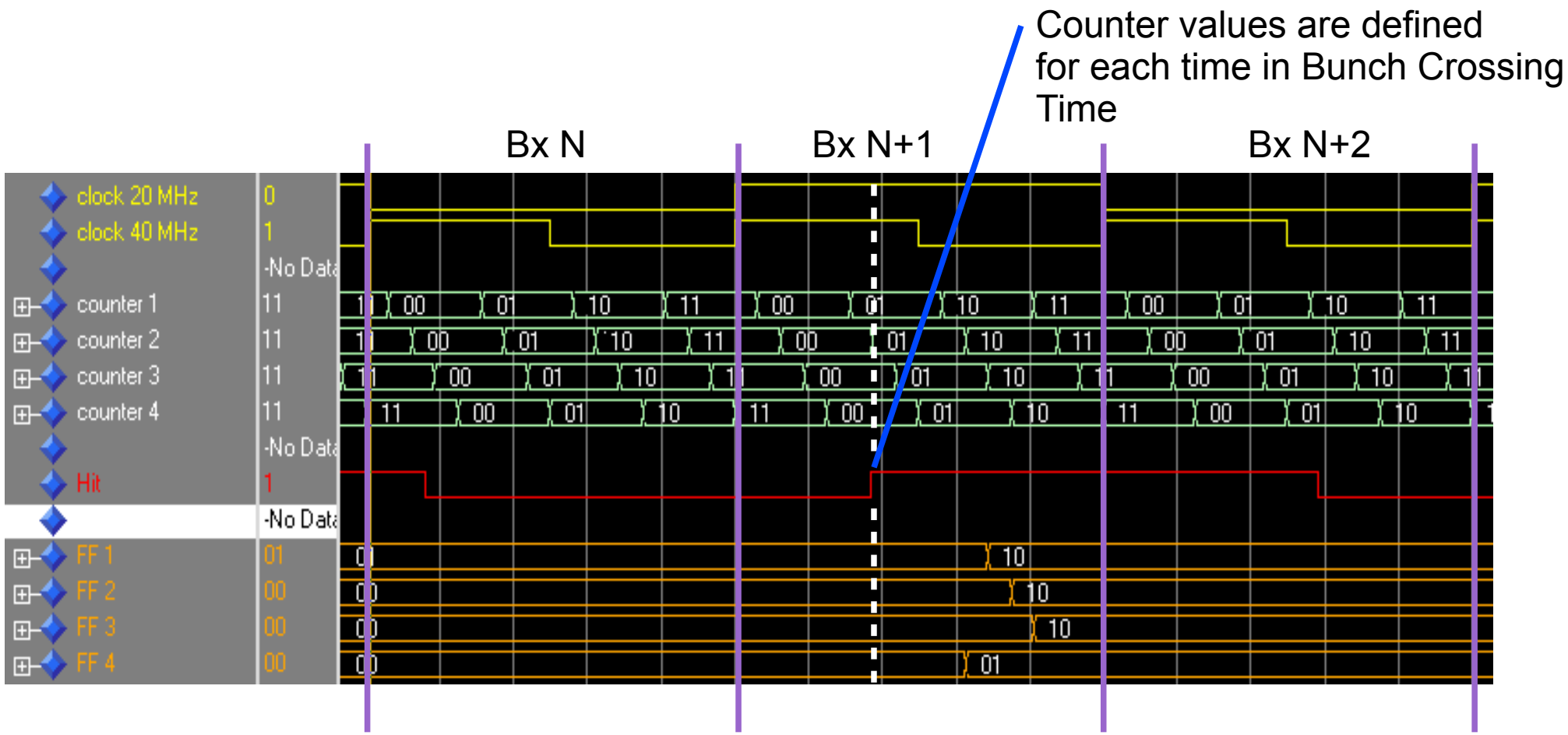
- Phase shifted counter
  - Time resolution of 1ns achievable
  - Easy to implement

Realisation: Phase Shifted Counter

- Use 4 synchronously running 2bit counters to divide Bx
  - Phase shift 90°, 4x system freq. ⟹ 16 bins
- Latching counter values for each hit
  - Encode time from counter values



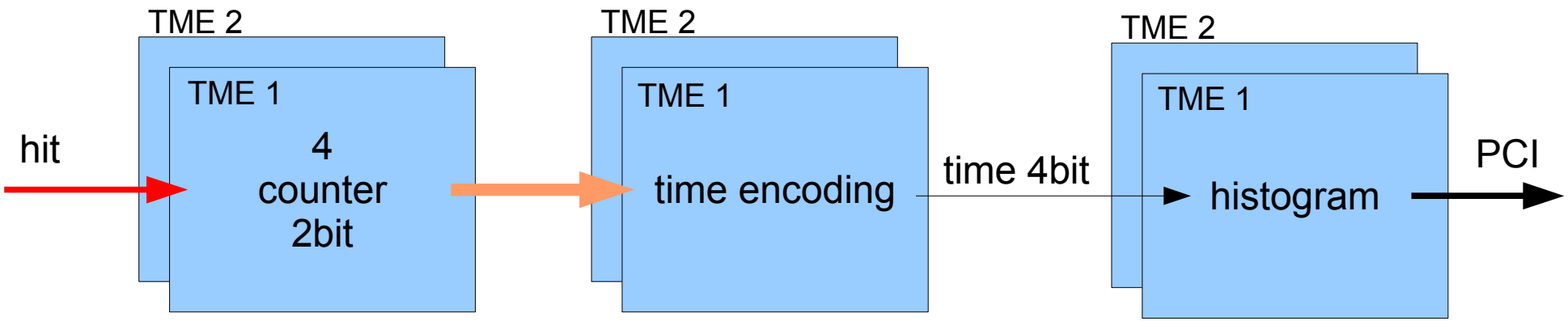
Timing Diagram



Block Diagram

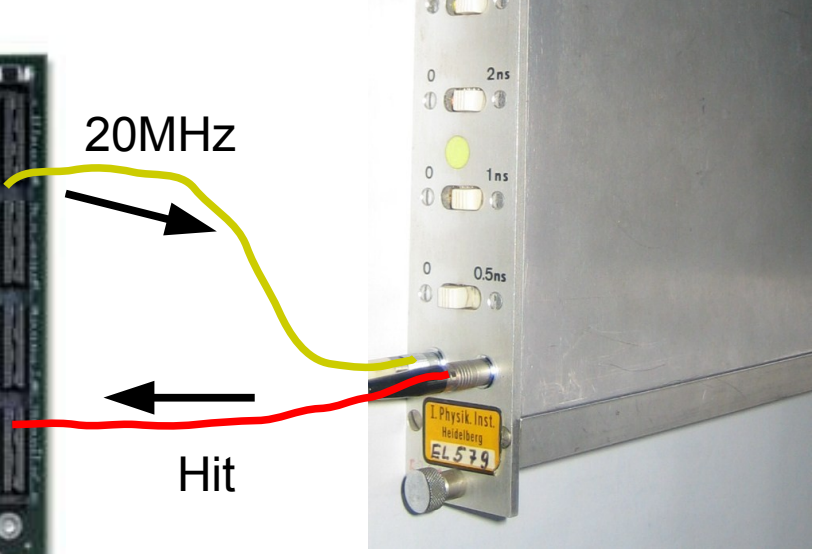
- 2 time measurement elements to avoid deadtime „during encoding“
  - One for even Bx one for odd Bx

	Bx N	Bx N+1	Bx N+2	Bx N+3	...
TME 1	**measuring**	**encoding**	**measuring**	**encoding**	**...**
TME 2	**encoding**	**measuring**	**encoding**	**measuring**	**...**

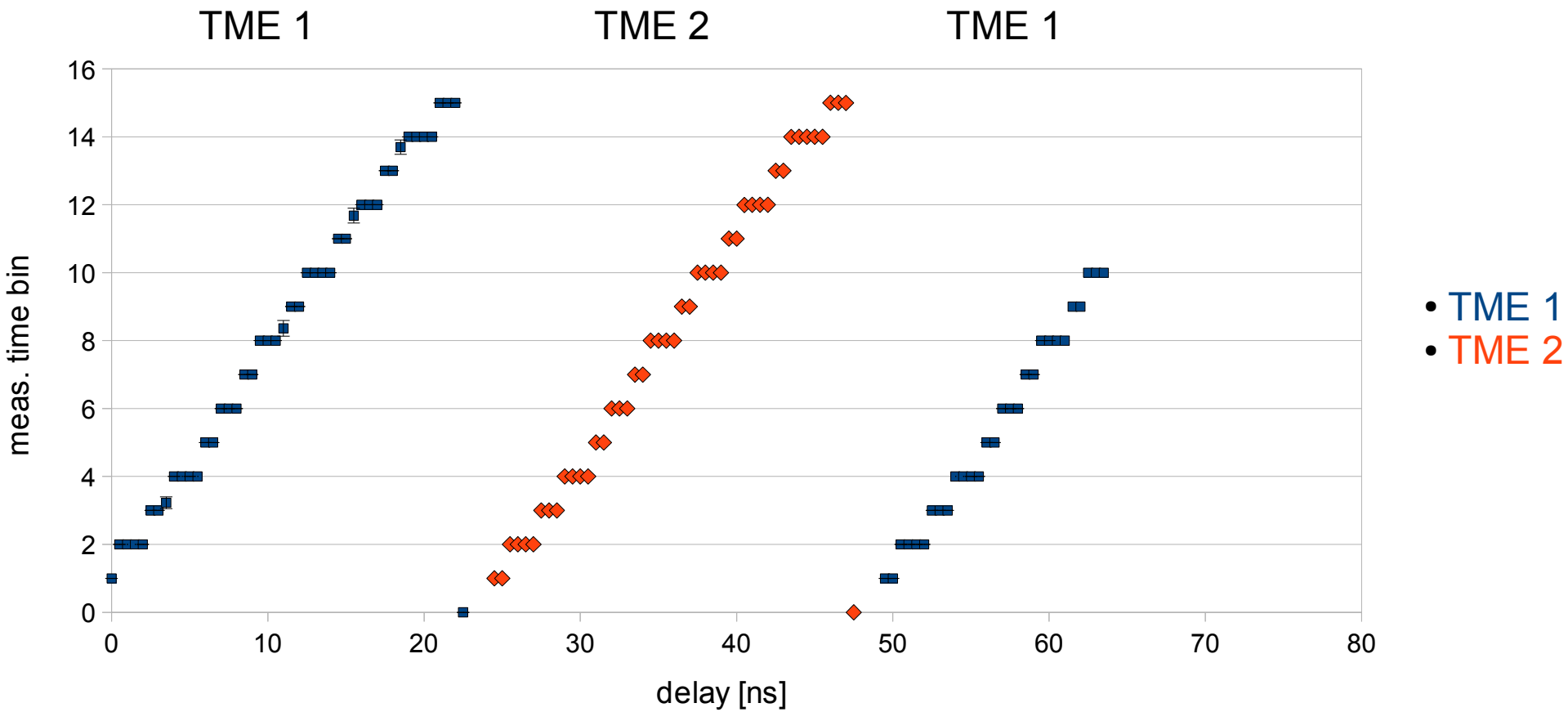


Used Equipment

- Stratix PCI Development Board
  - EP1S25F1020
- NIM Delay element
  - 0ns - 66ns in 0.5ns steps

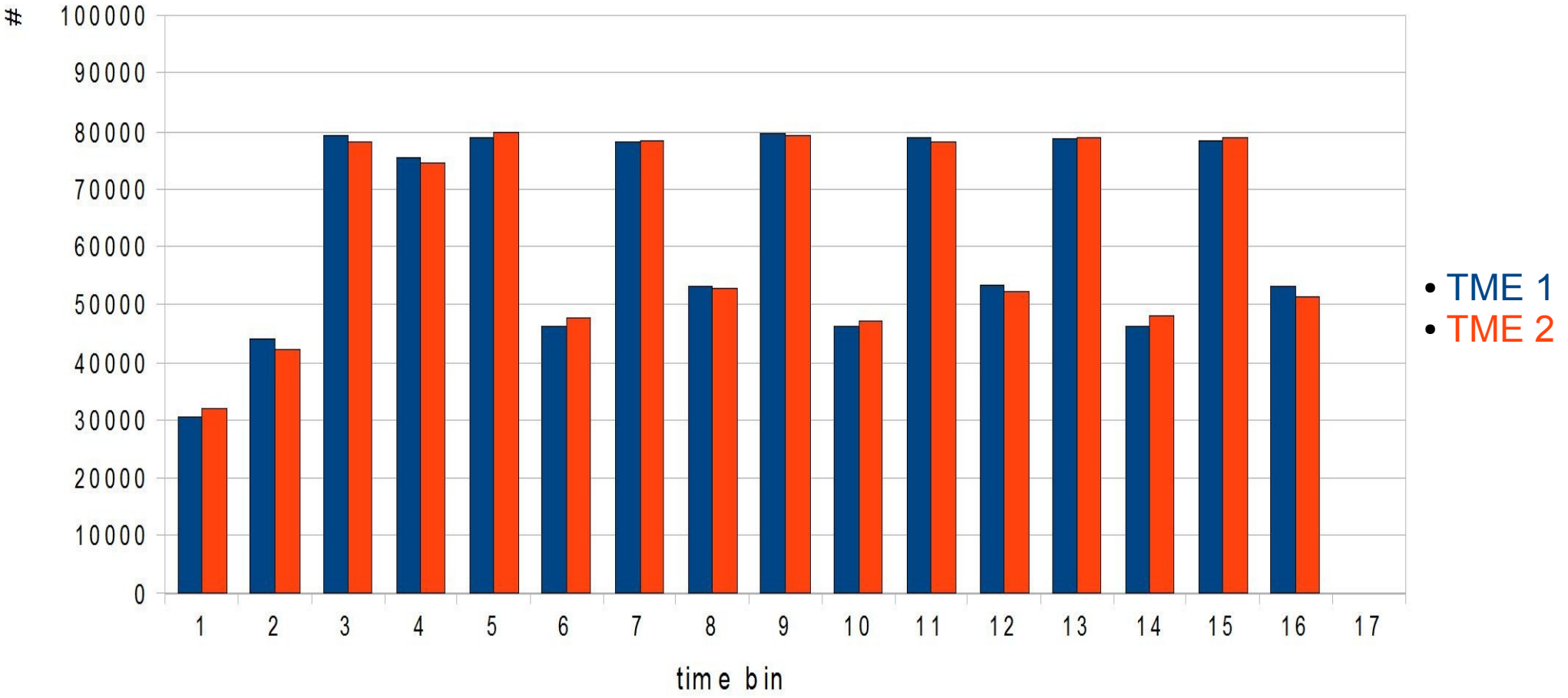


Delay Scan


TME 1
TME 2
TME 1
meas. time bin
delay [ns]
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
80
• TME 1
• TME 2

Bin Size

Using pulse generator with 1MHz clock for hit signal



Summary Part II

- Principle of phase shifted counters work for time measurement
- Fine structures in time measurements has to be further investigated
- Increase number of channels and bins (5bit)
- Develope a test board with an Arria GX FPGA and two 3.1Gbit/s optical links for irradiation tests in 2011

Thank you for your attention!

Backup