A new type of radiation-tolerant pixel detectors implemented in a commercial CMOS technology

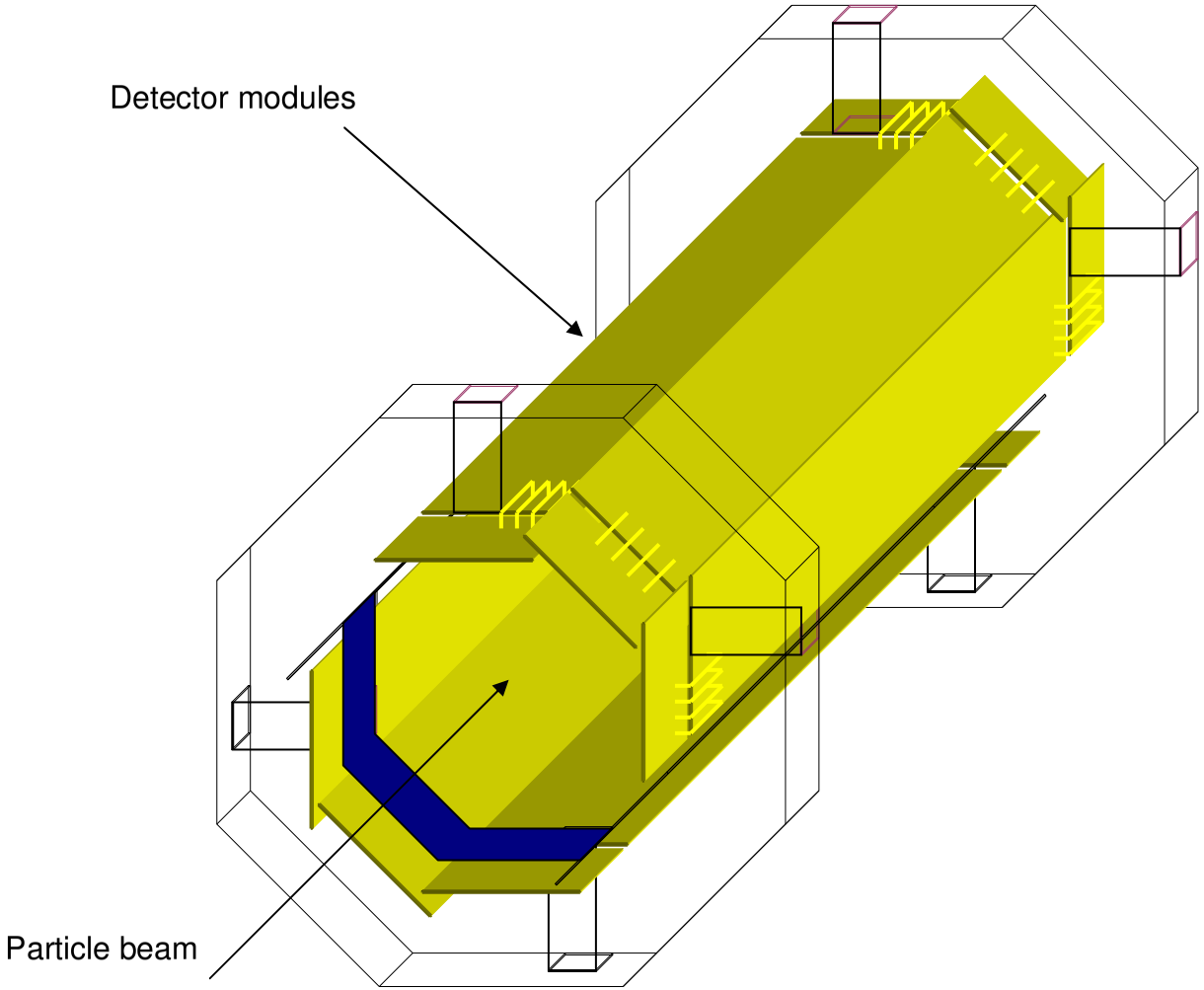
Ivan Peric,
University of Heidelberg
(Institut für Technische Informatik
LS Schaltungstechnik und Simulation)

Introduction
pixel detector technologies

Introduction

- Particle pixel detector technologies - classifications
  - 1. Hybrid detectors
  - 2. Monolithic detectors
  - 1. Detectors with intelligent pixels and sparse readout
  - 2. Detectors with simple pixels and frame readout
- Novel technology “Smart Diode Sensor” SDS
- “The recipe”
  - 1. Take a high-voltage CMOS technology
  - 2. Check if the technology offers “floating-logic” structure
  - 3. Use the depleted high-voltage diode as sensor (n-well in p-substrate diode)
  - Place the electronics inside the diode (inside the n-well)
- Properties:
  - Charge collection by drift
  - PMOS- and NMOS-based electronics in pixels possible
  - By need, simple- or intelligent pixels can be implemented
  - Different readout schemes:
  - 1. Rolling shutter readout
  - 2. Sparse readout
  - 3. Capacitive readout
- Capacitive Coupled Pixel Detector - CCPD

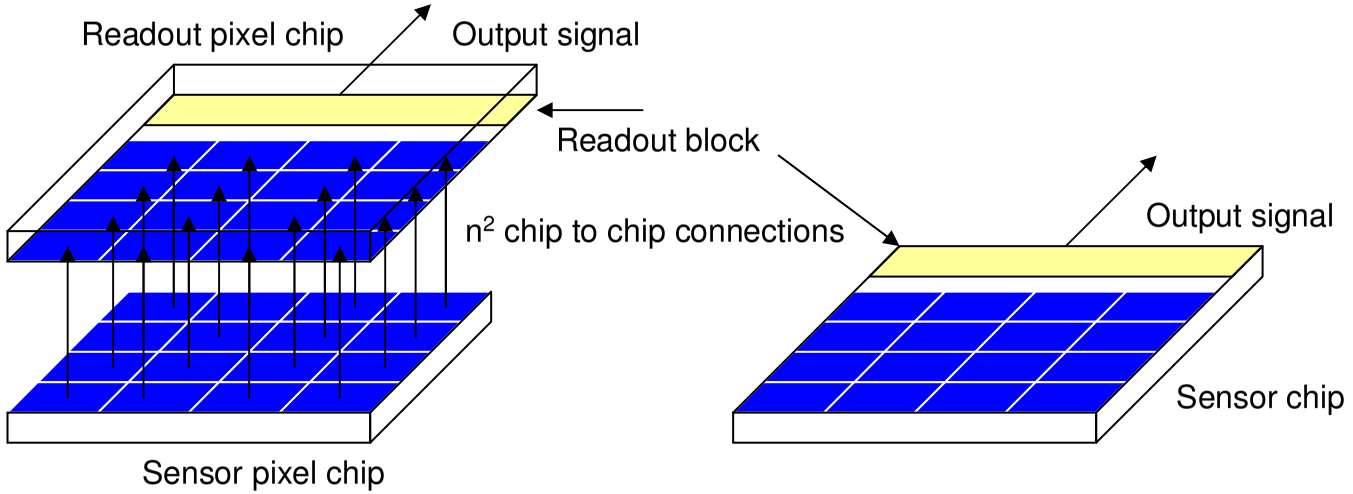
Typical mechanical structure



Specifications

- Particle pixel detector specifications:
  - Pixel size
  - Detector capacitance
  - Noise
  - Signal to noise ratio (SNR)
  - Time resolution
  - Power consumption
  - Fixed pattern noise
  - Amount of material
  - Radiation tolerance

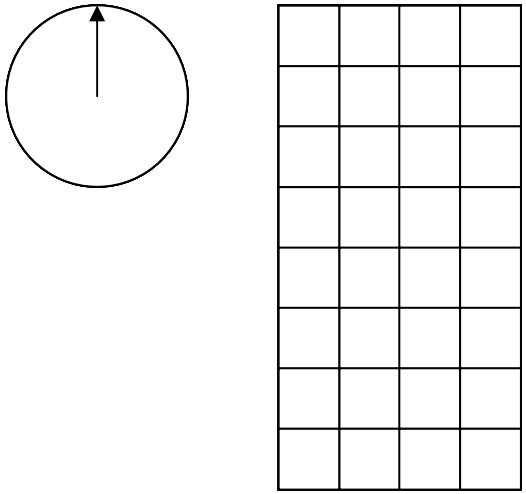
Detector types: hybrid - monolithic



Hybrid detector

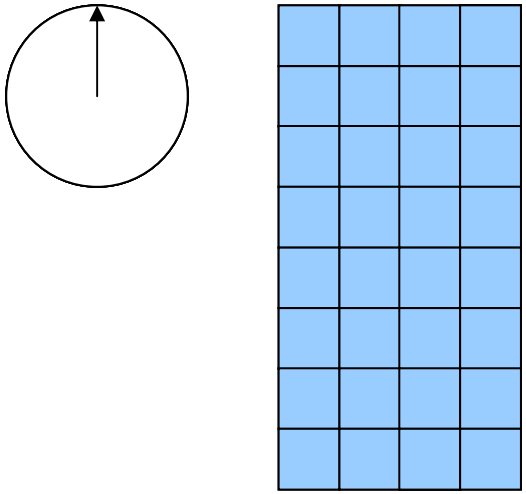
Monolithic detector

Frame readout



- Simple pixels
- Signal and leakage current is collected
- No time information is attached to hits
- The whole frames are readout
  - Small pixels
  - Low power consumption
  - Slow readout

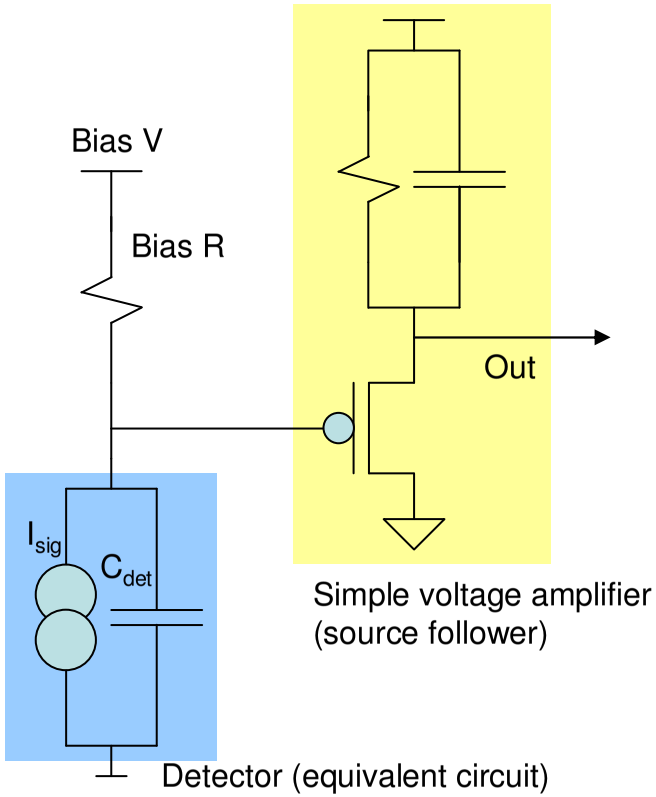
Sparse readout

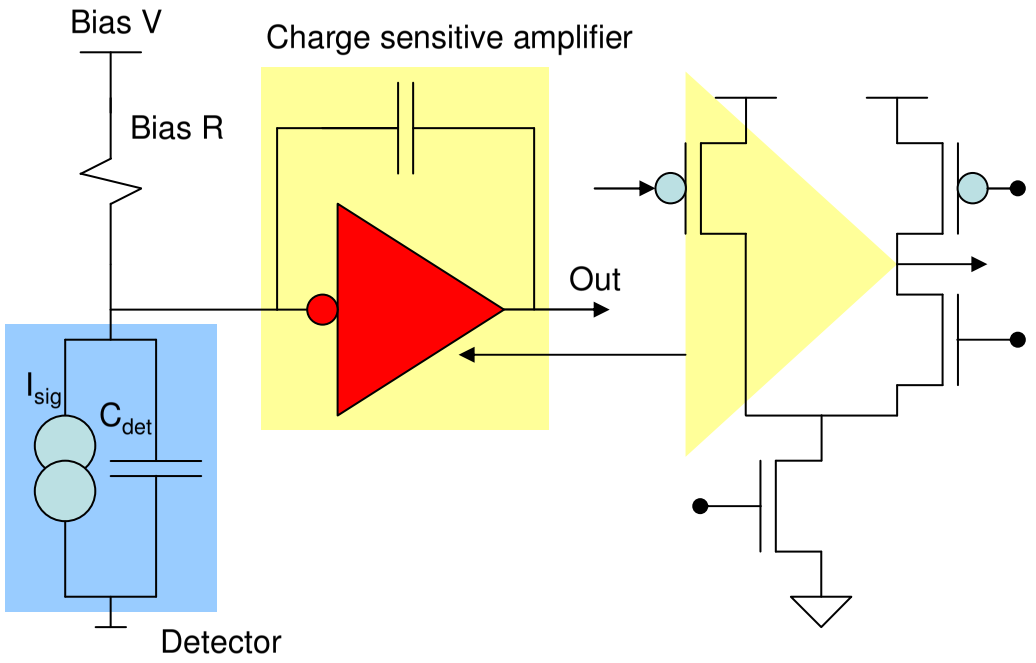


- Intelligent pixels
- FPN is tuned inside pixels
- Leakage current is compensated
- Hit detection on pixel level
- Time information is attached to hits

L Larger pixels
L Larger power consumption
J Fast (trigger based) readout

Front-end pixel electronics





Simple pixels

Intelligent pixels

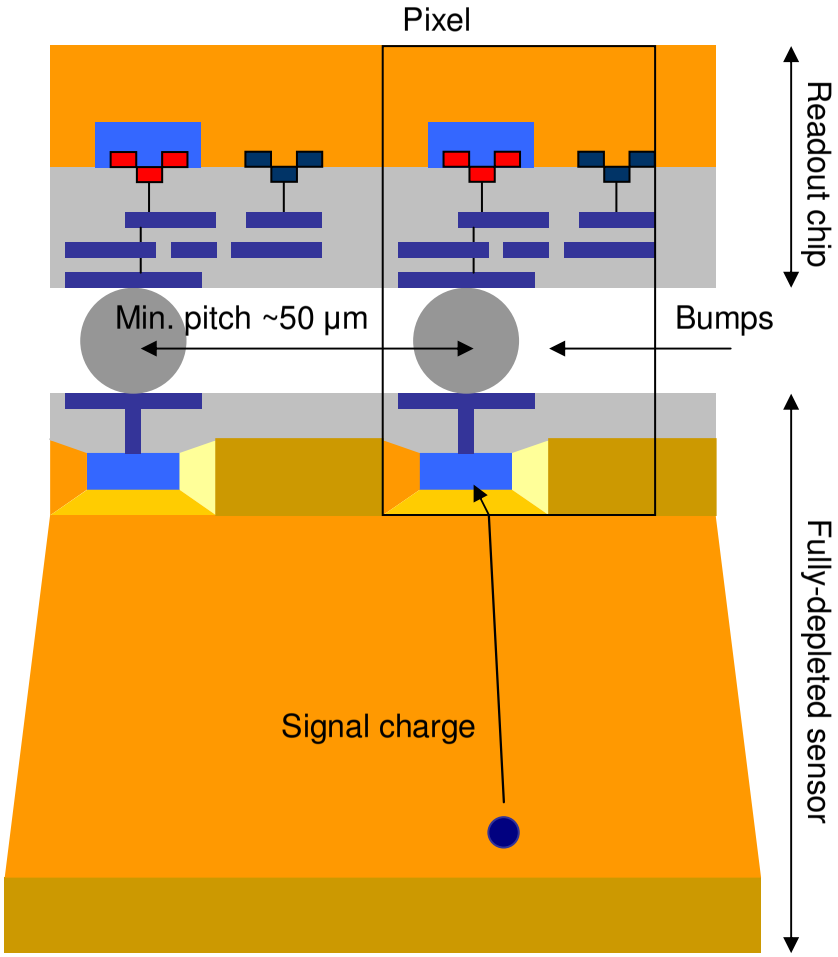
Pixel detector technologies

- State of the art pixel detectors
- Hybrid detectors
  - Standard hybrid detectors
    - intelligent pixels
    - fully-depleted sensor
    - bump-bonding as connection technology
  - Hybrid detectors obtained by 3D integration
    - intelligent pixels
    - fully-depleted sensor
    - wafer-bonding and through silicon “vias” as connection technology
  - SDS with capacitive readout (CCPD)
    - intelligent pixels
    - SDS as sensor
    - capacitive-coupling as connection technology
- Monolithic detectors based on fully-depleted sensor
  - SOI detectors
    - intelligent pixels
    - based on modified SOI technology
  - DEPFET
    - special technology
- Monolithic detectors based on standard CMOS technologies
  - Standard MAPS
    - simple pixels
    - based on an “epi” layer “opto” CMOS process
    - charge collection by diffusion
  - TWELL MAPS
    - intelligent pixels,
    - implemented in a standard deep submicron technology
    - charge collection by diffusion
  - INMAPS
    - intelligent pixels
    - adjusted CMOS technology
    - diffusion
  - SDS
    - intelligent pixels
    - implemented in high-voltage CMOS technology
    - drift as charge collection mechanism

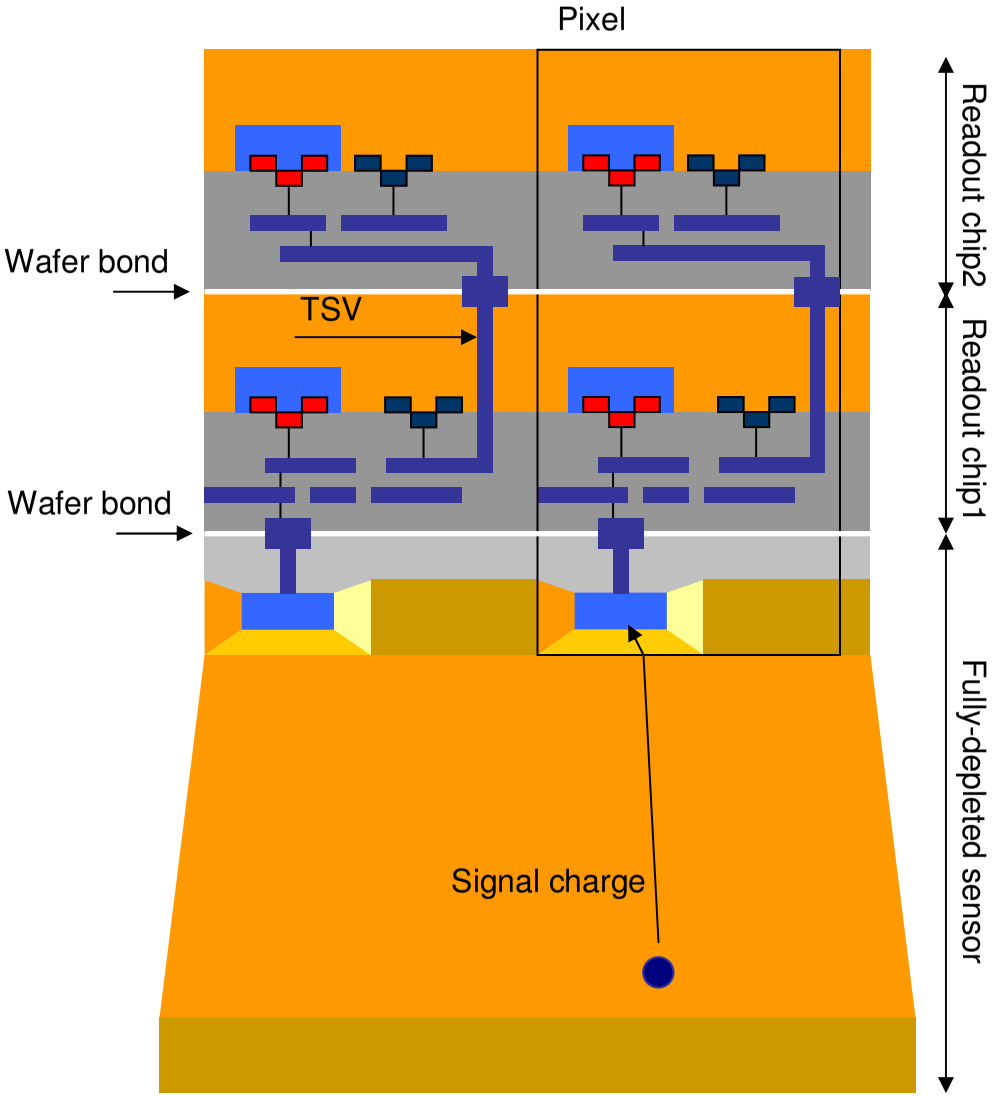
Pros and contras

Type	Pixel size	Readout speed	Amount of Material	Radiation tolerance	Cost
Standard hybrid	large (bump pitch)	High (sparse RO)	large (cooling + bumps + sensor)	high	high (LD sensor + bumps)
3D hybrid	small	high (sparse RO)	moderate (cooling + sensor)	high	high (new technology, LD sensor)
SDS - CCPD	moderate (electrode) ~ 40-50 um	moderate-high (sparse RO) (shaping ~100-300 ns)	low-moderate (cooling)	high 10^{15} n_{eq}, 60MRad	low (standard technology)
SOI	small - moderate	high (sparse RO)	moderate (cooling + sensor)	high?	low? (only one producer)
DEPFET	small	low (frame RO)	low (air cooling)	moderate (~10 MRad, ~10^{13} n_{eq})	? (self made)
Standard MAPS	small	low (frame RO)	low (air cooling)	low (diffusion) 2 x 10^{12} – 10^{13} n_{eq}, a few MRad	low (standard technology)
TWELL MAPS	small	moderate (sparse RO) (charge collection)	low-moderate (cooling)	low-moderate (diffusion but larger electrode)	low (standard technology)
INMAPS	small	moderate (sparse RO) (charge collection)	low-moderate (cooling)	low (diffusion)	? (nonstandard technology)
SDS (frame RO)	small	low (frame RO)	low (air cooling)	moderate – high (leakage current)	low (standard technology)
SDS (sparse RO)	moderate ~ 40-50 um	moderate-high (shaping ~ 100-300ns)	low-moderate (cooling)	high 10^{15} n_{eq}, 60MRad	low (standard technology)

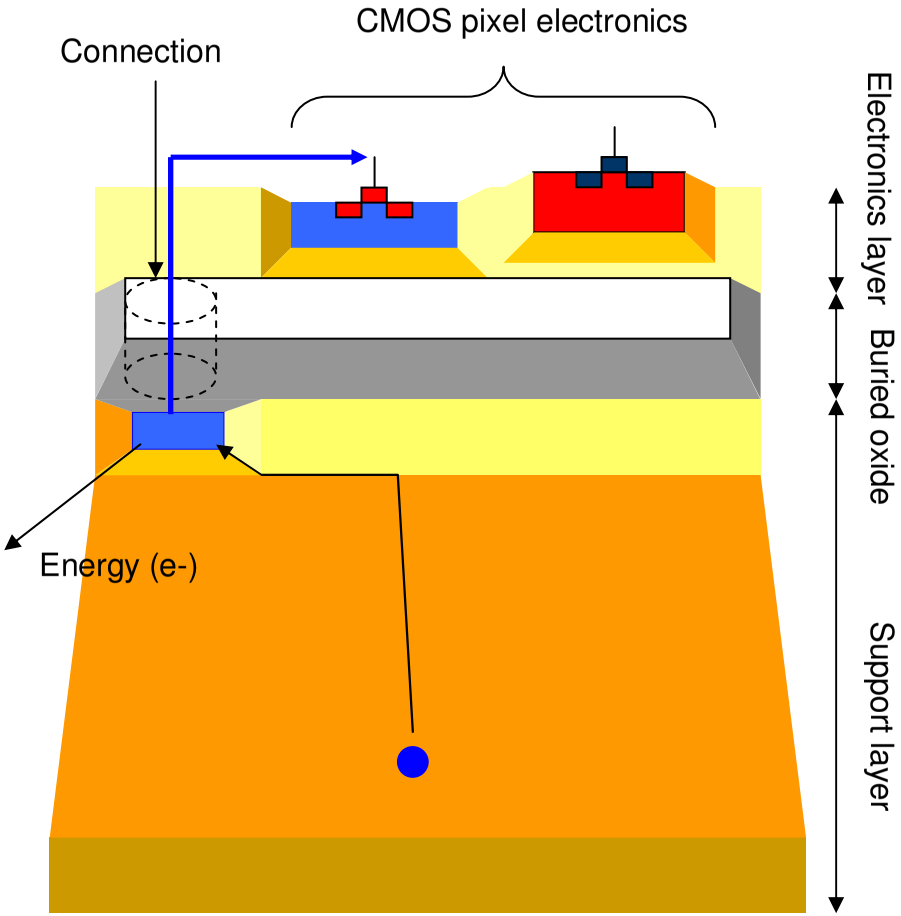
Standard hybrid pixel detector



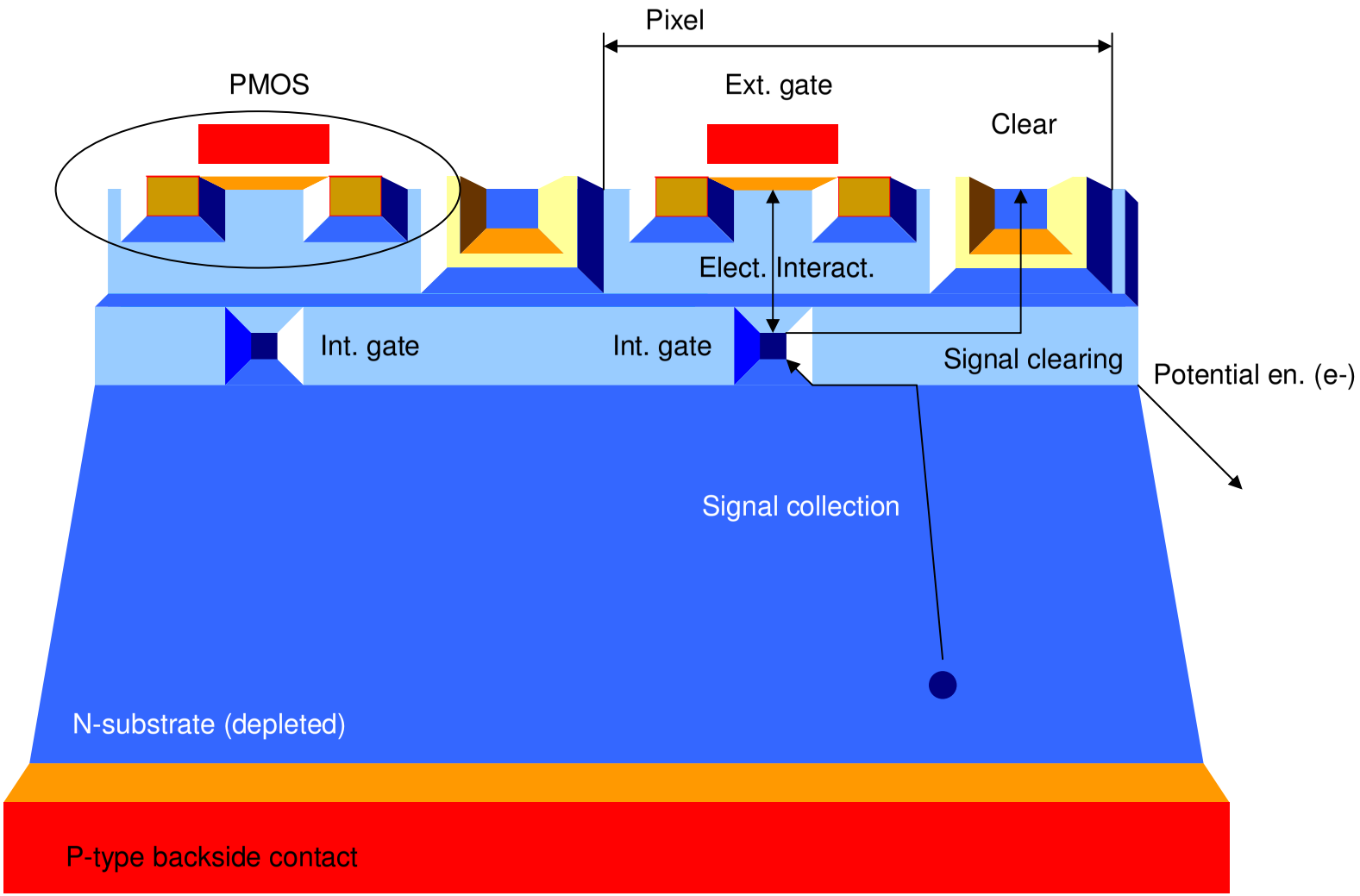
3D hybrid pixel detector



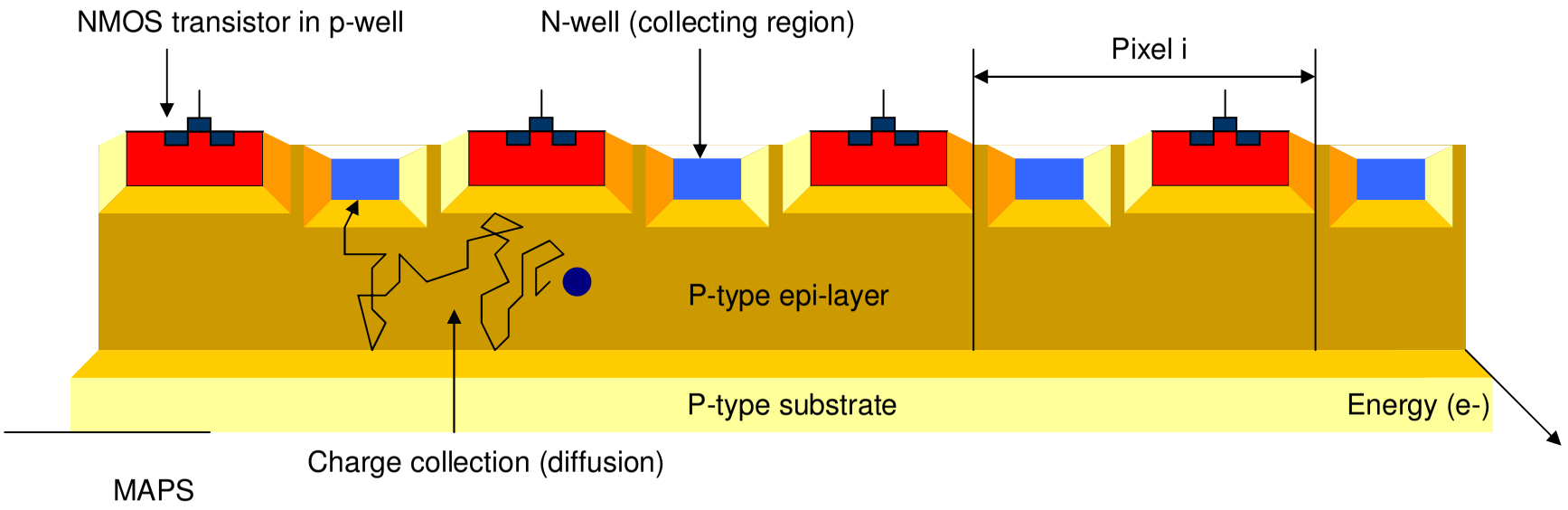
SOI detector



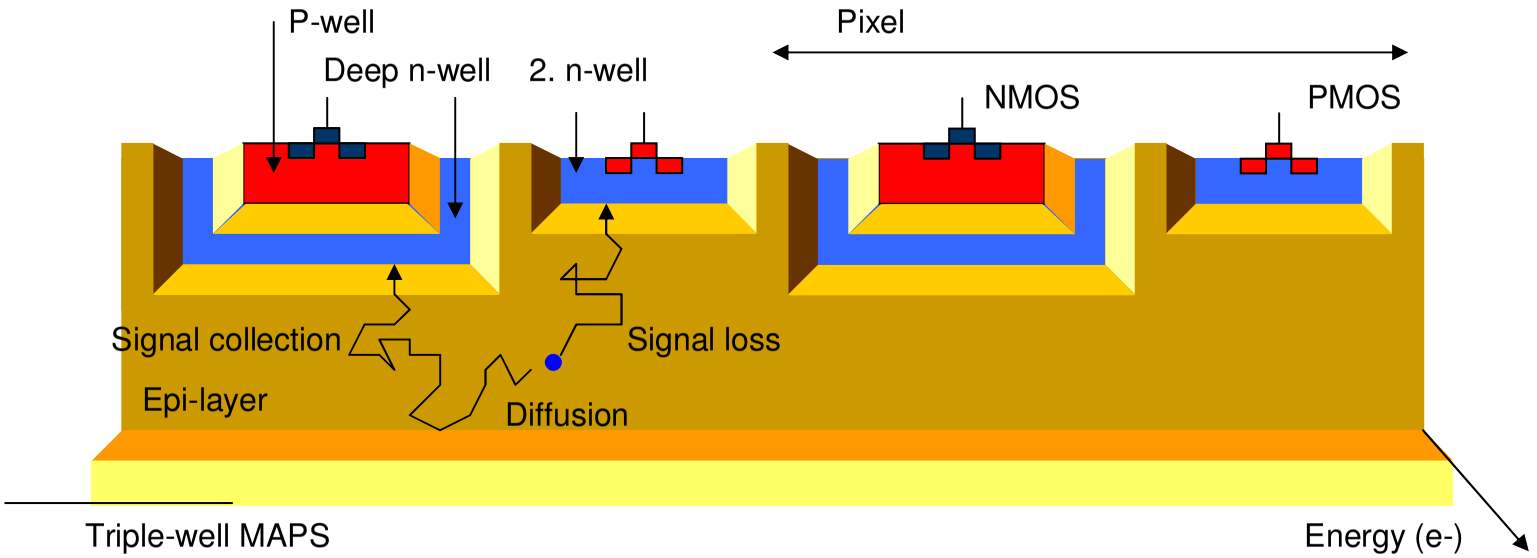
DEPFET


Pixel
PMOS
Ext. gate
Clear
Elect. Interact.
Int. gate
Int. gate
Signal clearing
Potential en. (e-)
Signal collection
N-substrate (depleted)
P-type backside contact

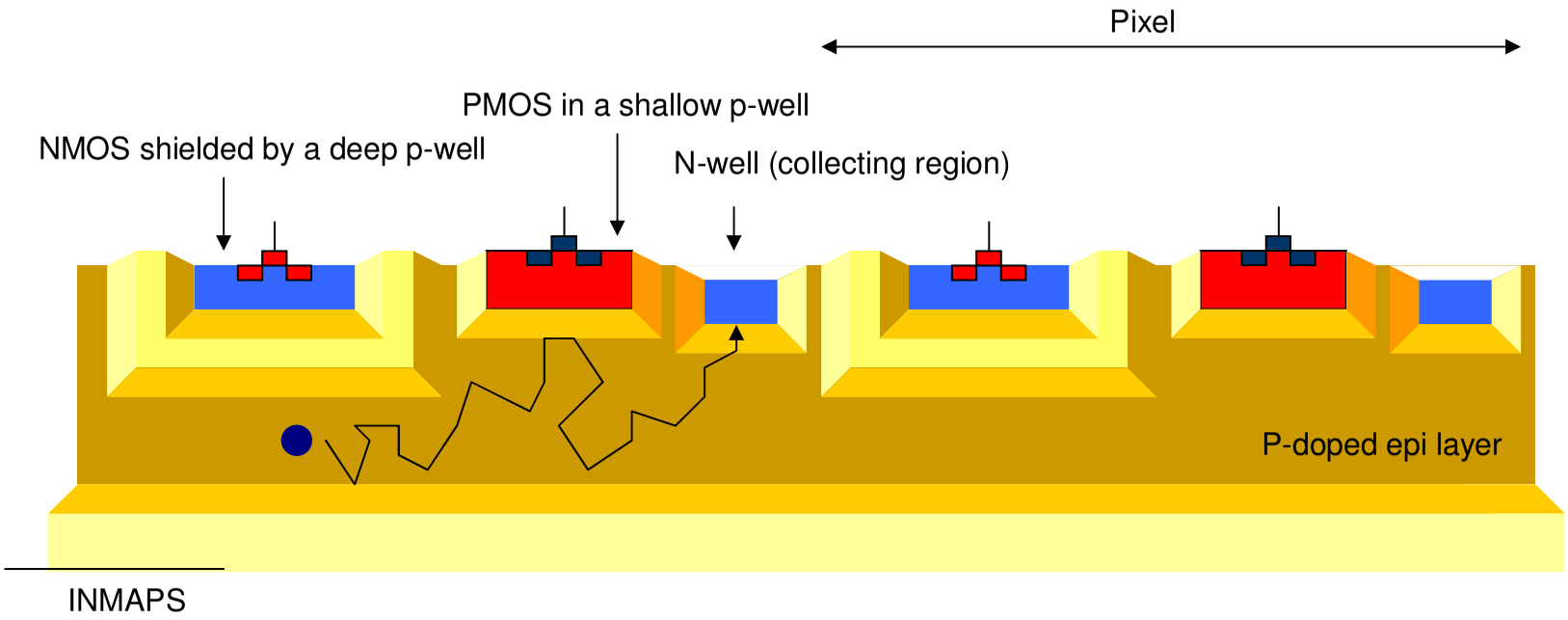
Standard MAPS



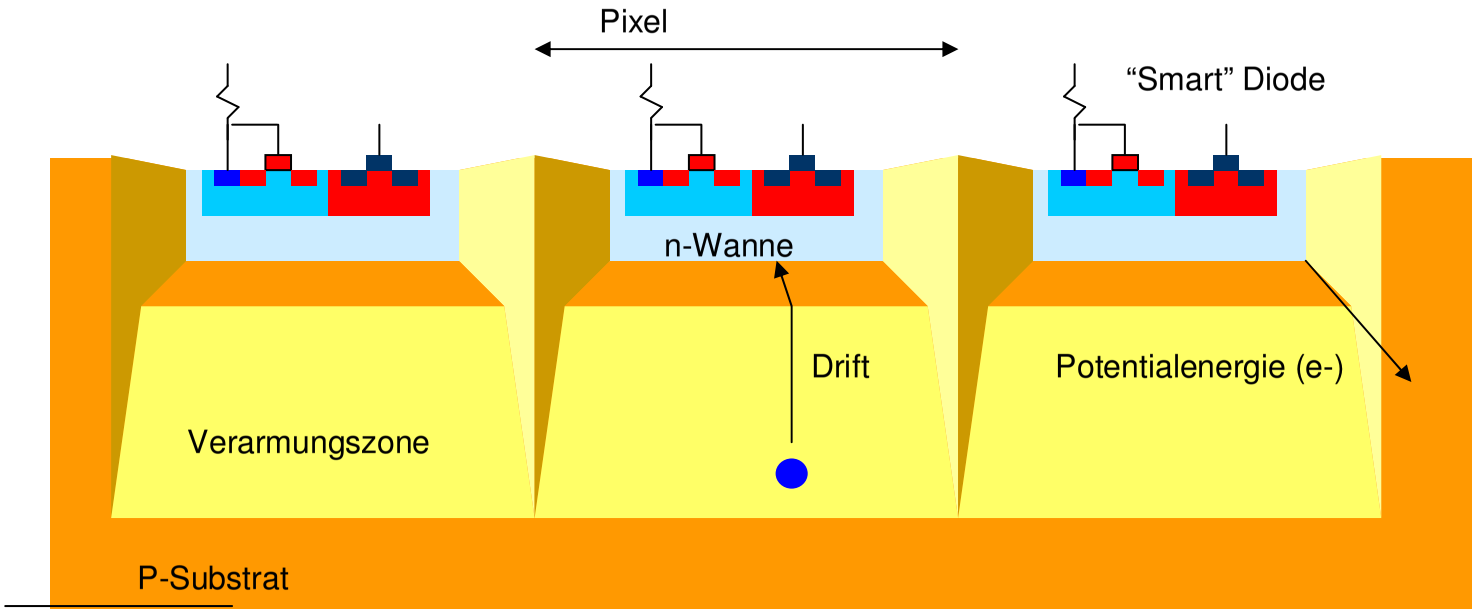
TWELL MAPS


P-well
Deep n-well
2. n-well
Pixel
NMOS
PMOS
Signal collection
Signal loss
Epi-layer
Diffusion
Triple-well MAPS
Energy (e-)

INMAPS

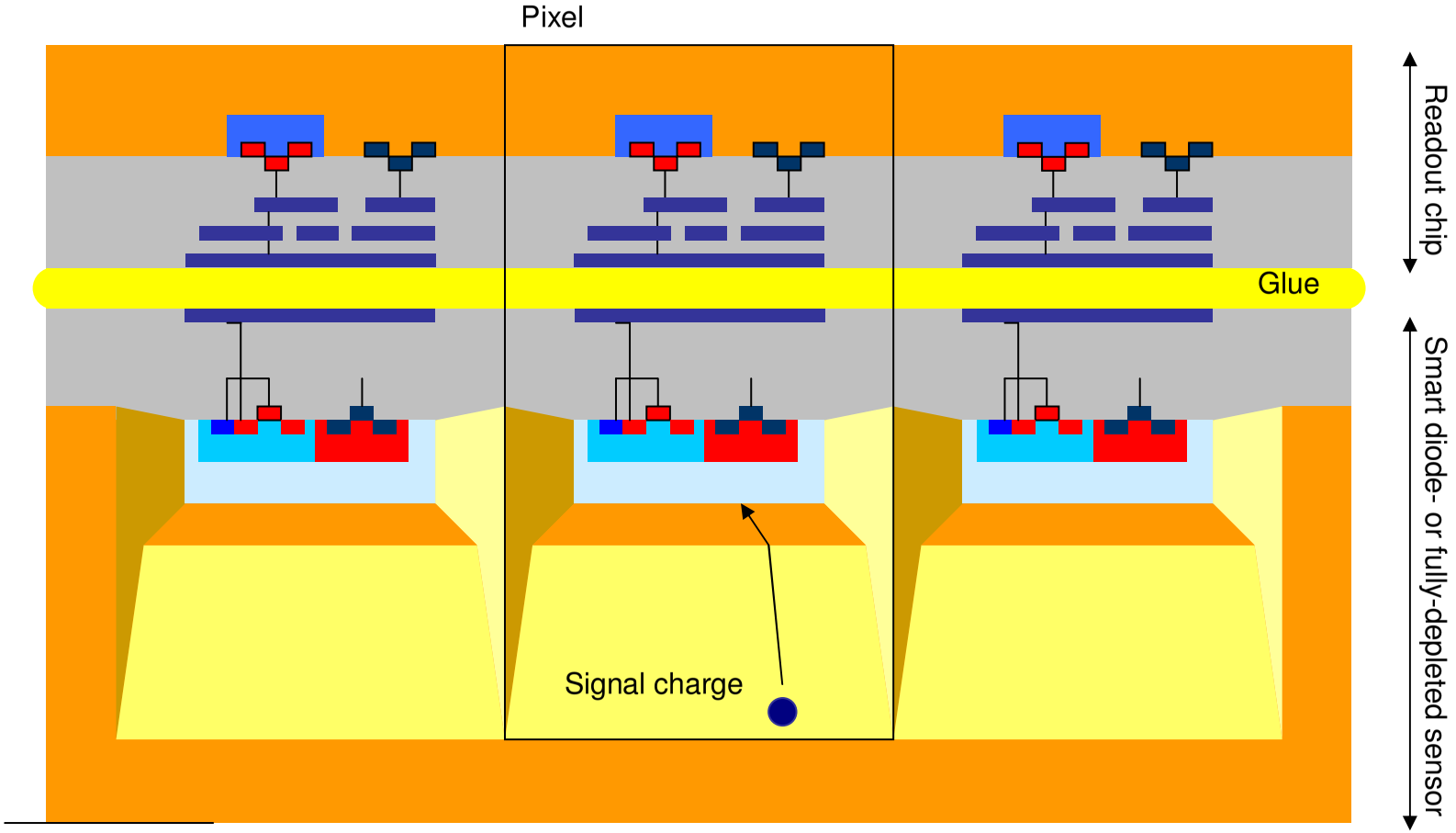

Pixel
PMOS in a shallow p-well
NMOS shielded by a deep p-well
N-well (collecting region)
P-doped epi layer
INMAPS

Smart diode sensor



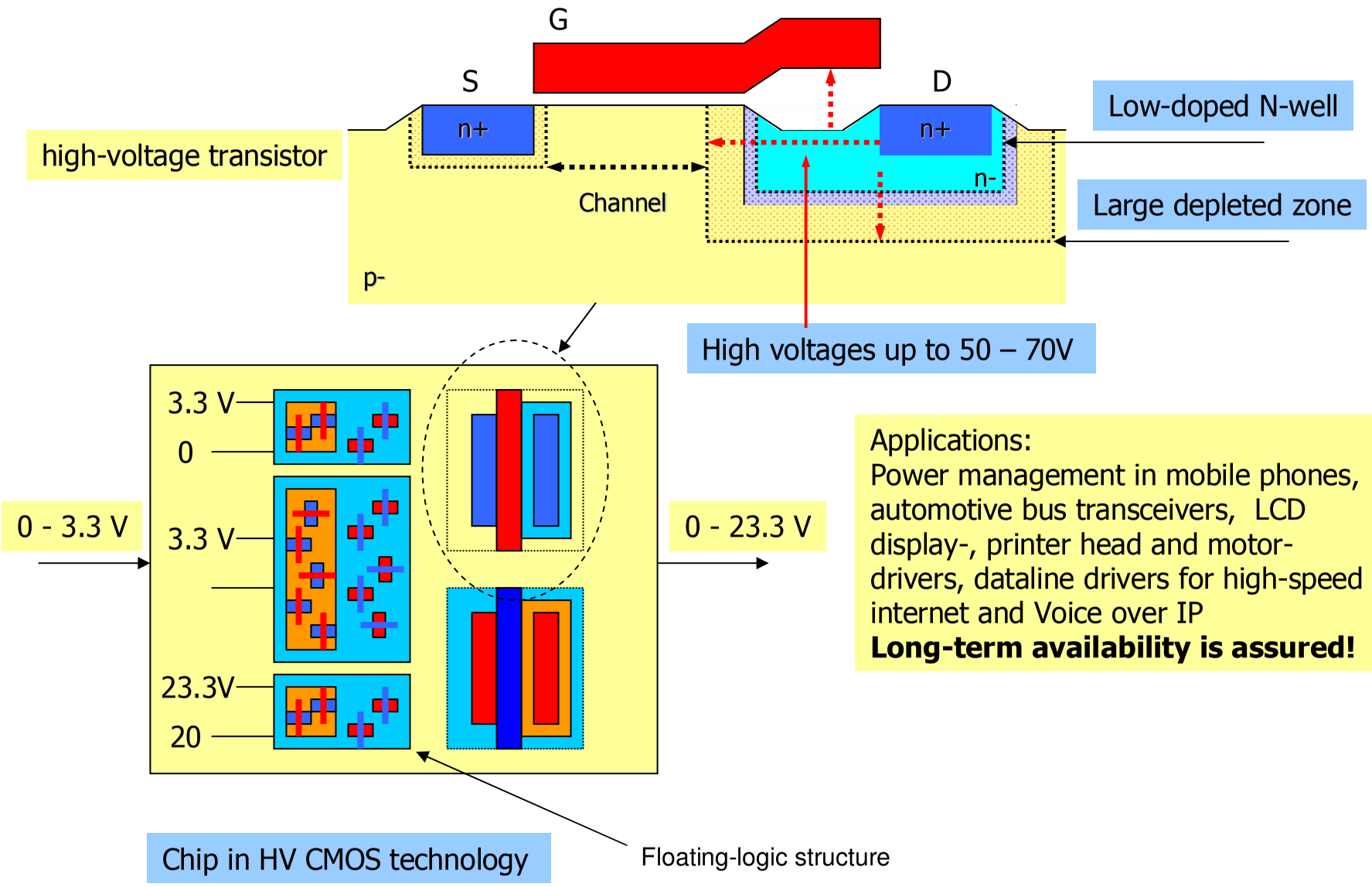
“Smart diode” Detector

Smart diode array with capacitive readout (CCPD)



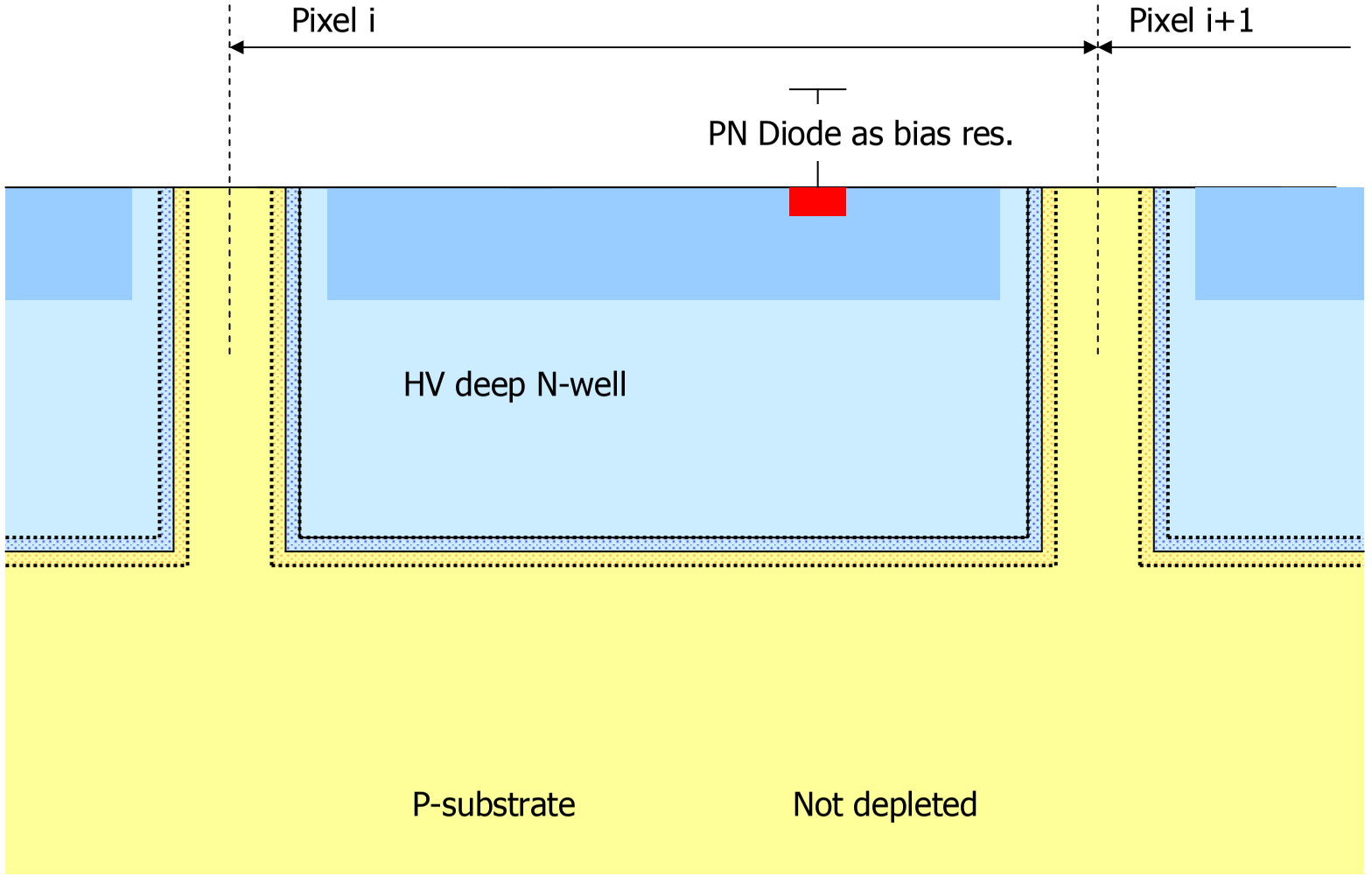
Smart diode sensor

High-voltage CMOS technology

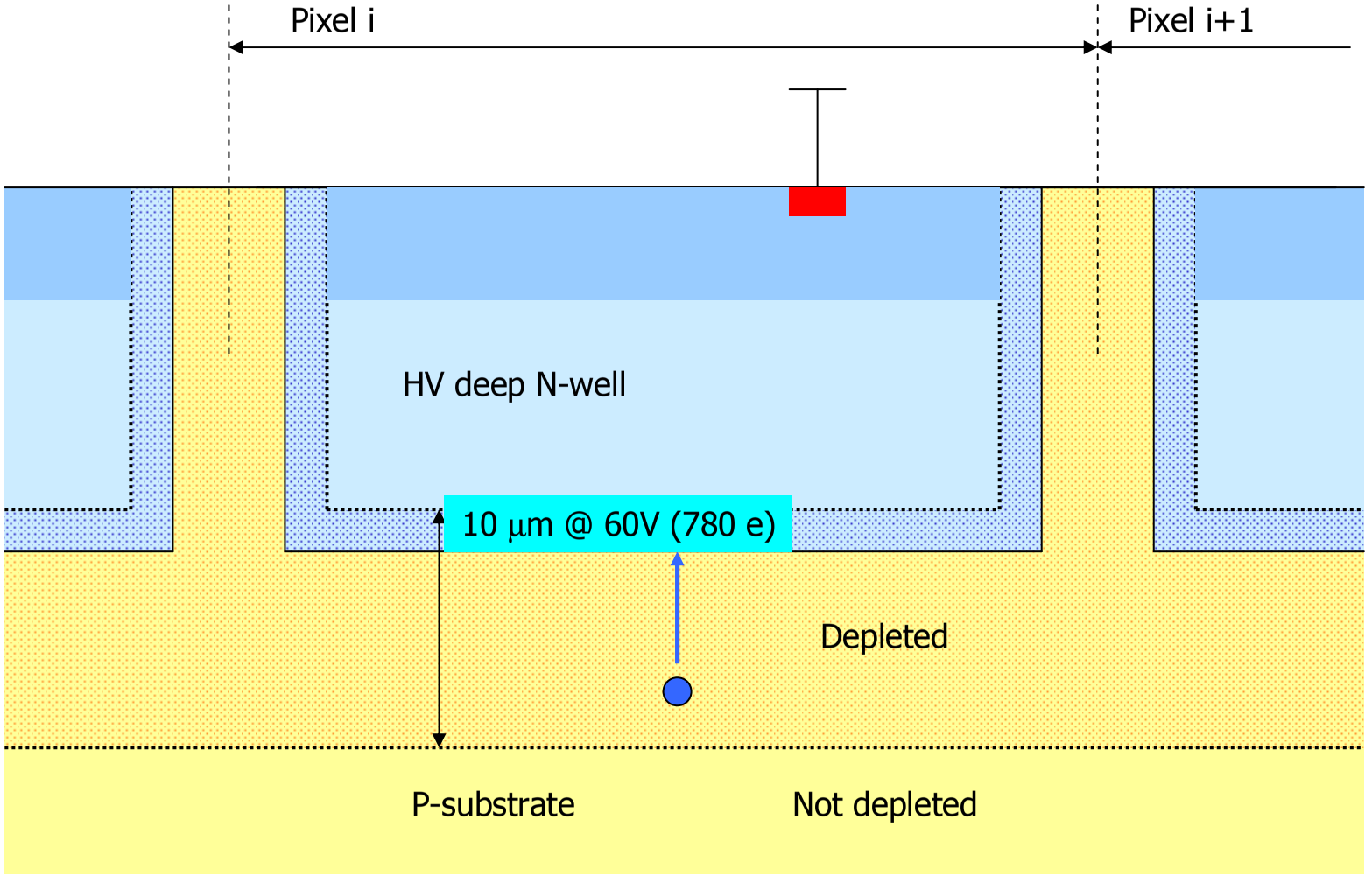


Applications:
Power management in mobile phones, automotive bus transceivers, LCD display-, printer head and motor-drivers, dataline drivers for high-speed internet and Voice over IP
Long-term availability is assured!

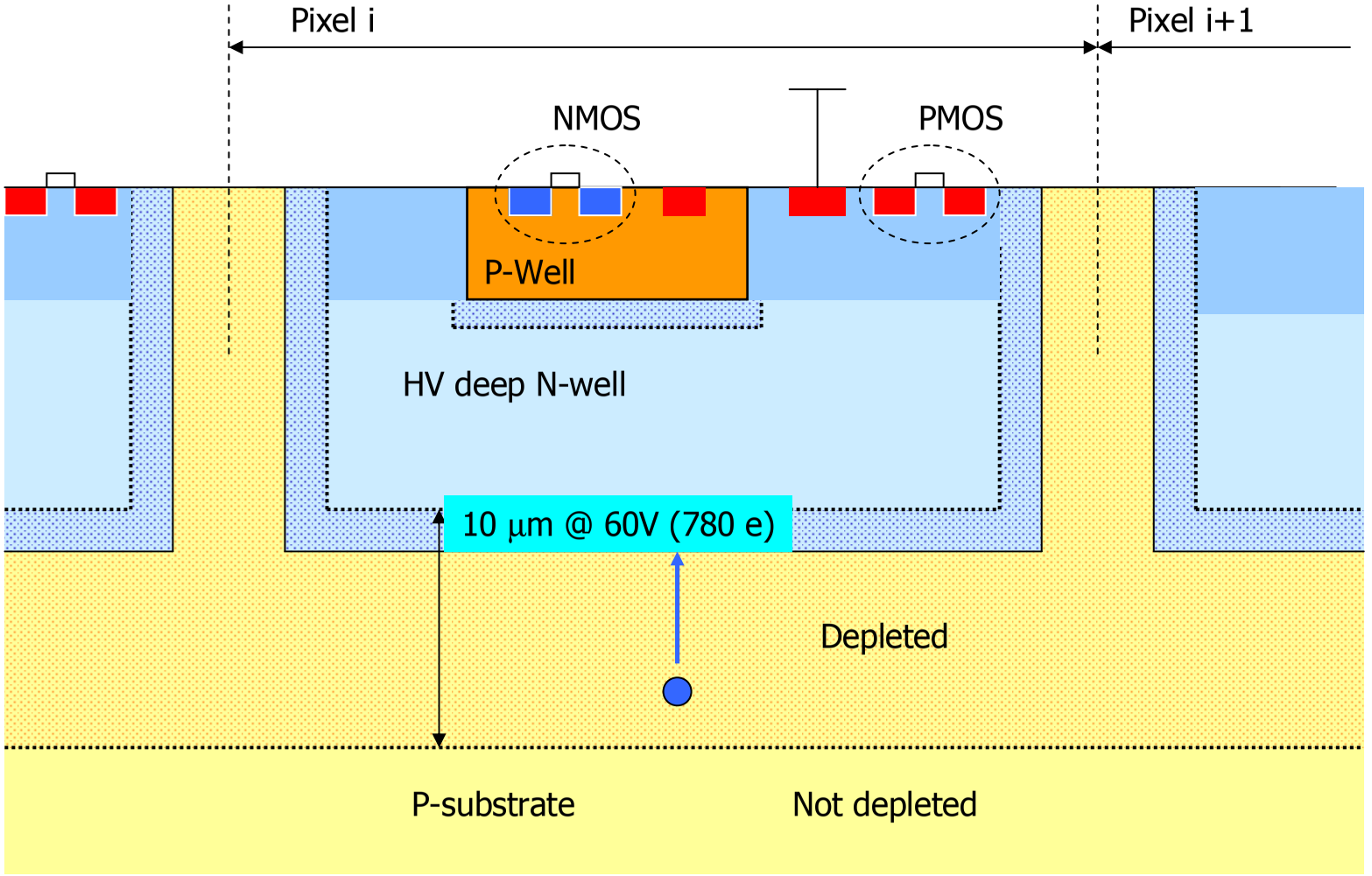
Smart diode


Pixel i
Pixel i+1
PN Diode as bias res.
HV deep N-well
P-substrate
Not depleted

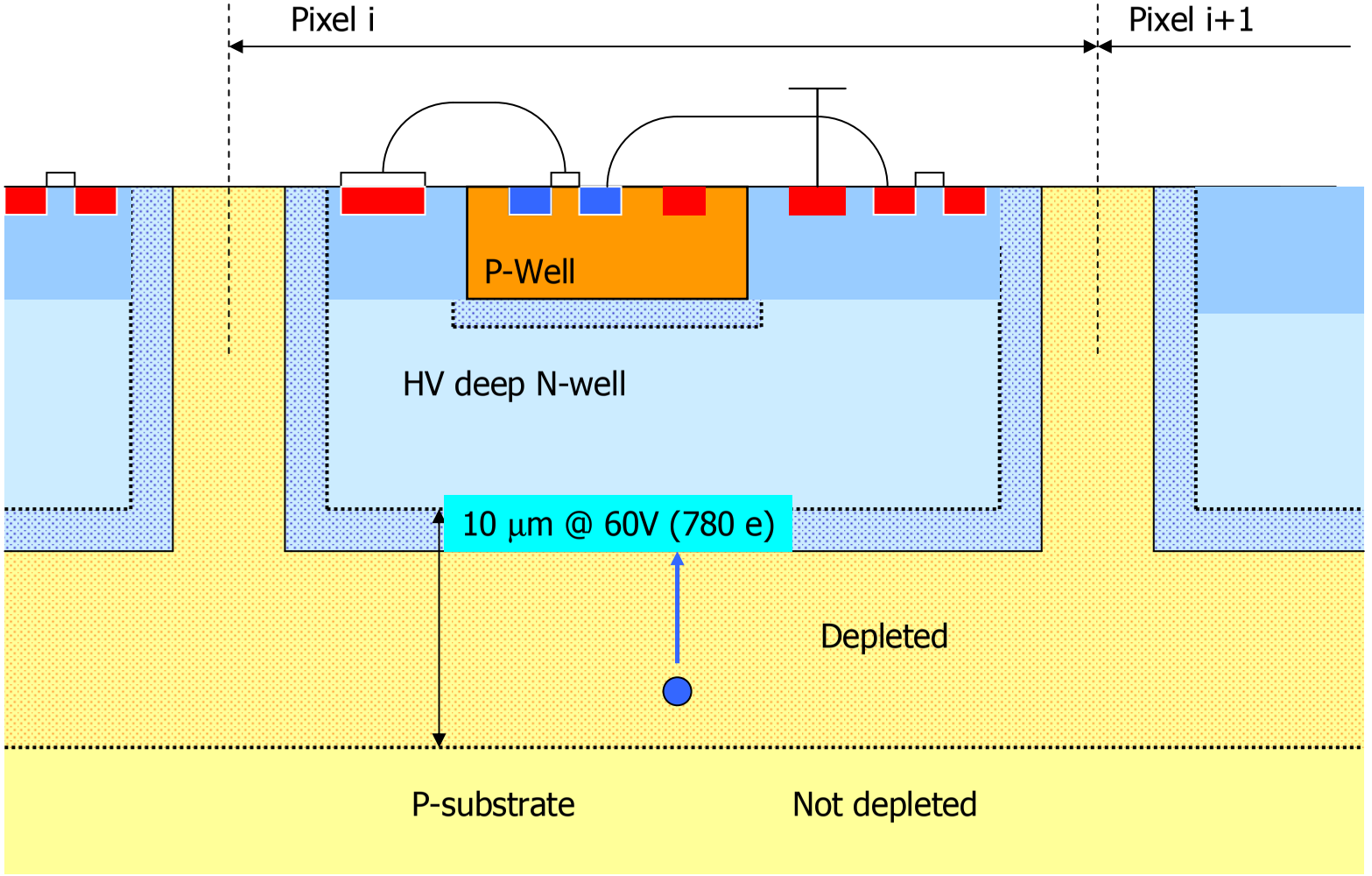
Smart diode


Pixel i
Pixel i+1
HV deep N-well
10 µm @ 60V (780 e)
Depleted
P-substrate
Not depleted

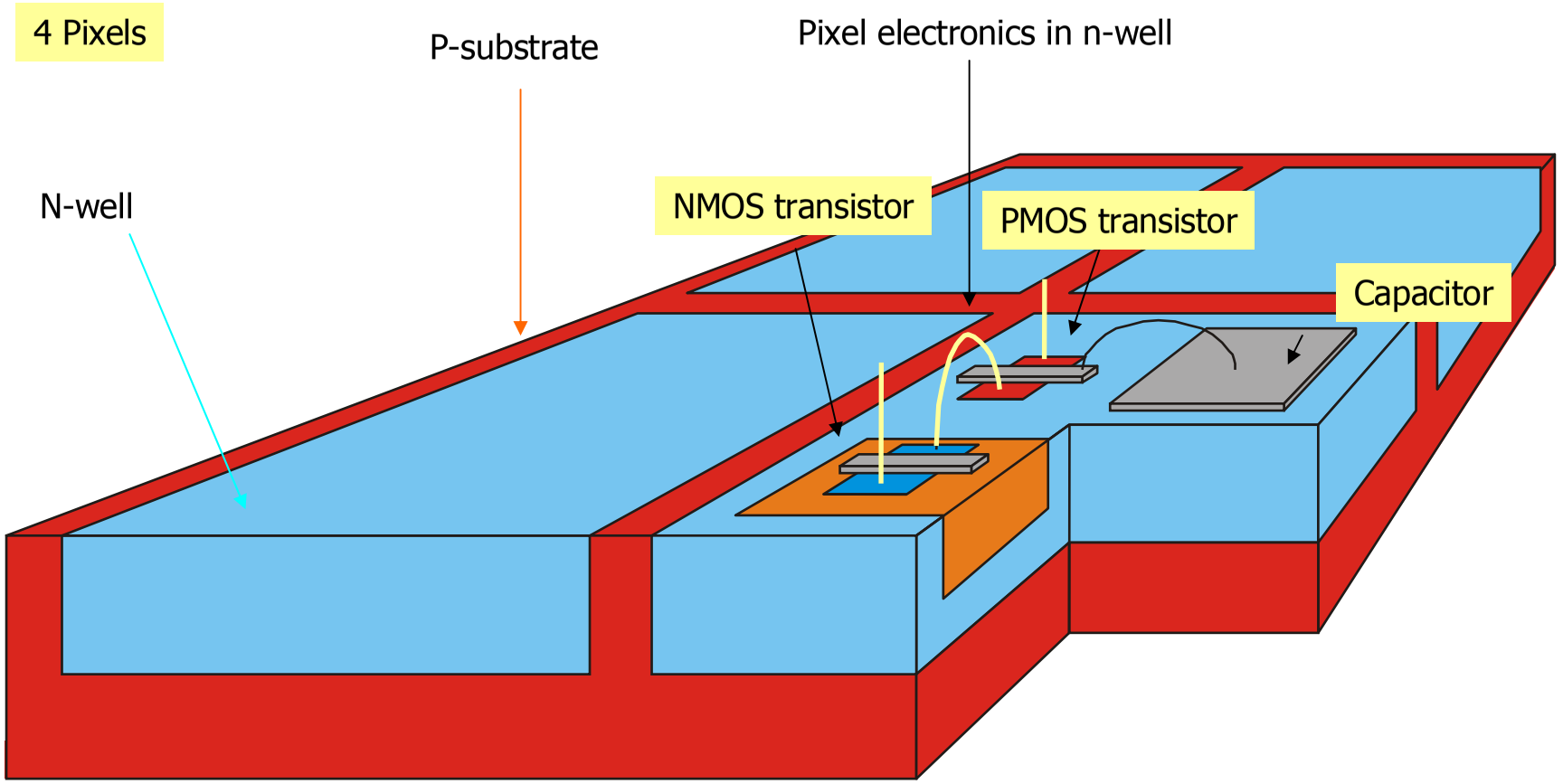
Smart diode


Pixel i
Pixel i+1
NMOS
PMOS
P-Well
HV deep N-well
10 µm @ 60V (780 e)
Depleted
P-substrate
Not depleted

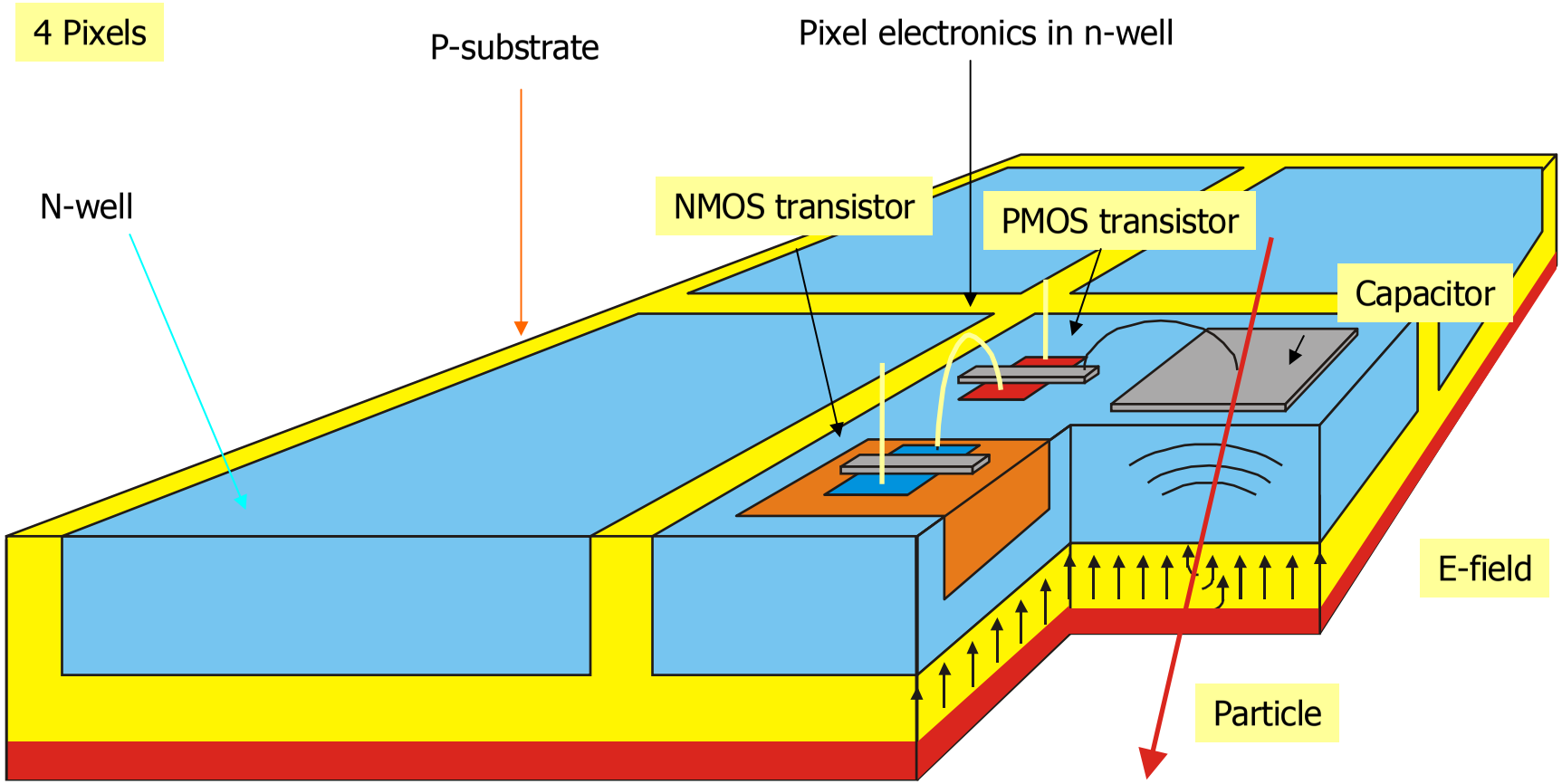
Smart diode


Pixel i
Pixel i+1
P-Well
HV deep N-well
10 µm @ 60V (780 e)
Depleted
P-substrate
Not depleted

Smart diode sensor



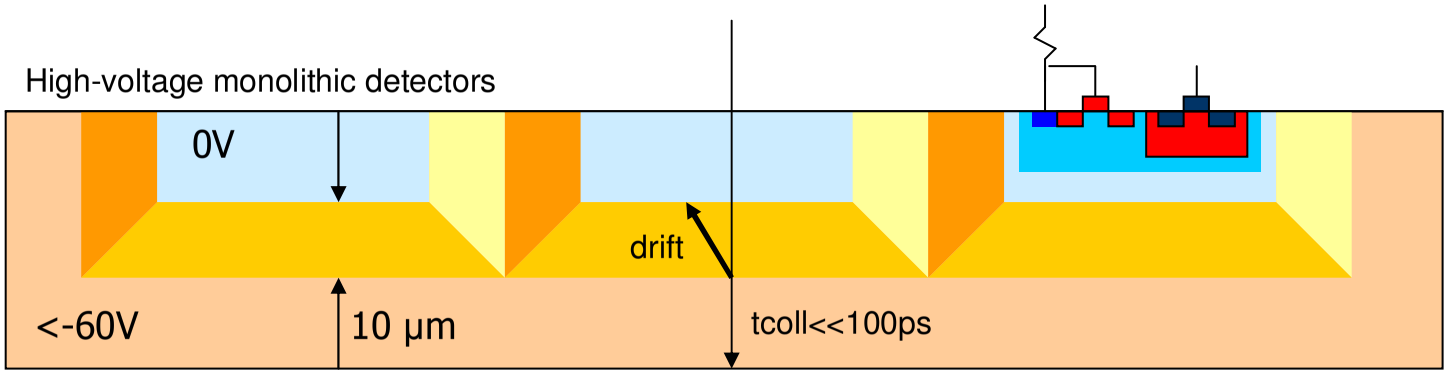
Smart diode sensor

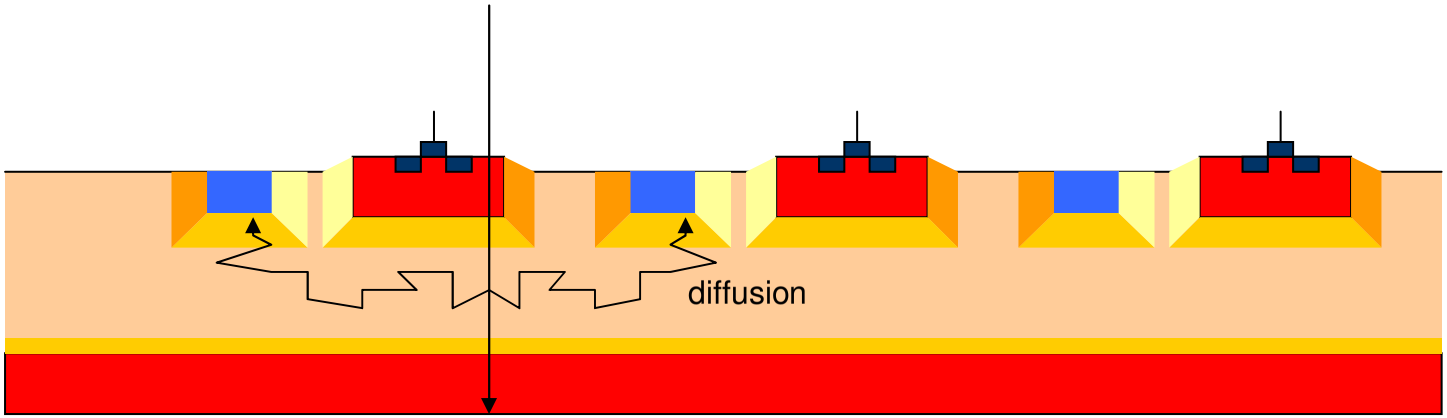


Smart-diode sensor

- Monolithic pixel detectors in high-voltage CMOS technology
- **Main features**:
- Easy to implement (standard CMOS technology used), radiation hard and fast
- Intelligent pixels and sparse readout can be implemented (CMOS electronics)
- Can be very thin (thinner than 50 μm)
- Possible applications: particle tracking in the case of high occupancy and harsh radiation environment such as in (S)LHC, CBM, Belle II, as well as ILC

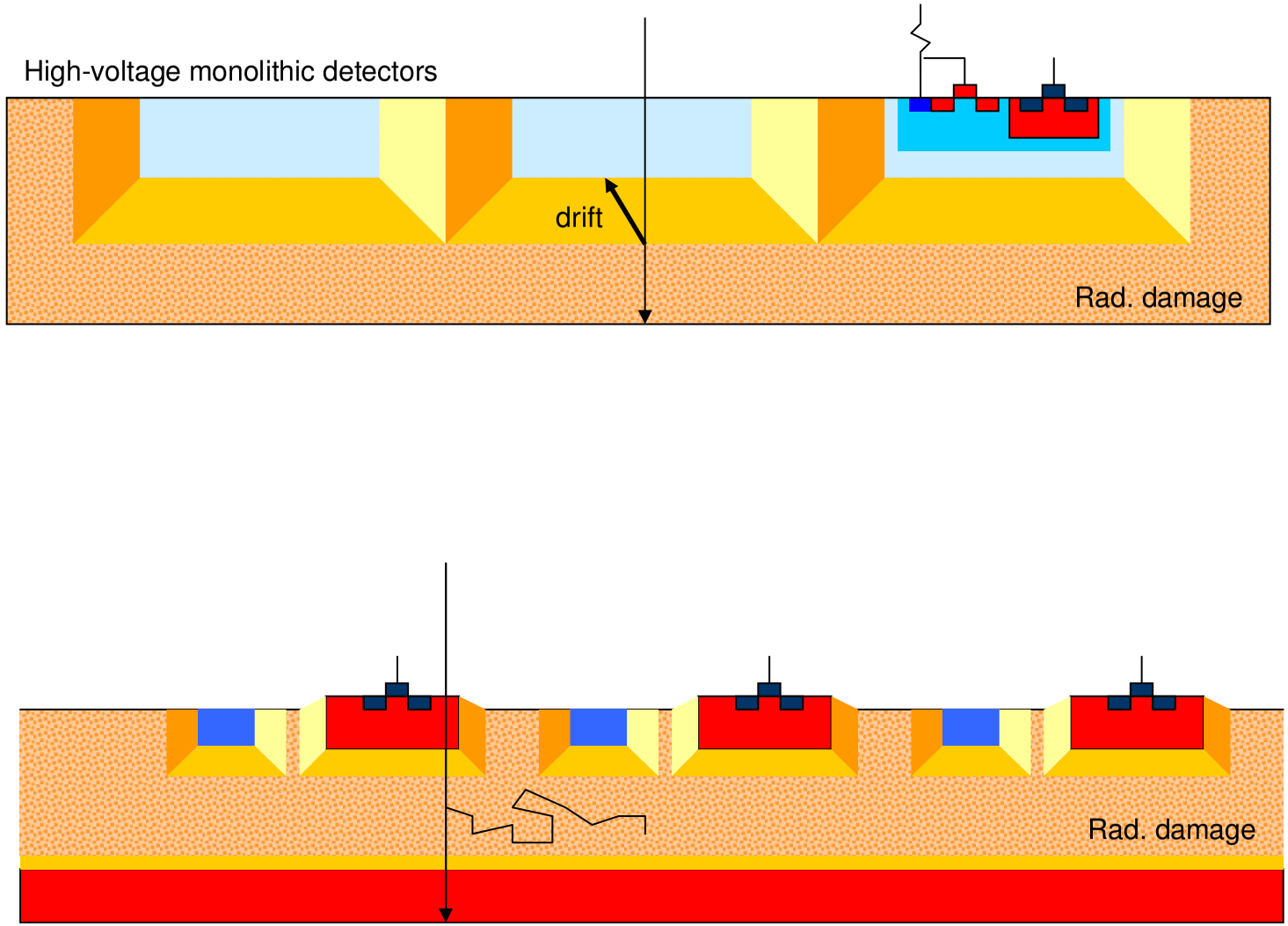
Radiation tolerance





MAPS (as comparison)

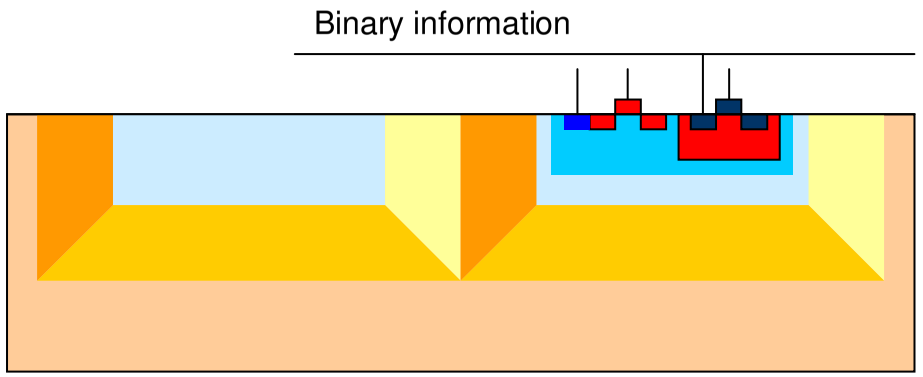
Radiation tolerance



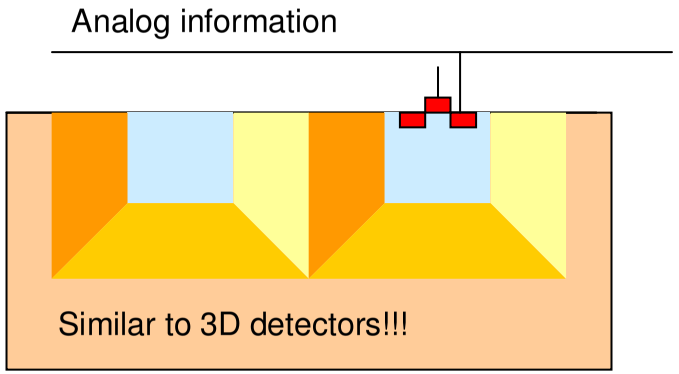
Smart diode sensor - types and achieved results

Detector types

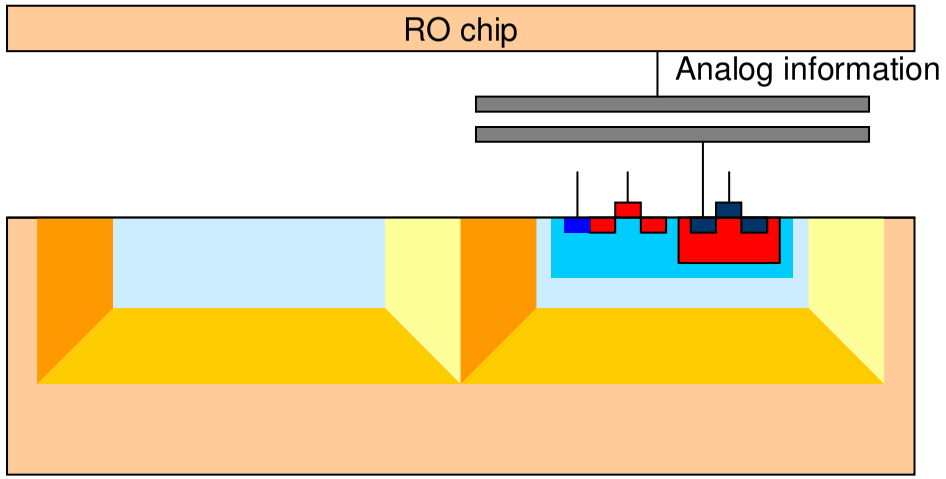
SDS with sparse readout
(intelligent CMOS pixels)
HV2 chip



SDS with frame readout
(simple PMOS pixels)
HVM chip



SDS with capacitive readout
(intelligent pixels)
CCPD1 and CCPD2 detectors

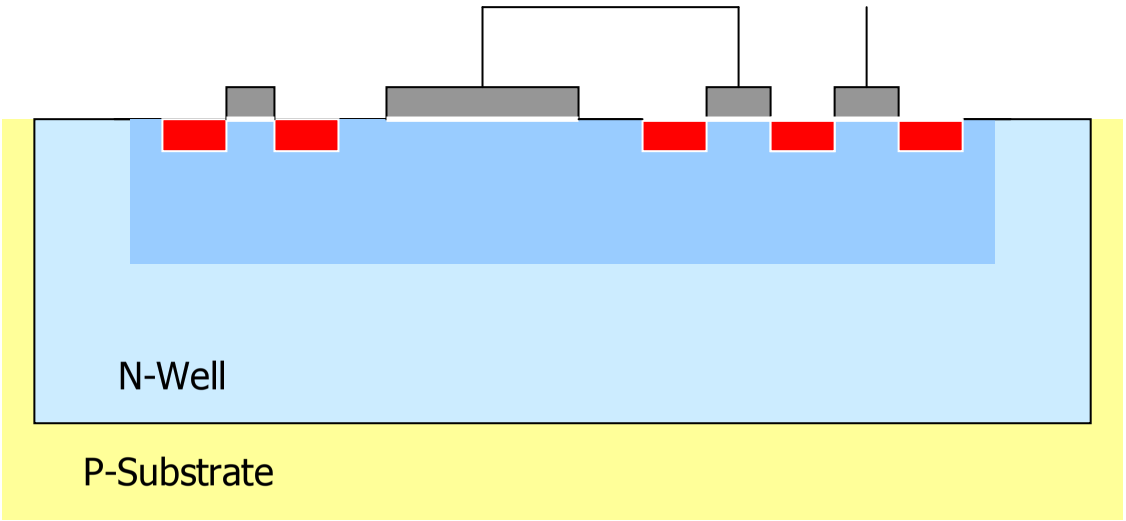


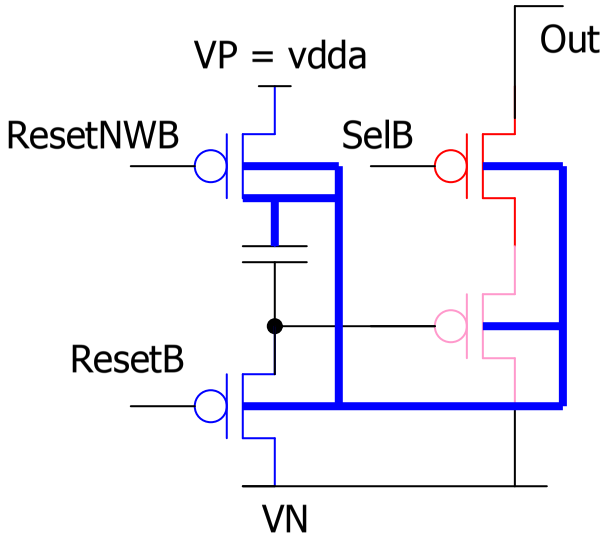
Achieved results

- SDS with frame readout (HVM):
- Pixel size 21 x 21 μm, power: 10.5 μW/pixel (2.6 μ W/pixel analog), 128 x 128 frame readout rate 41 μs, MIP signal 1300e (single pixel) – **2200e** cluster, noise 90e (30e - new chip version, cluster signal to single pixel noise **SNR ~ 94** (beta source ^{22}Na)),
- Signal after neutron irradiation (10^{14} n_{eq}) 1000e (1300e)
- SDS with sparse readout (HV2):
- Pixel size 55 x 55 μm, power 20 μW/pixel, hit timing ~ 150 ns, MIP single pixel signal ~ 1800e, noise 60e (125 ns shaping time), threshold dispersion 30e
- SDA with **capacitive readout (CCPD1 and CCPD2)**:
- Pixel size 50 x 50 μm, power 15 μ W/pixel, hit timing ~ 300 ns, MIP single pixel signal ~ 1800e, noise 30 - 40e, SNR ~ 60 - 45,
- **SNR measured with beta source ^{22}Na after proton irradiation (10^{15} n_{eq}) at 10°C ~ 55**
- **Noise at room temperature after x-ray irradiation (60Mrad) 120e**
- Test beam:
- Efficiency 85% (probably due to test setup timing issues, not the real detector inefficiency), cluster signal 2200e, seed 1300e, spatial resolution ~ 7 μm, noise 90e (new chip version has 30e, we expect better results with the new version)

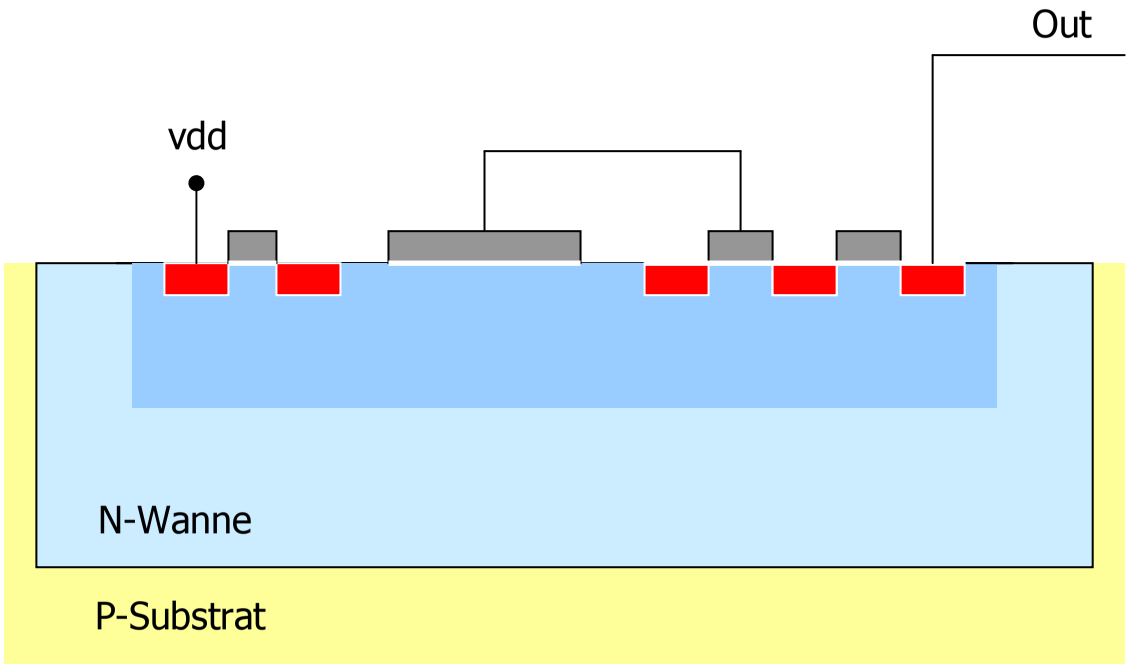
Smart diode sensor – the variant with simple pixels and frame-mode readout

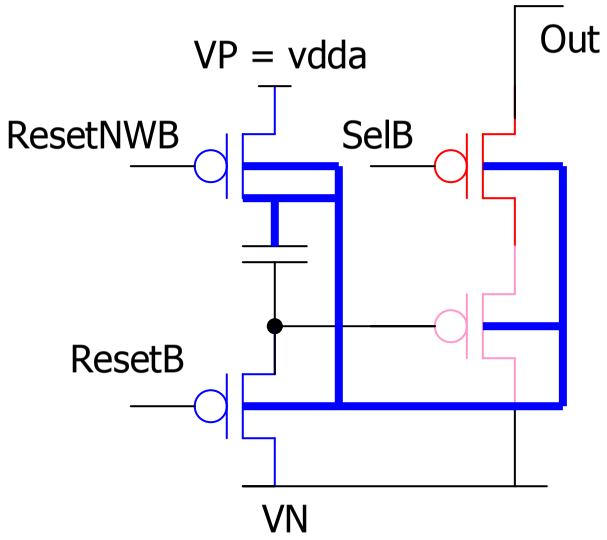
Simple pixel cross-section



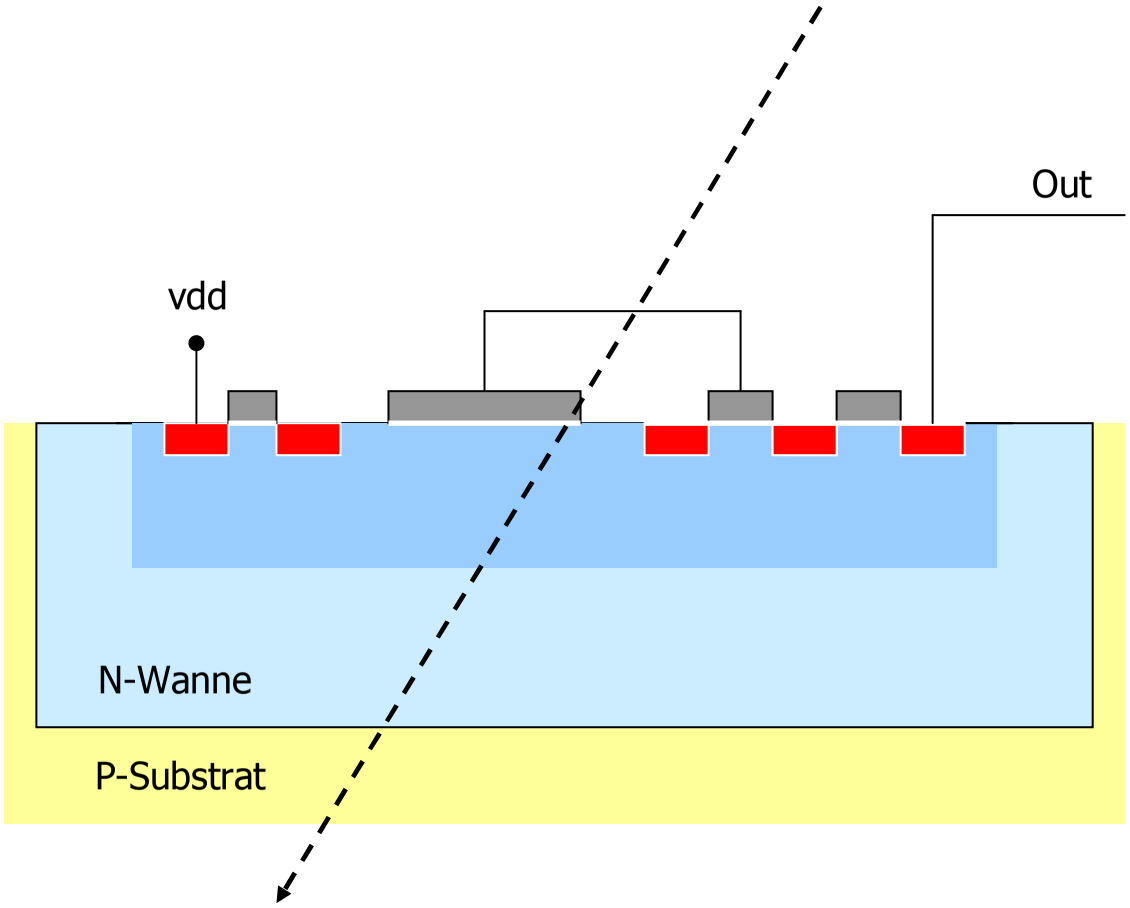


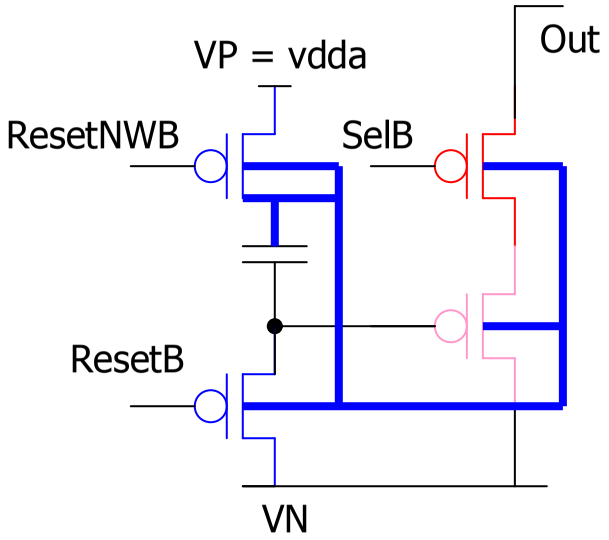
Simple pixel – signal generation



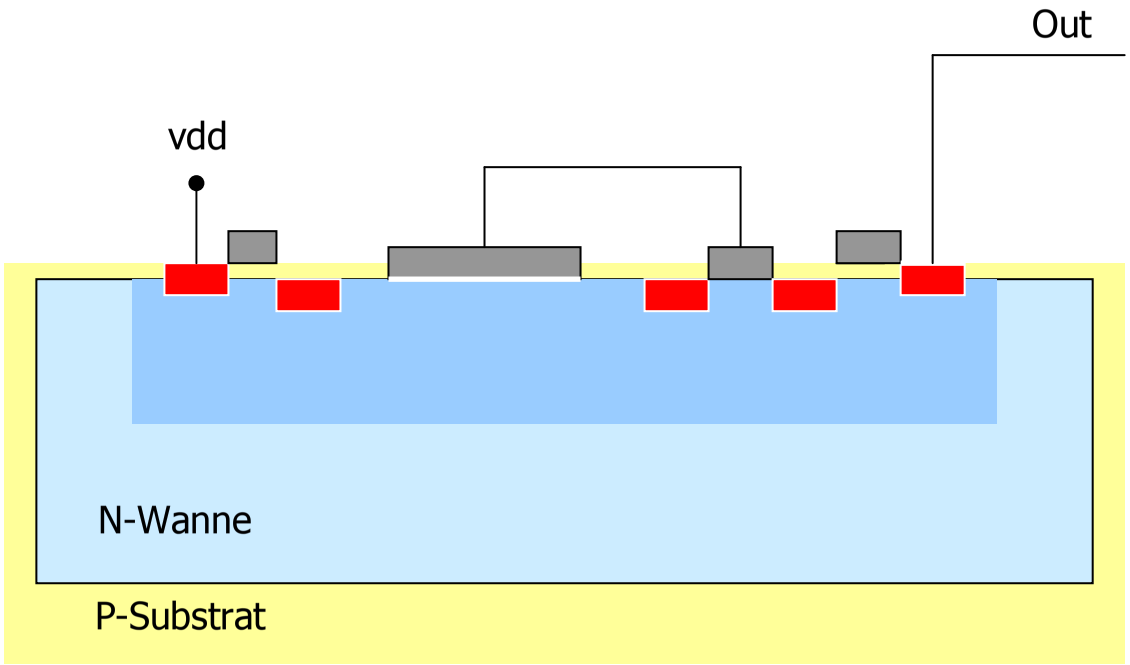


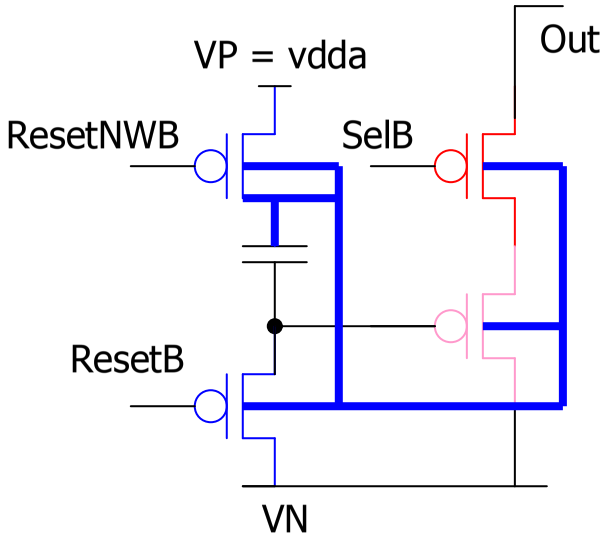
Hit


Out
vdd
N-Wanne
P-Substrat

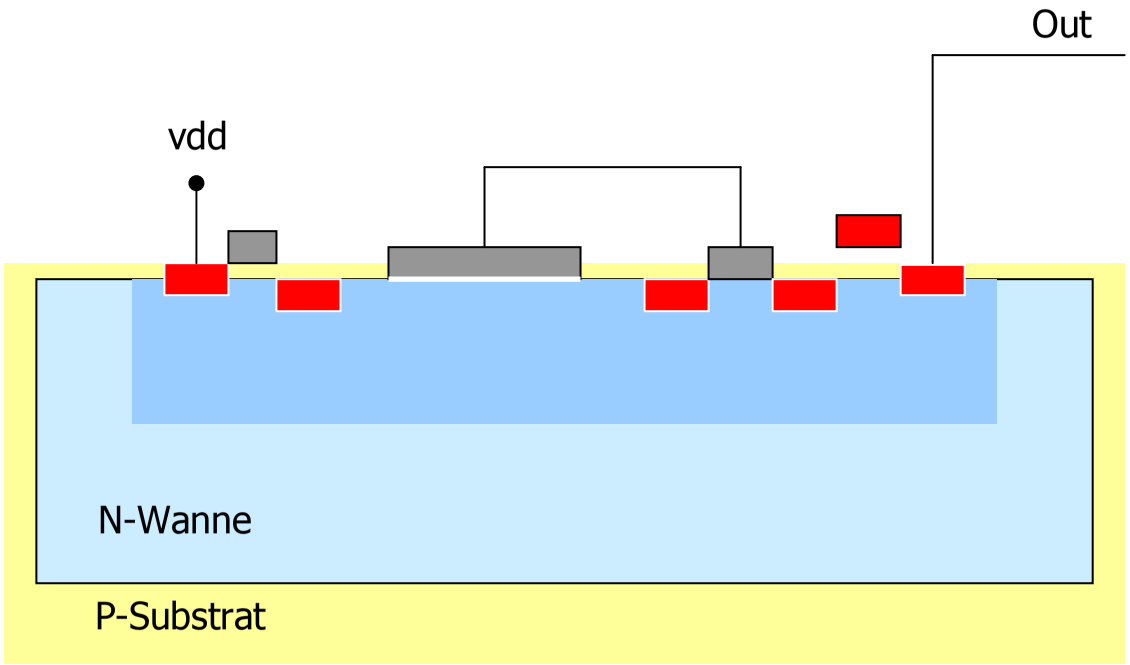

VP = vdda
Out
ResetNWB
SelB
ResetB
VN

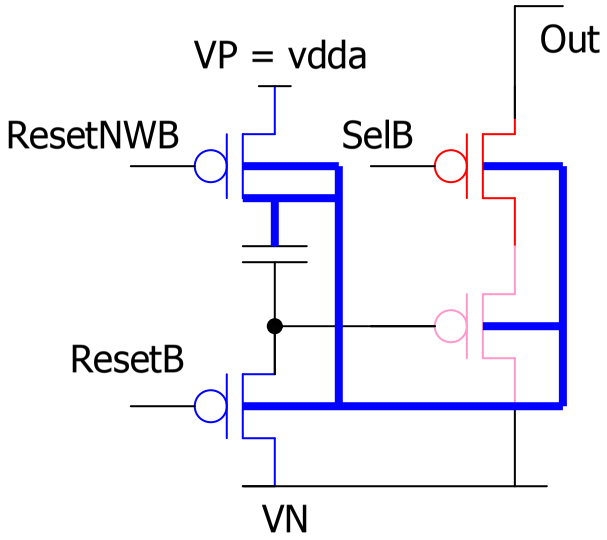
Charge collection



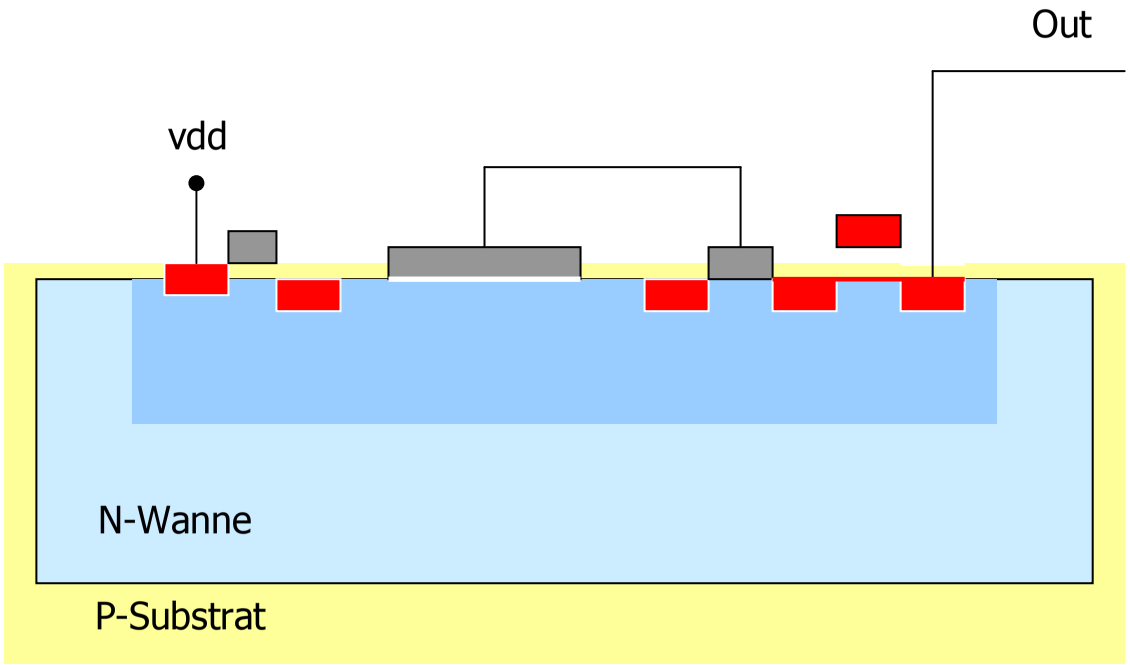


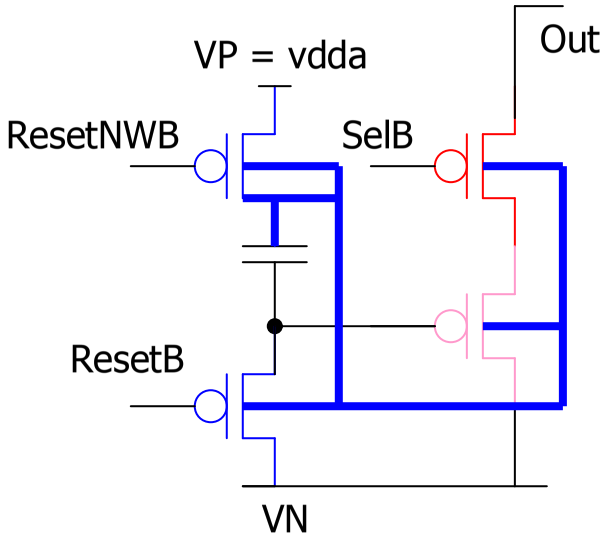
Signal readout



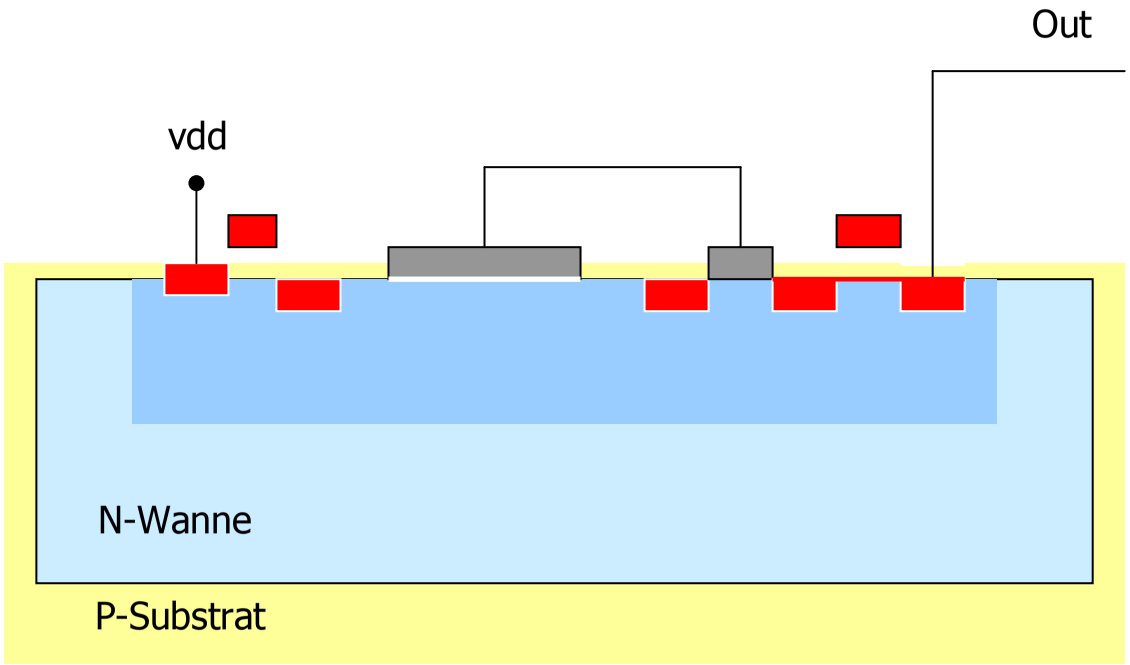


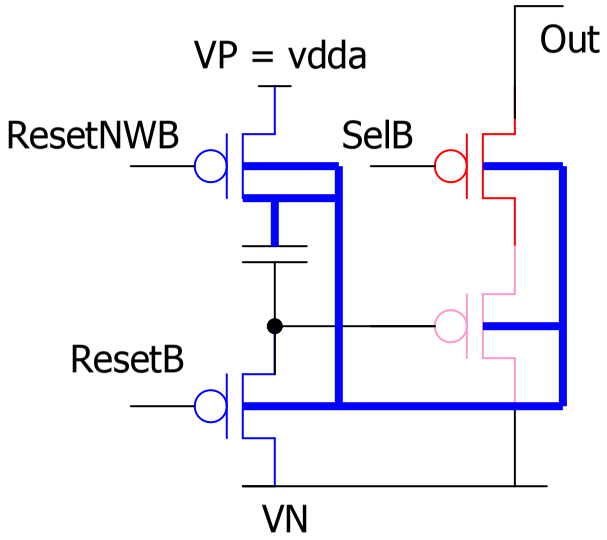
Signal readout



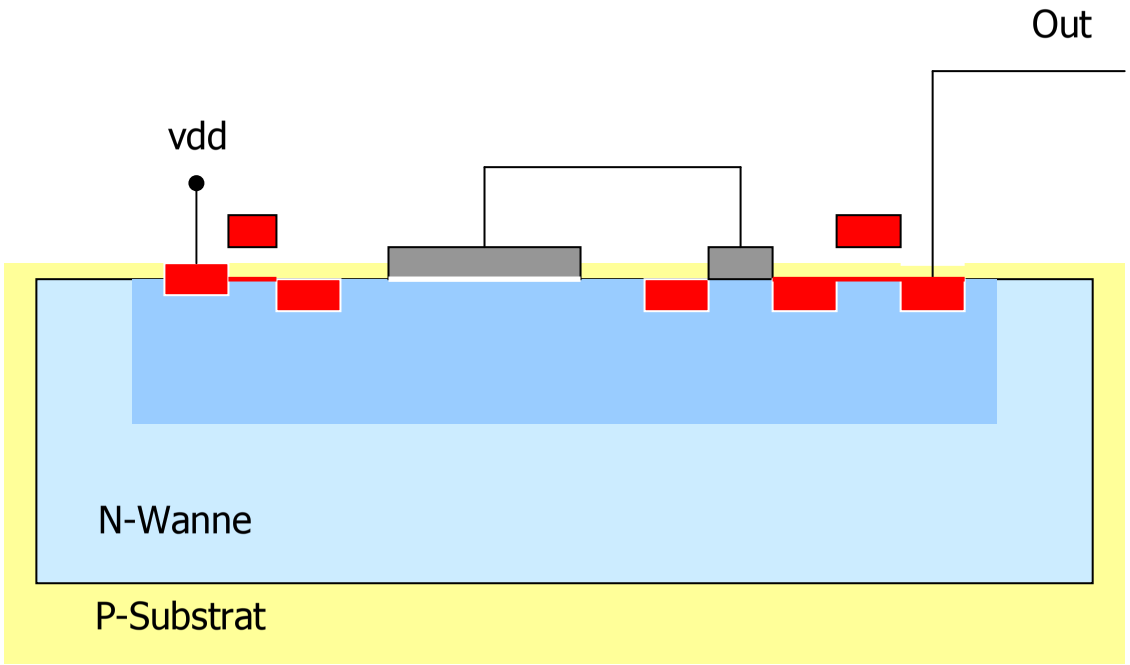


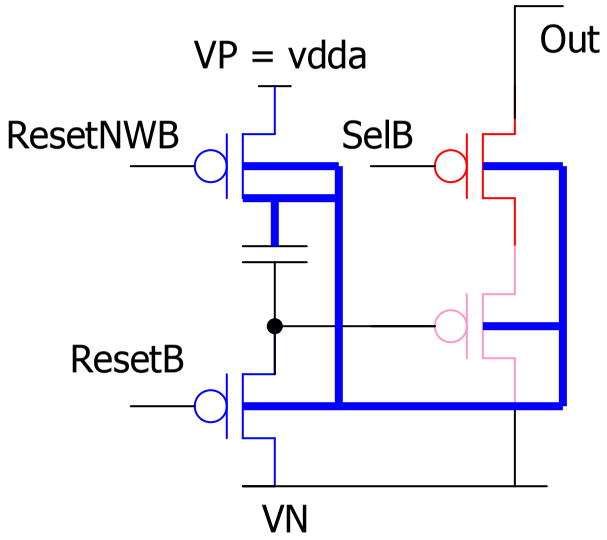
Reset


Out
vdd
N-Wanne
P-Substrat

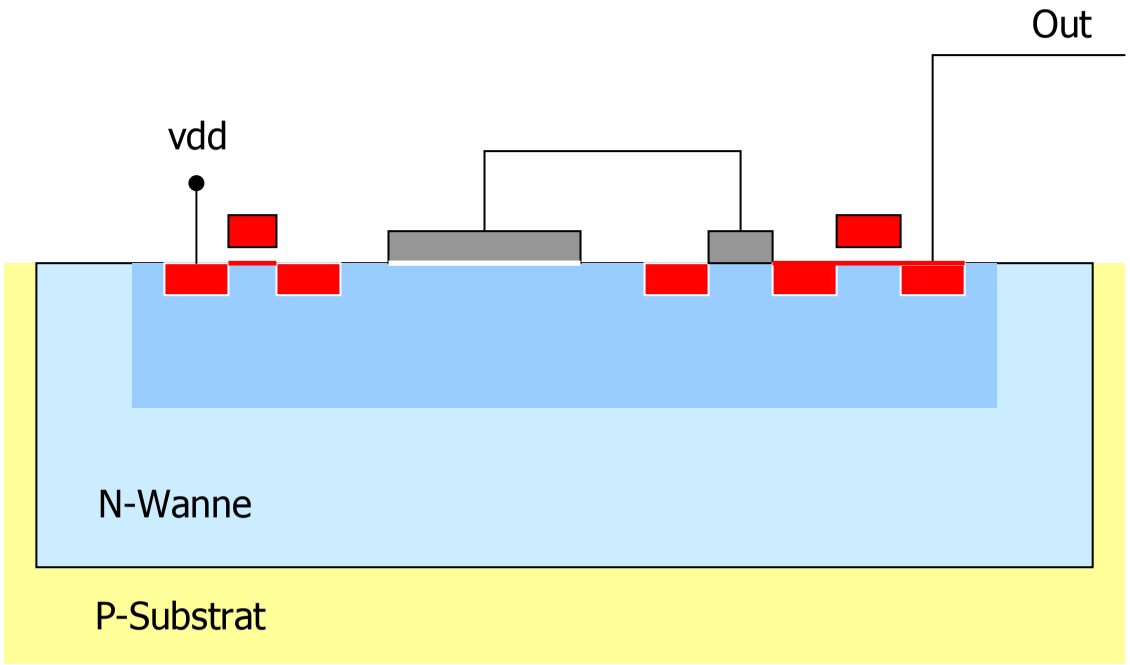

VP = vdda
Out
ResetNWB
SelB
ResetB
VN

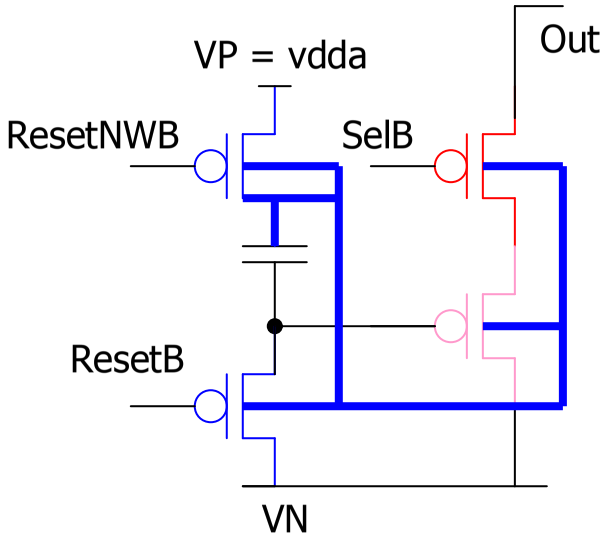
Reset


Out
vdd
N-Wanne
P-Substrat

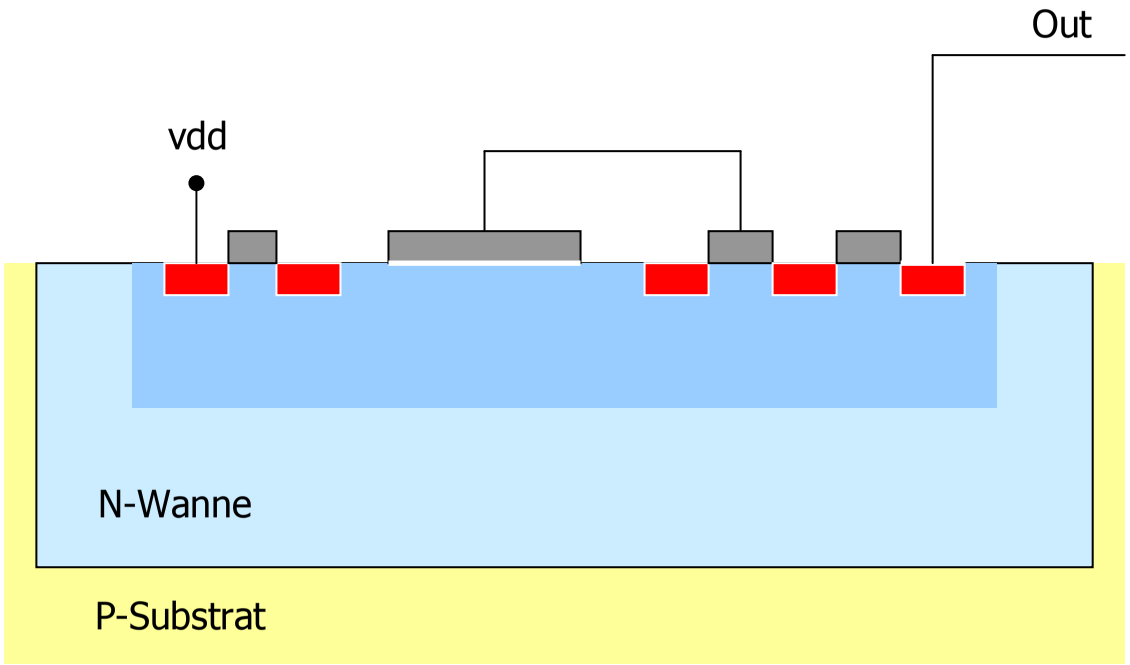

VP = vdda
Out
ResetNWB
SelB
ResetB
VN

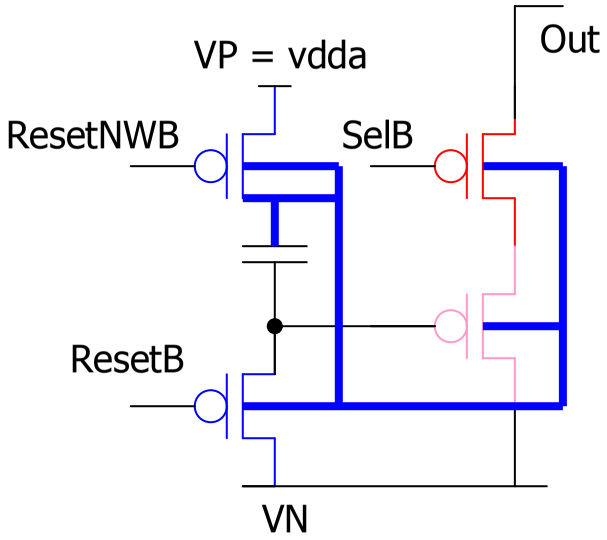
Reset + offset readout



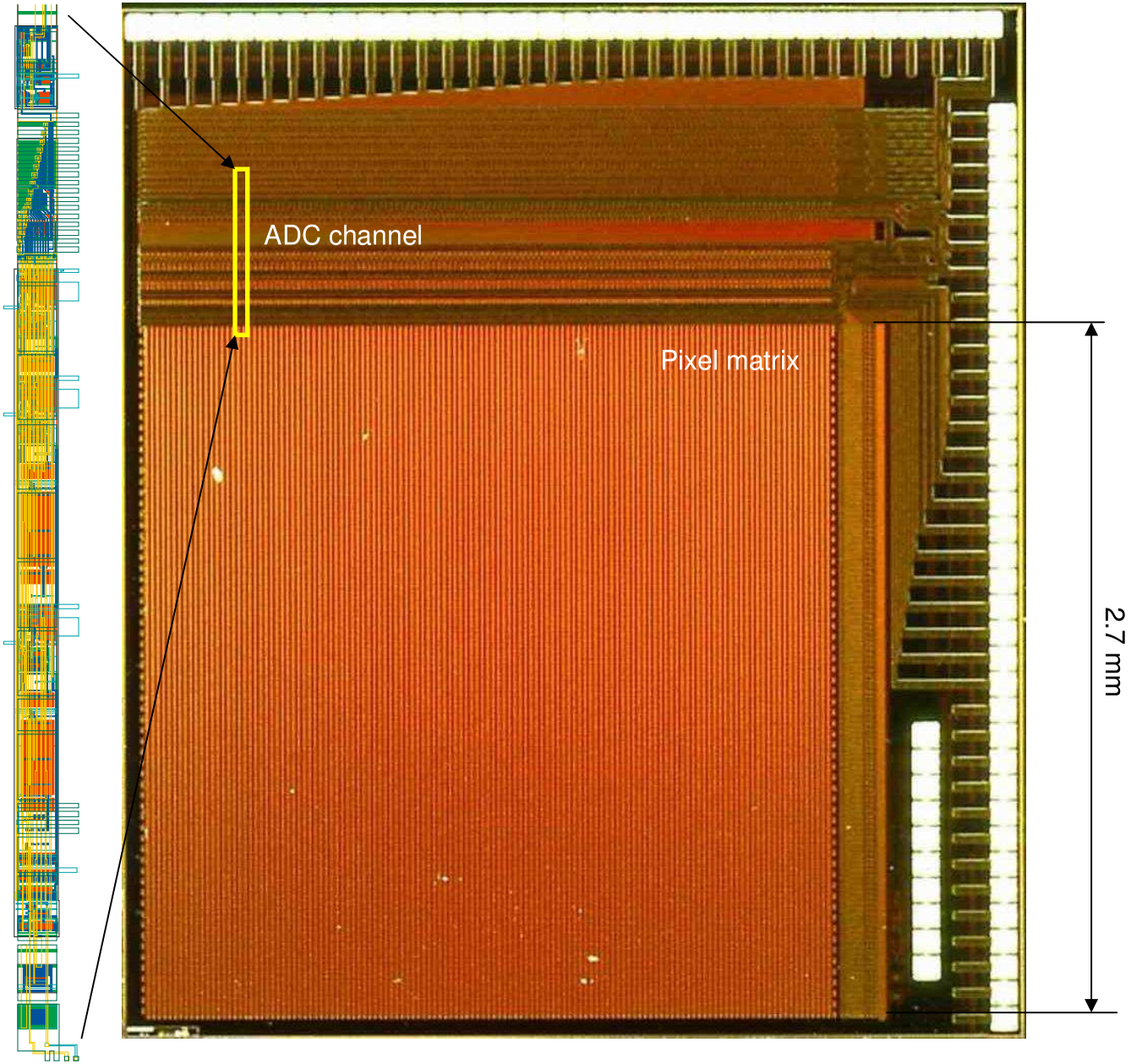


End of readout

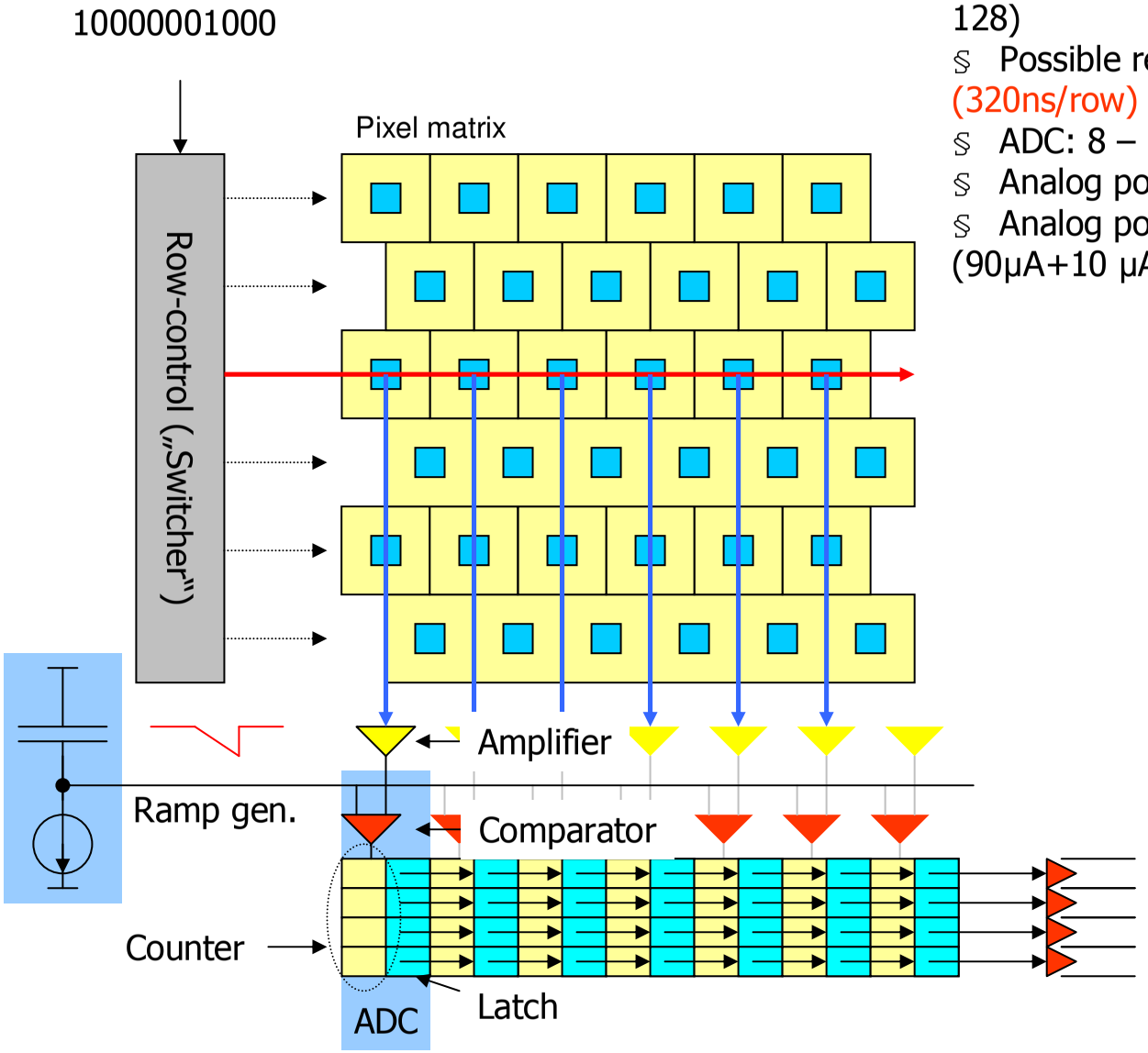




SDS with frame readout – HVM chip

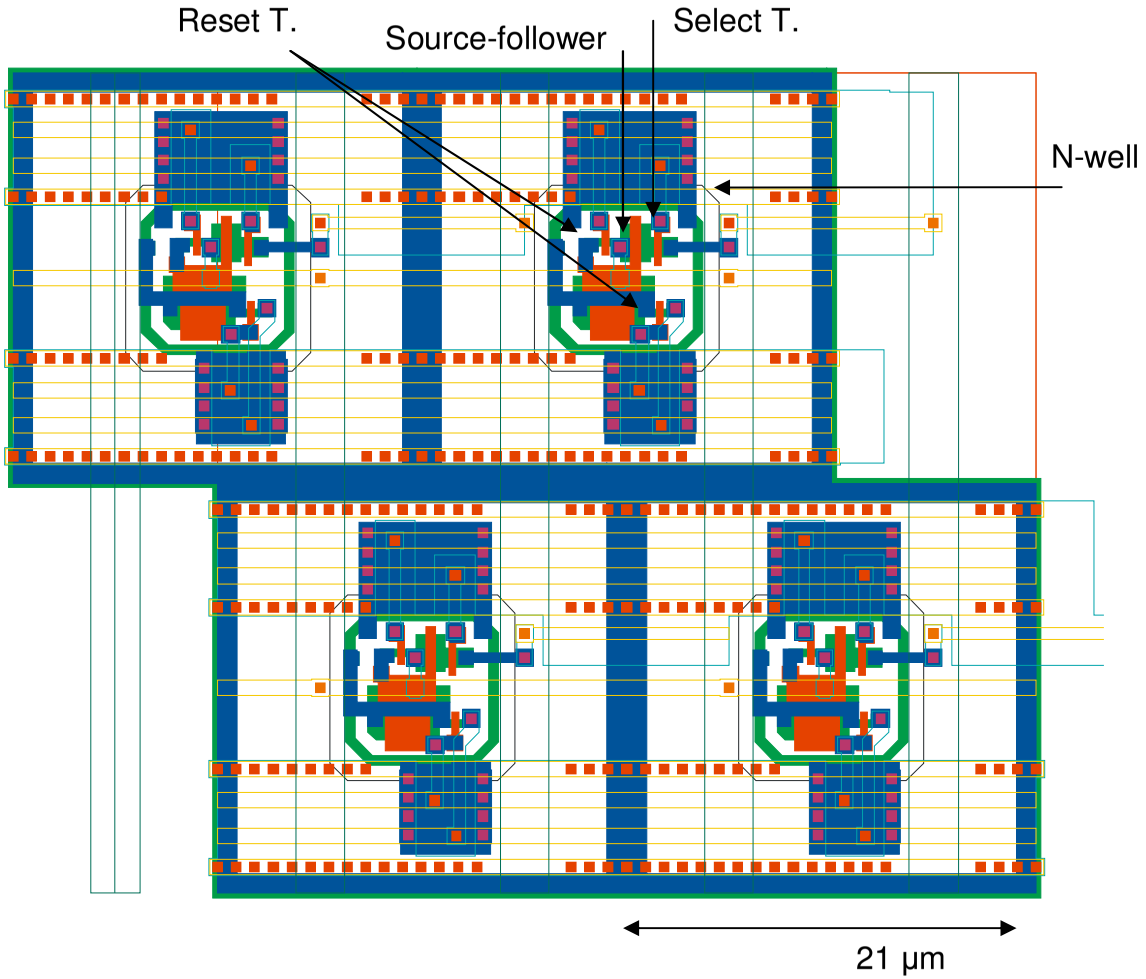


HVM chip structure



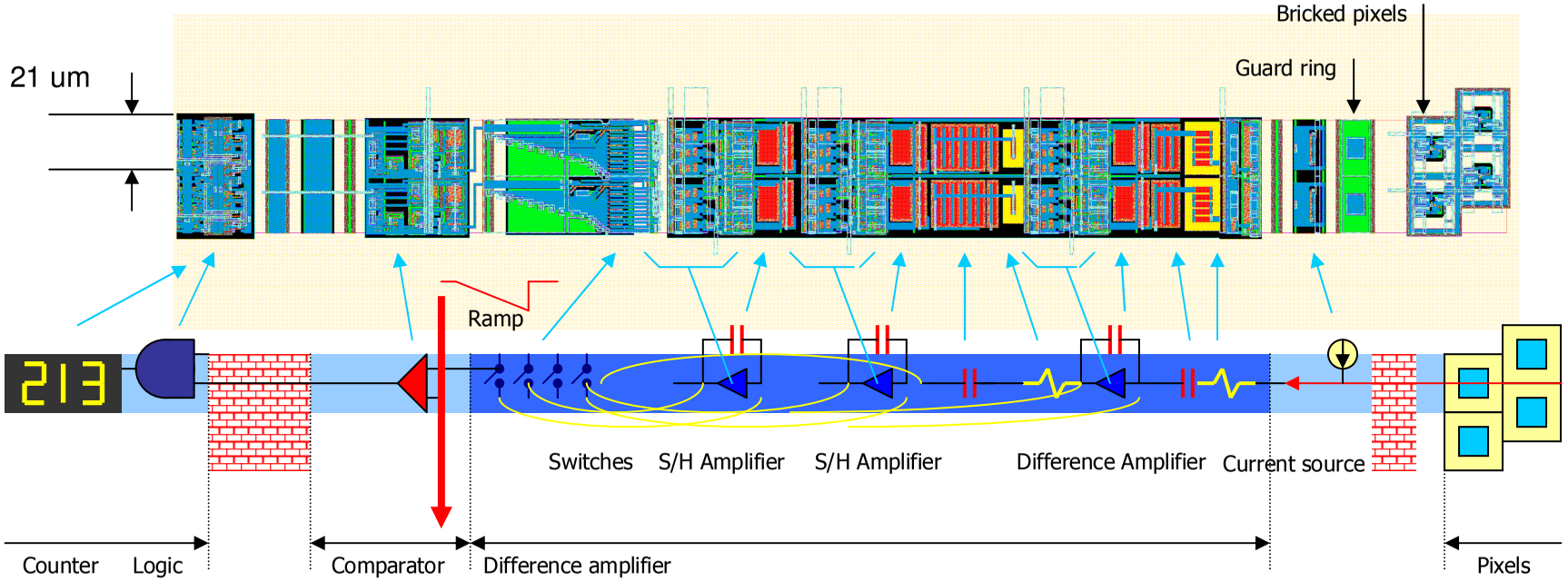
- Pixel size: 21 X 21 µm
- Matrix size: 2.69 X 2.69 mm (128 X 128)
- Possible readout time/matrix: ~ 40 µs (320ns/row) (tested so far 1.28 µs/row)
- ADC: 8 – Bit
- Analog power: 54.9mW (7.63mW/mm^2)
- Analog power: ADC: 0.363mW/ADC (90µA+10 µA)

HVM pixel layout

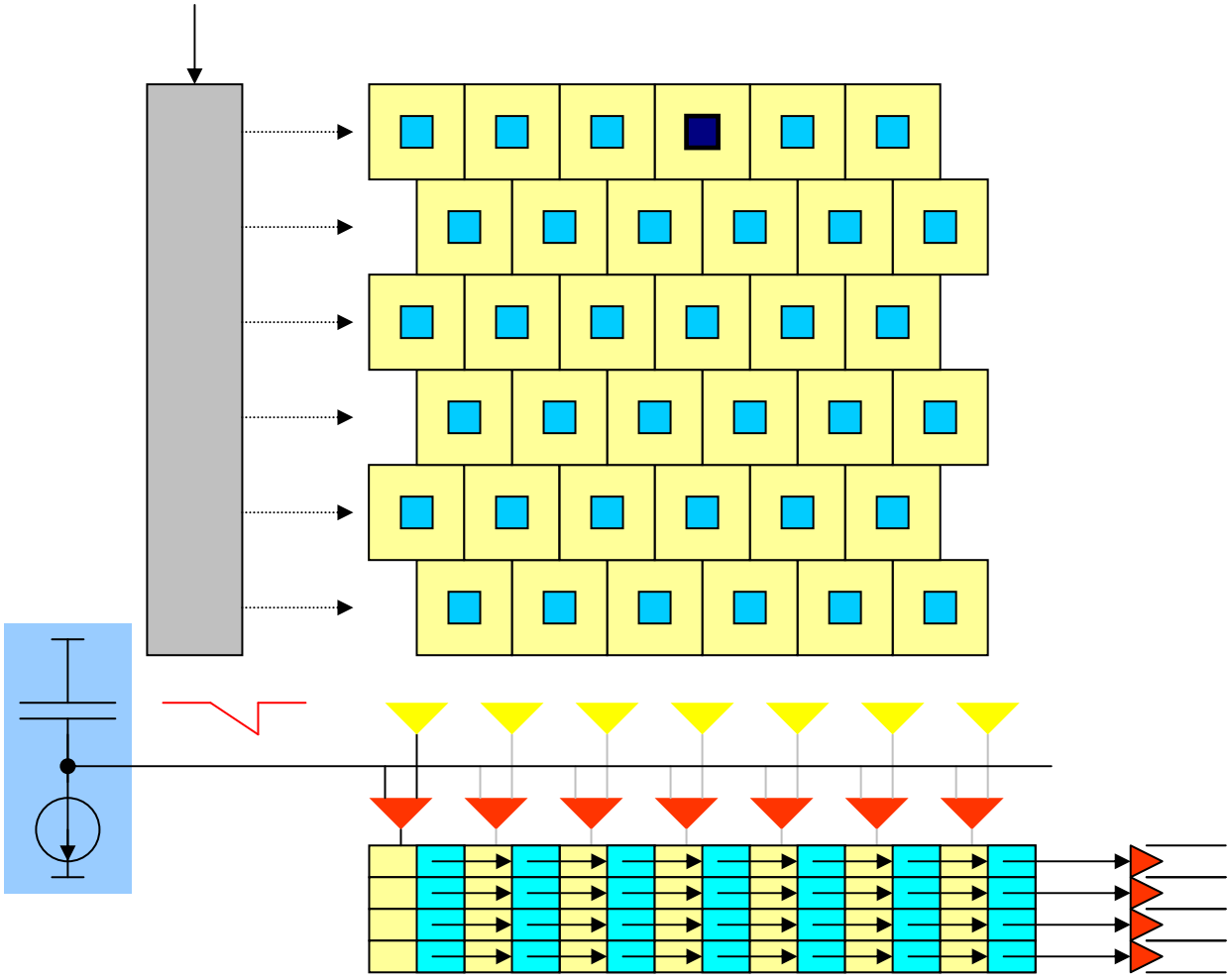


HVM ADC

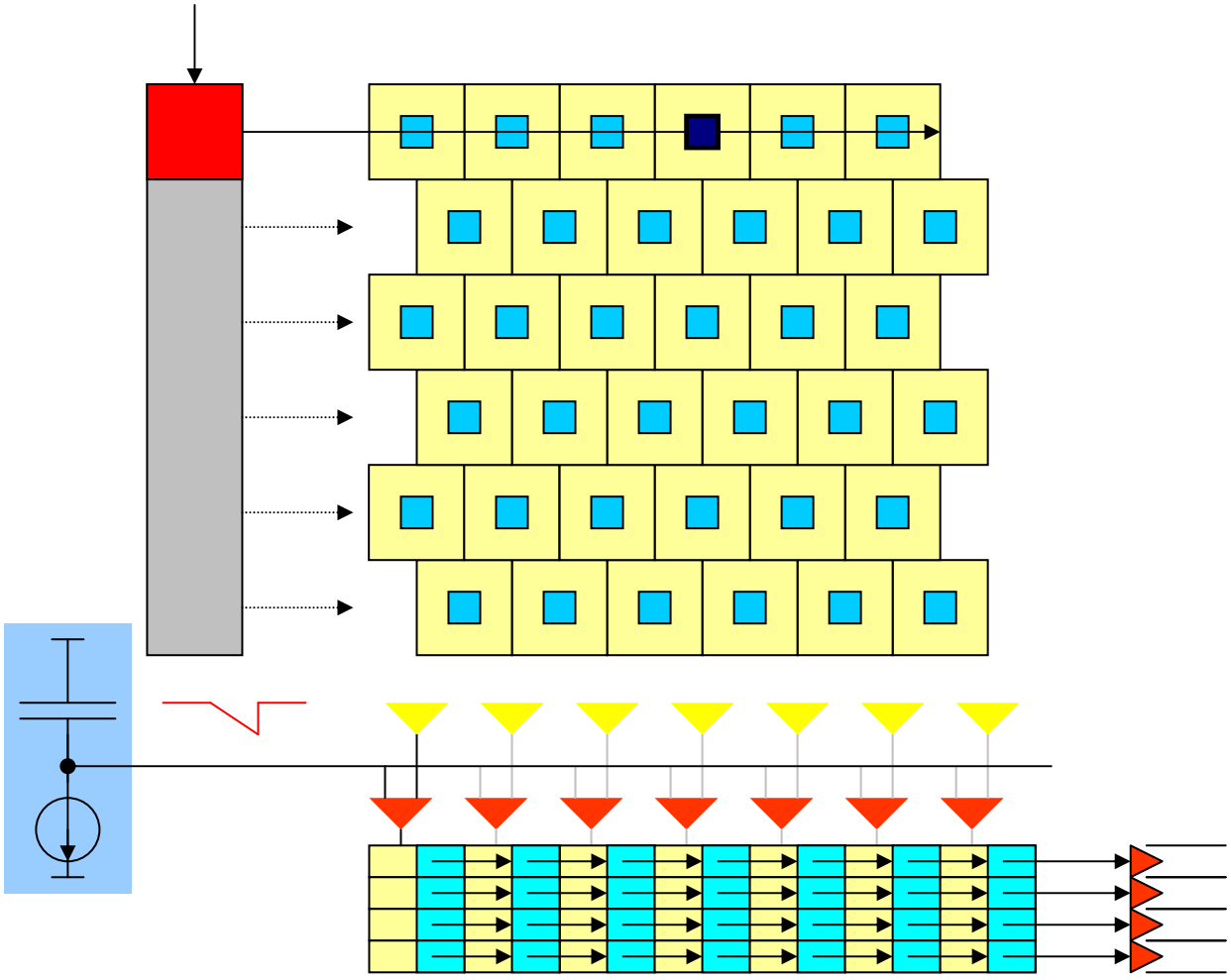
- Switched capacitor amplifier
- Single-slope ADC
- Asynchronous 8-bit counter



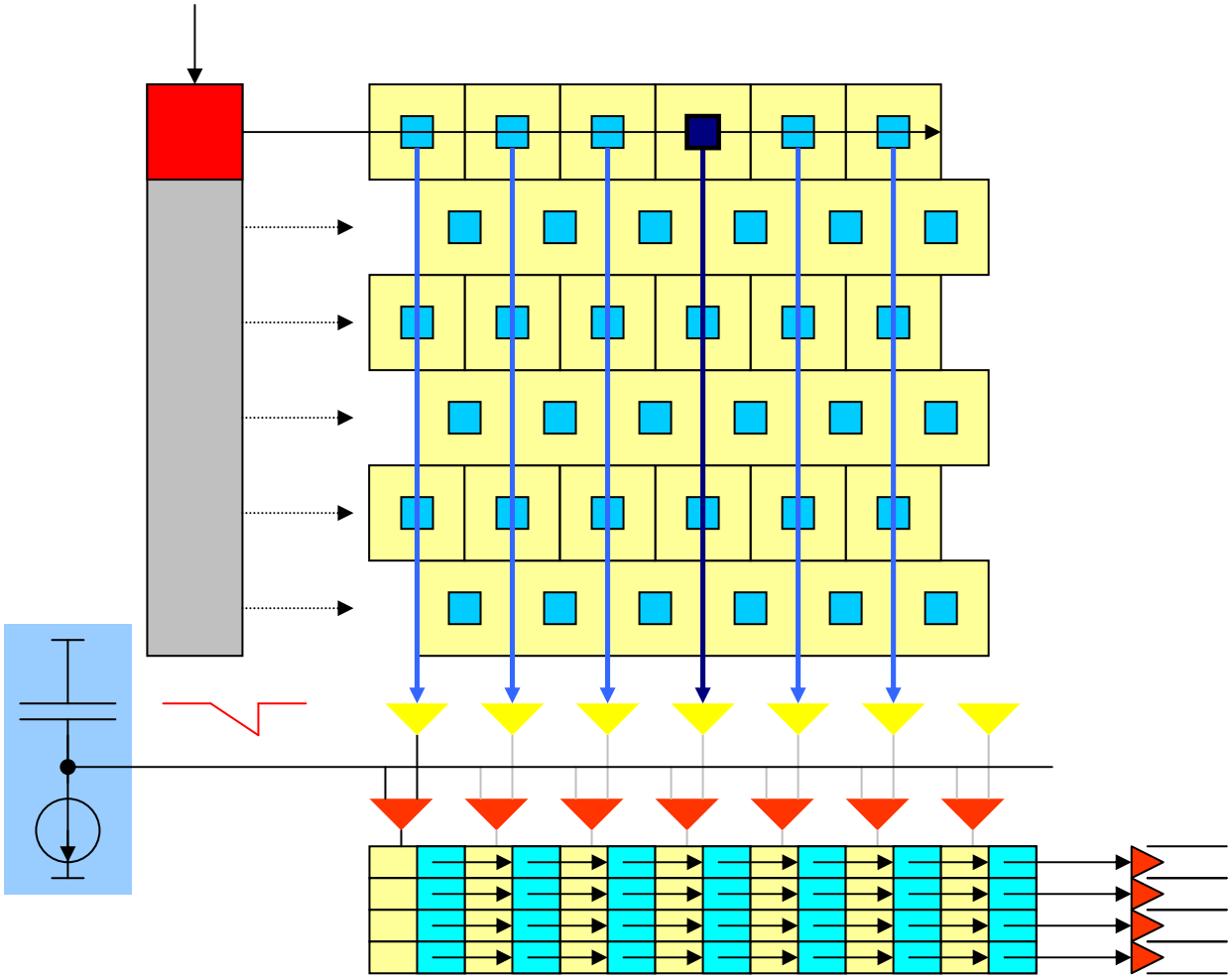
A/D conversion and readout - Start



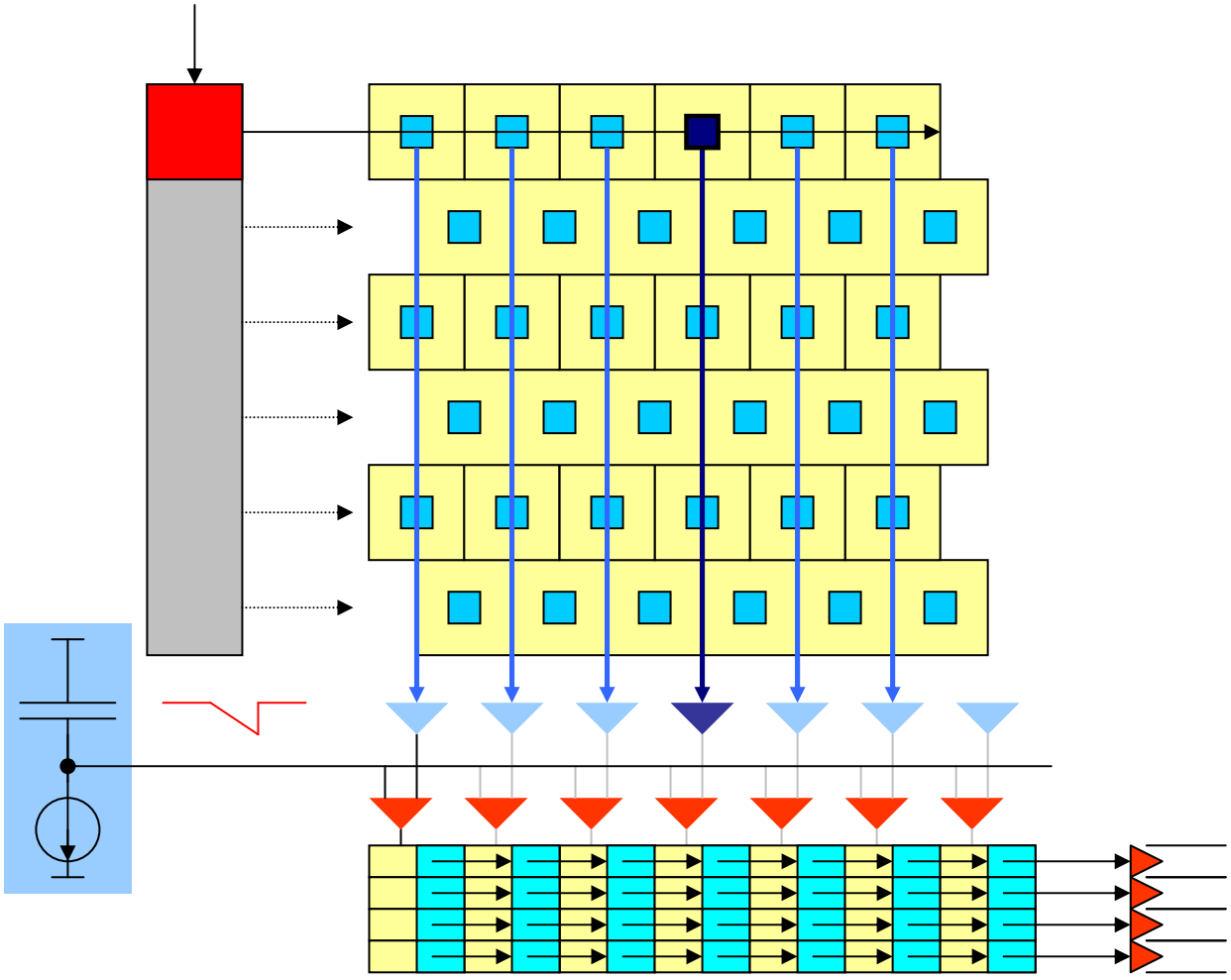
Select row



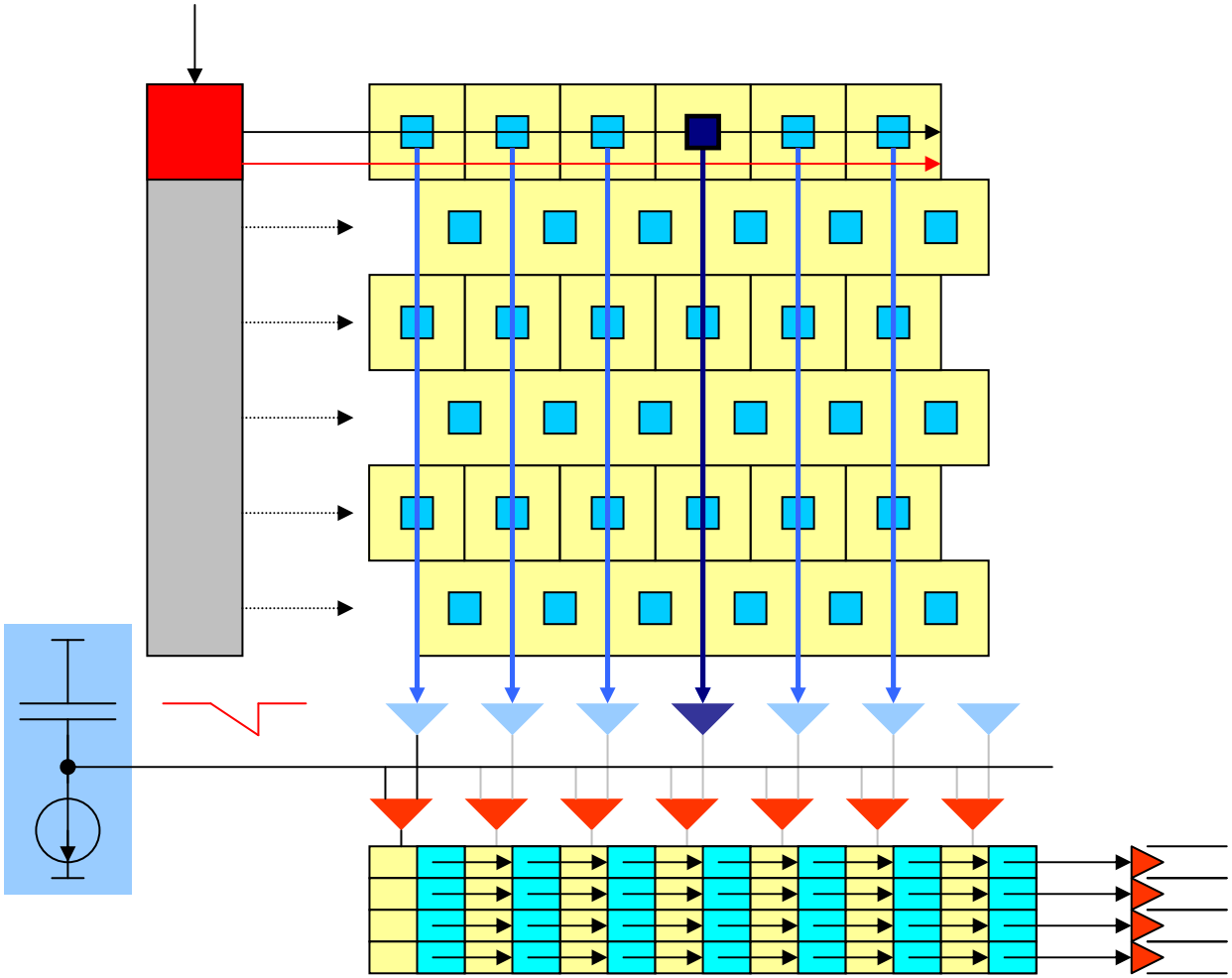
Select row



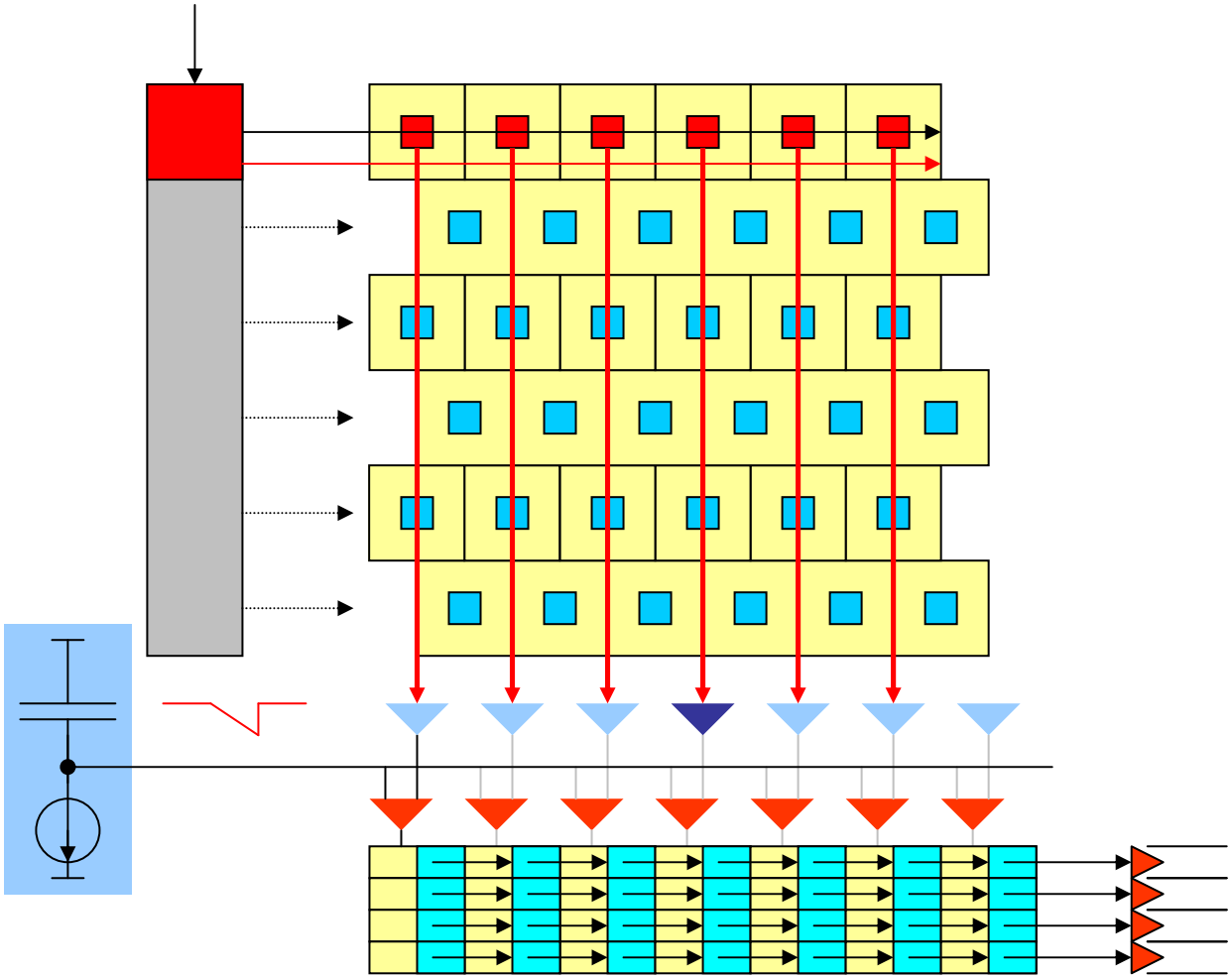
Store signal



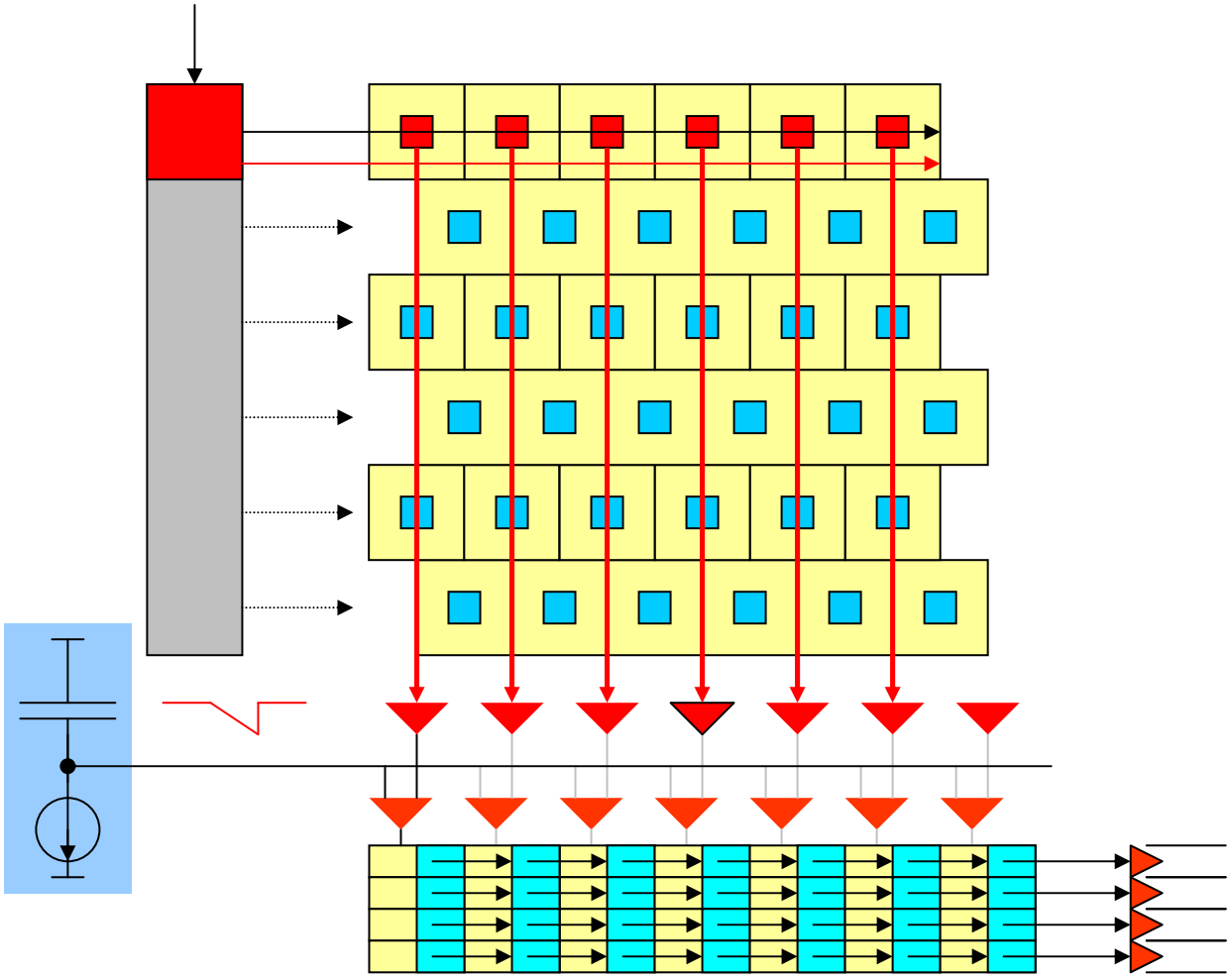
Reset



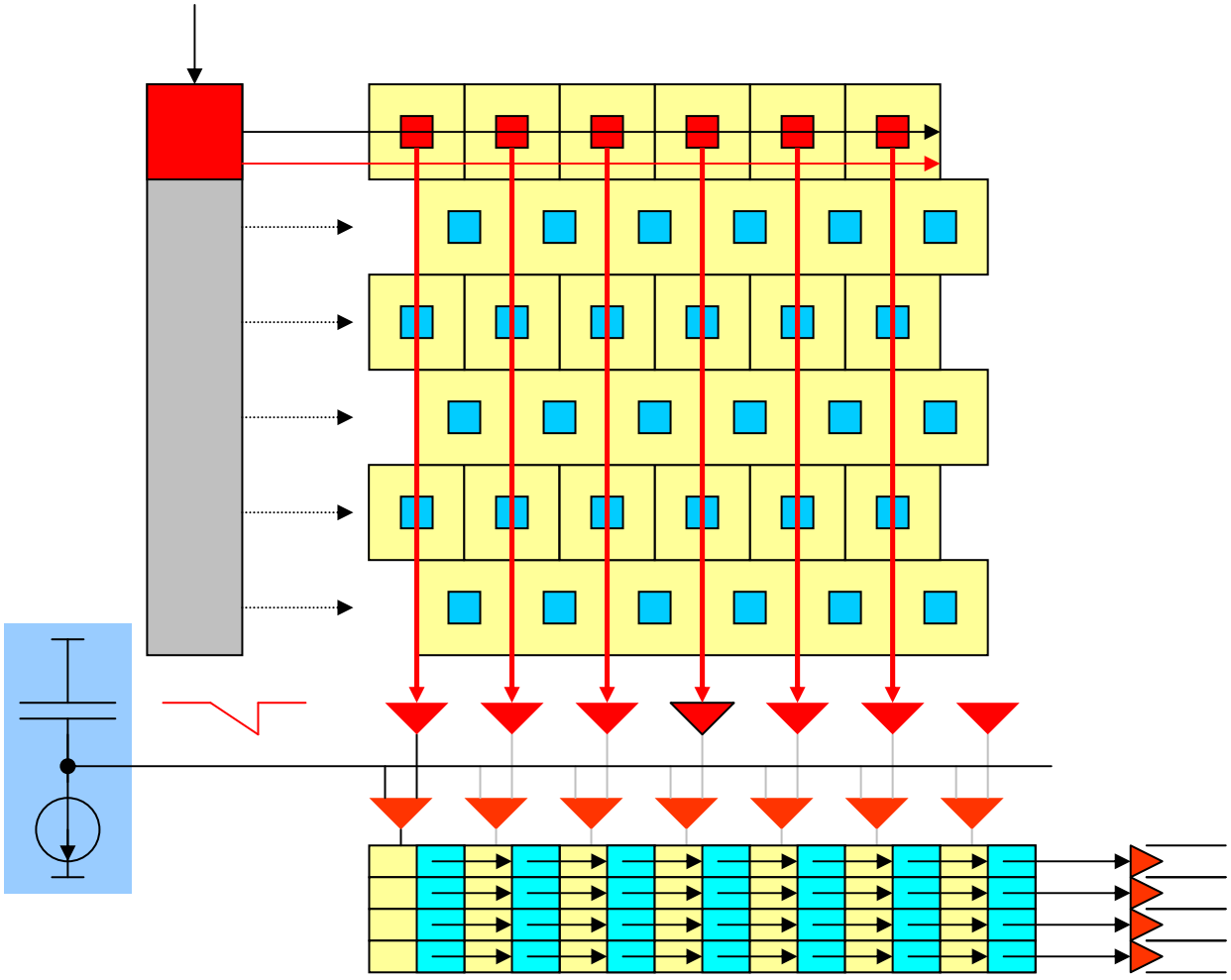
Reset



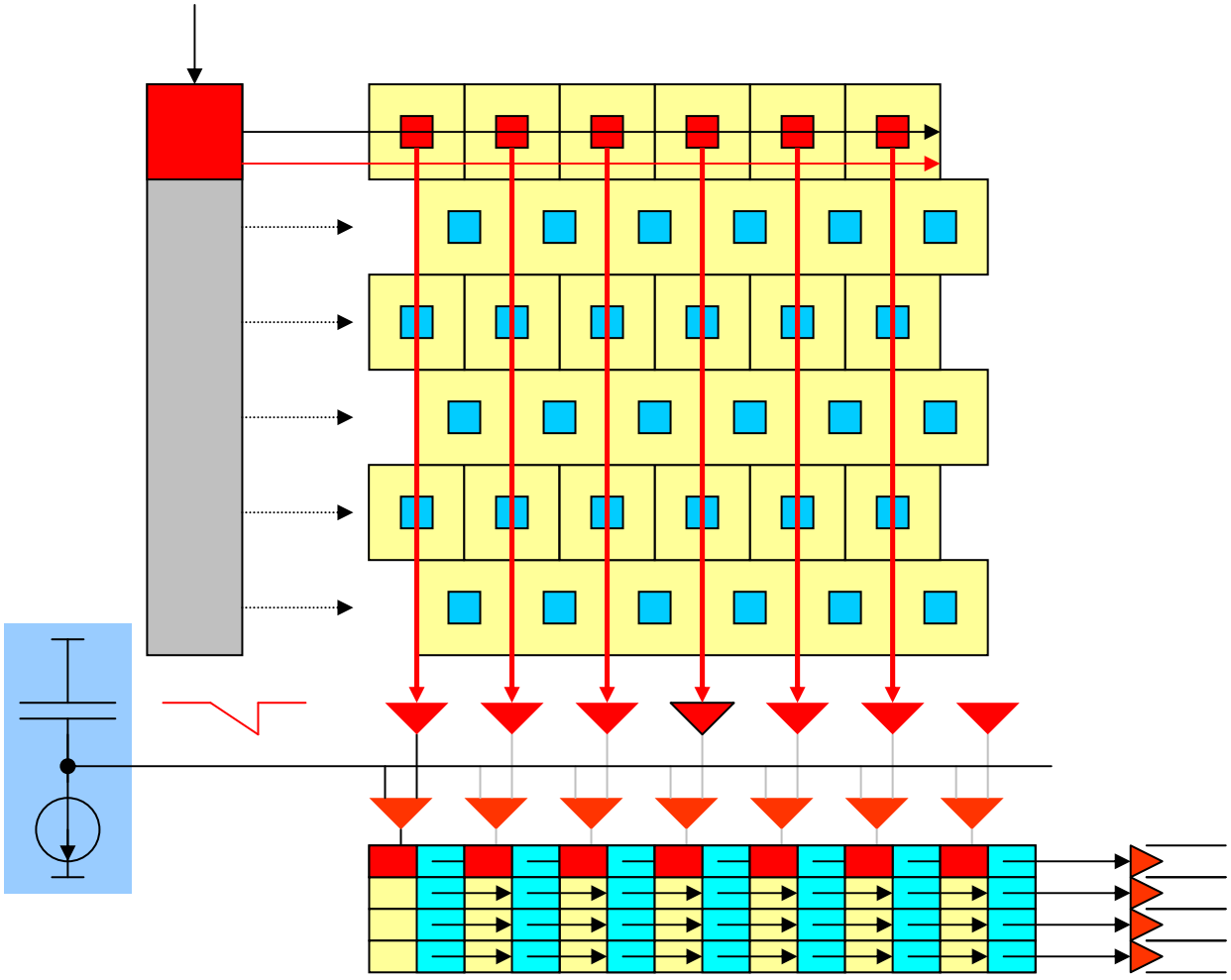
Subtract offset



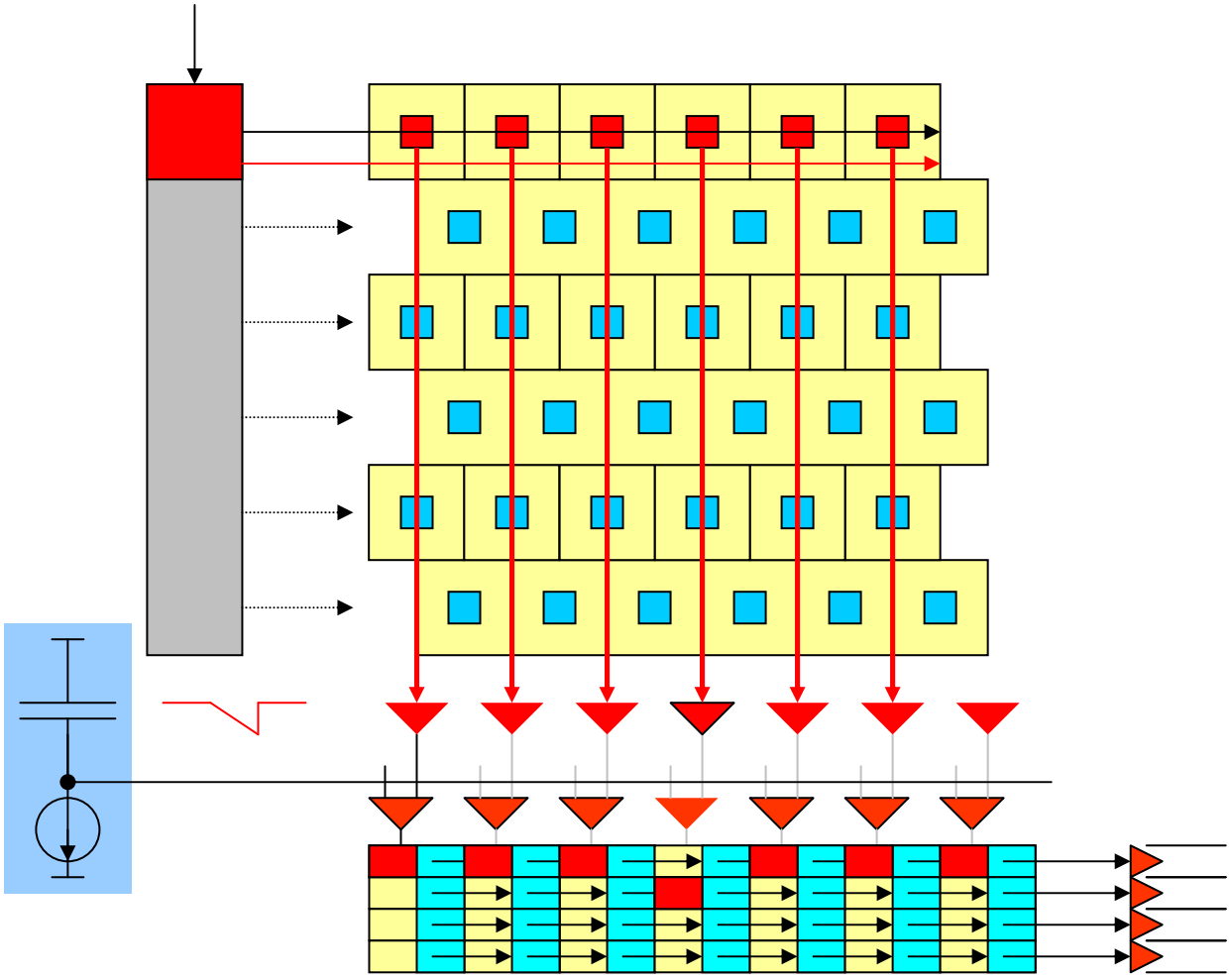
Start conversion



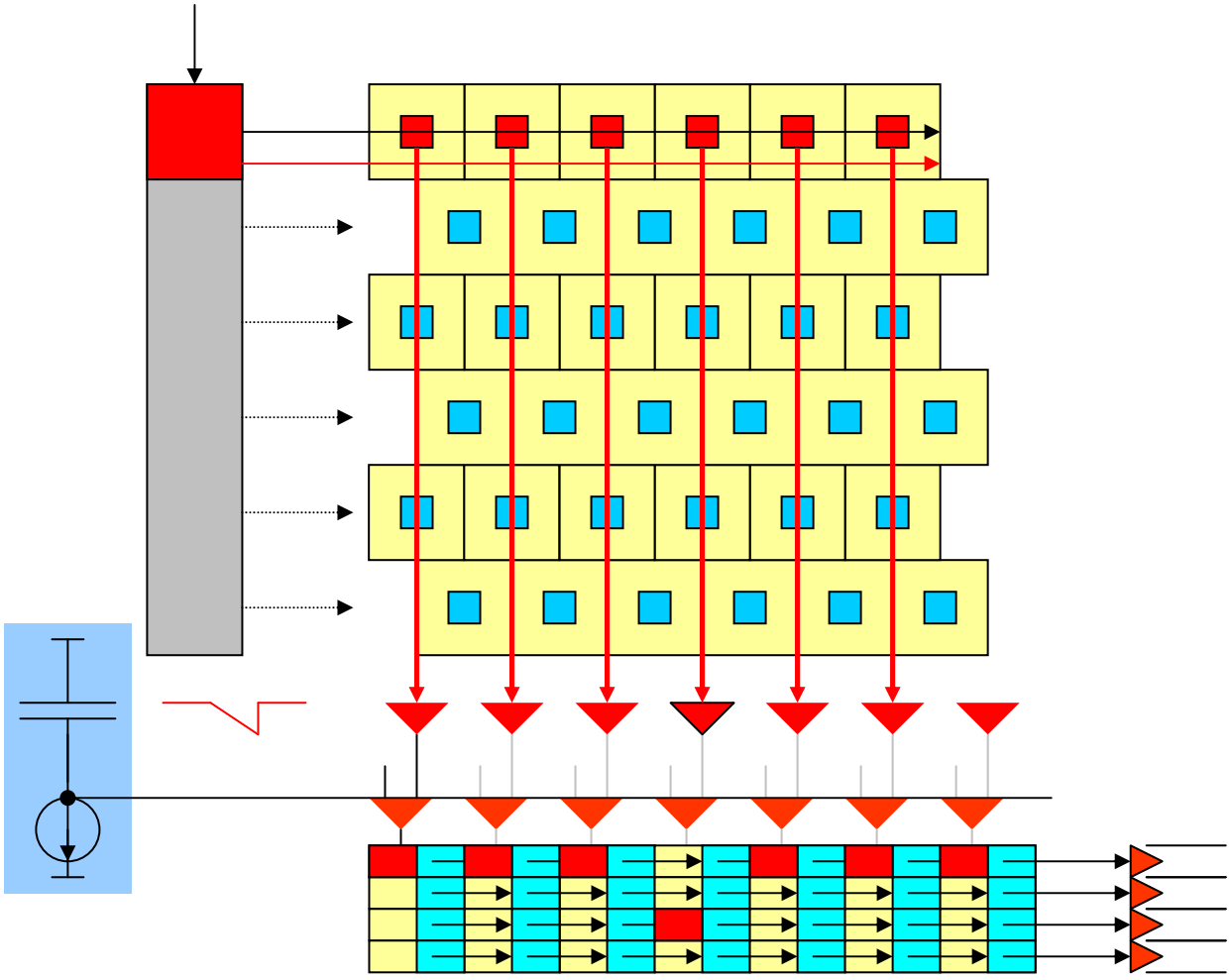
Measure Time and decrease Ramp



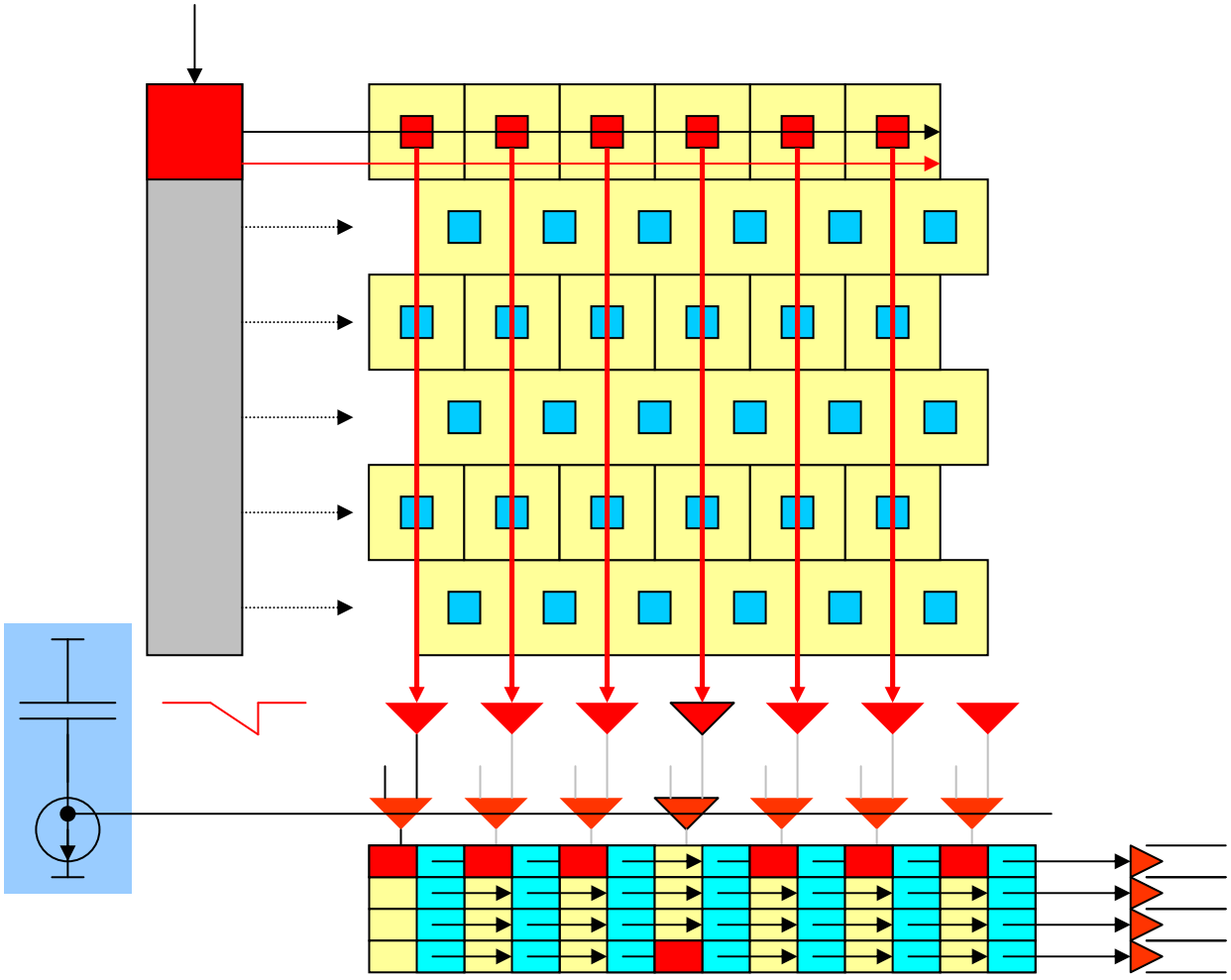
Measure Time and decrease Ramp



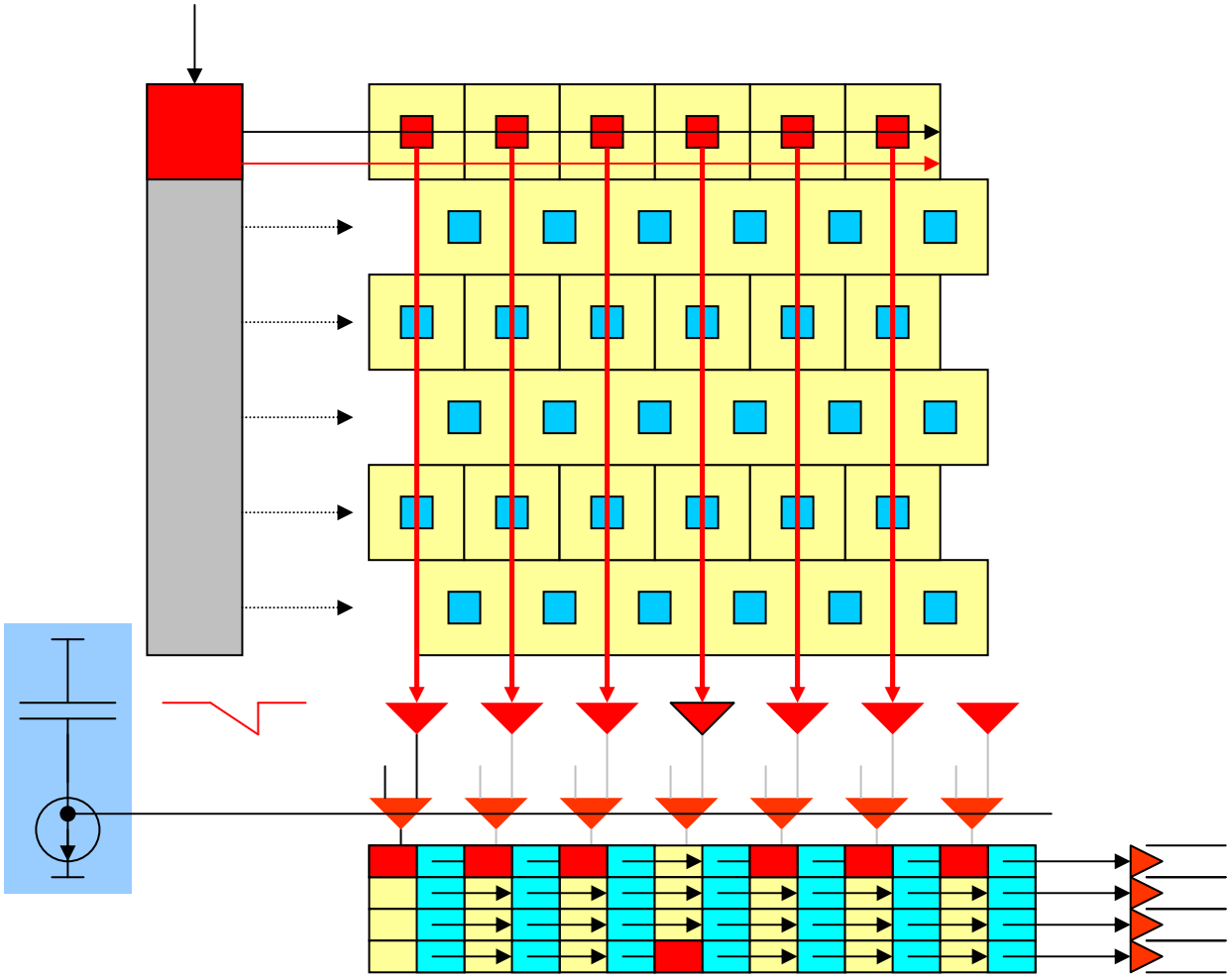
Measure Time and decrease Ramp



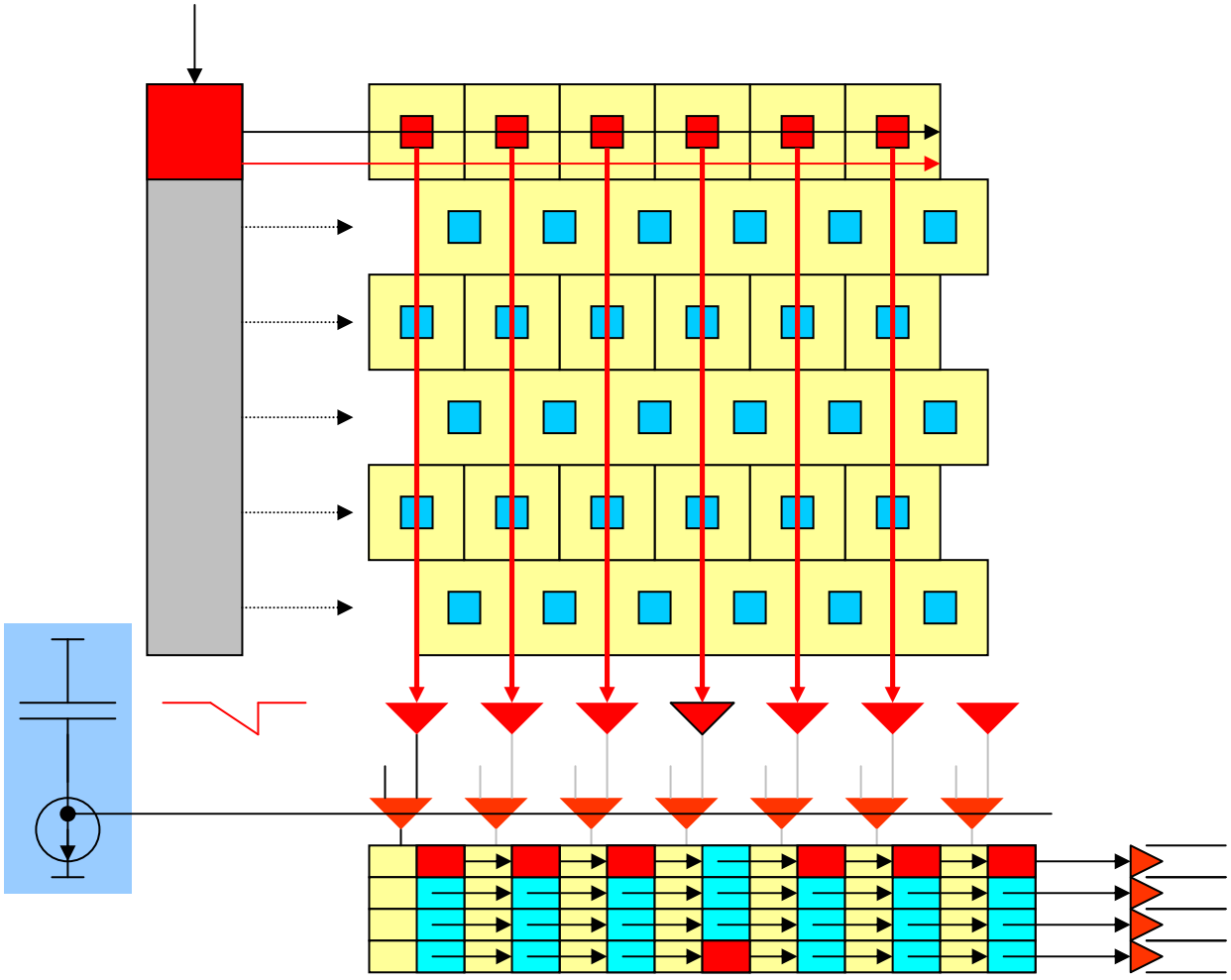
Measure Time and decrease Ramp



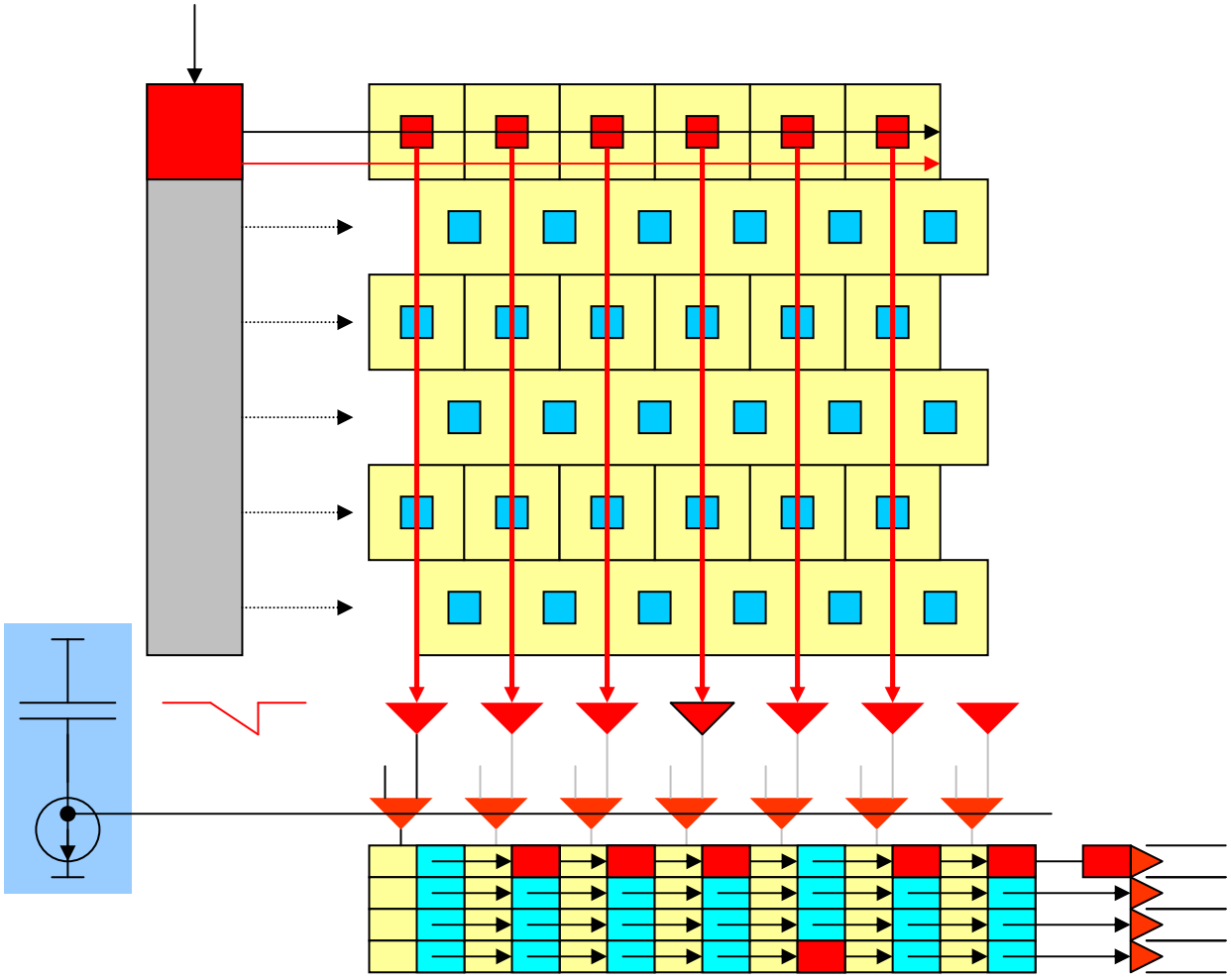
Shift out of time stamps



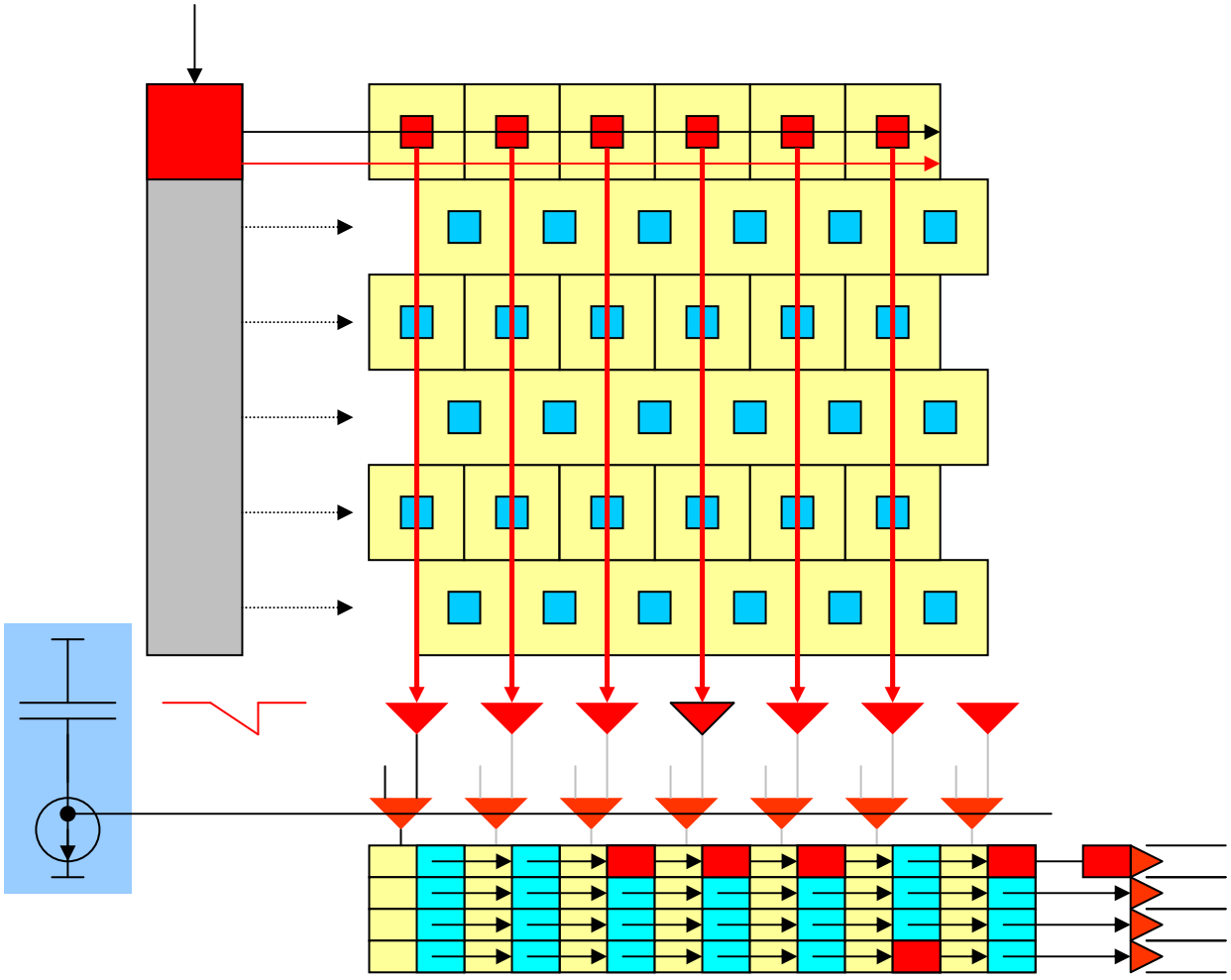
Shift out of time stamps



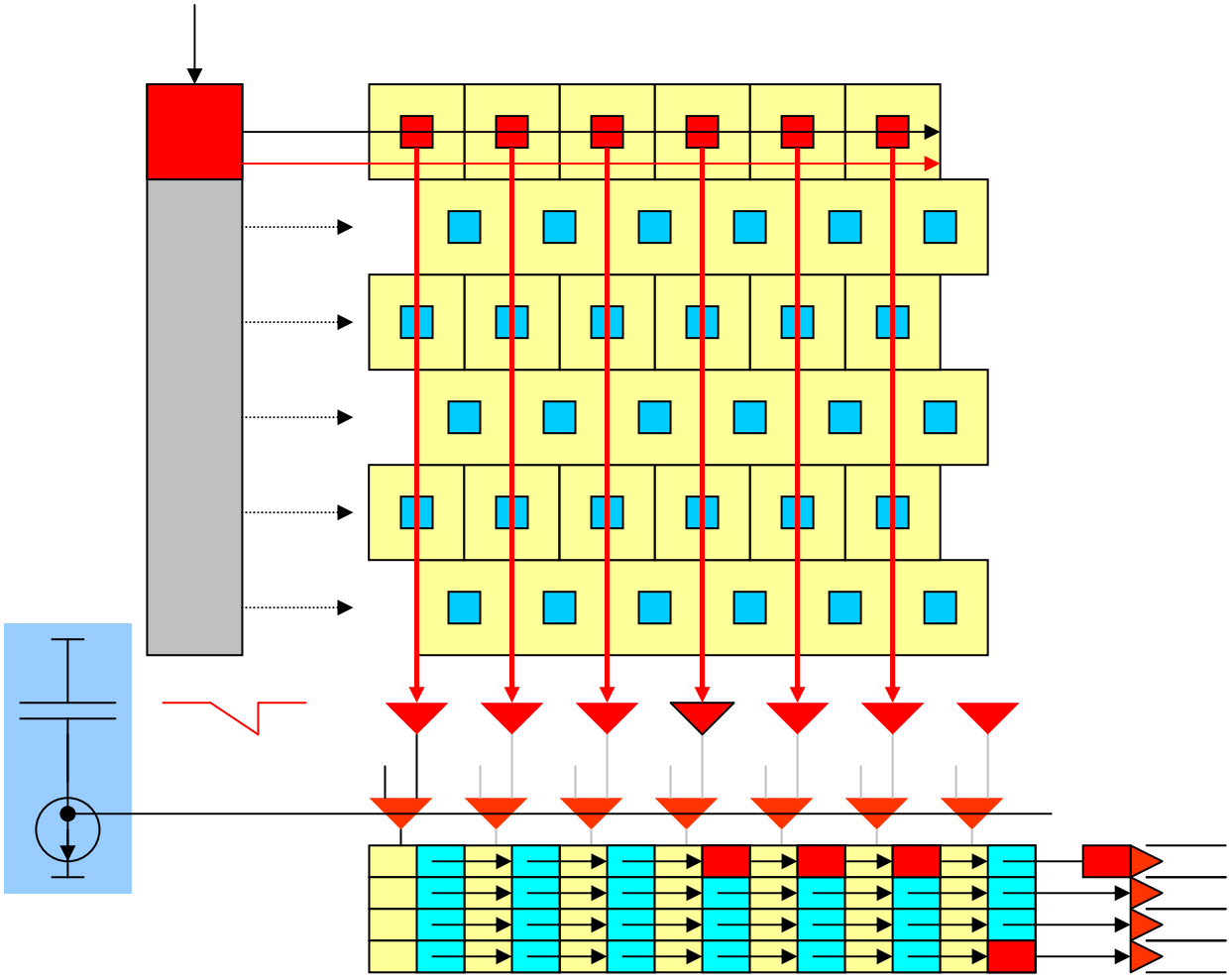
Shift out of time stamps



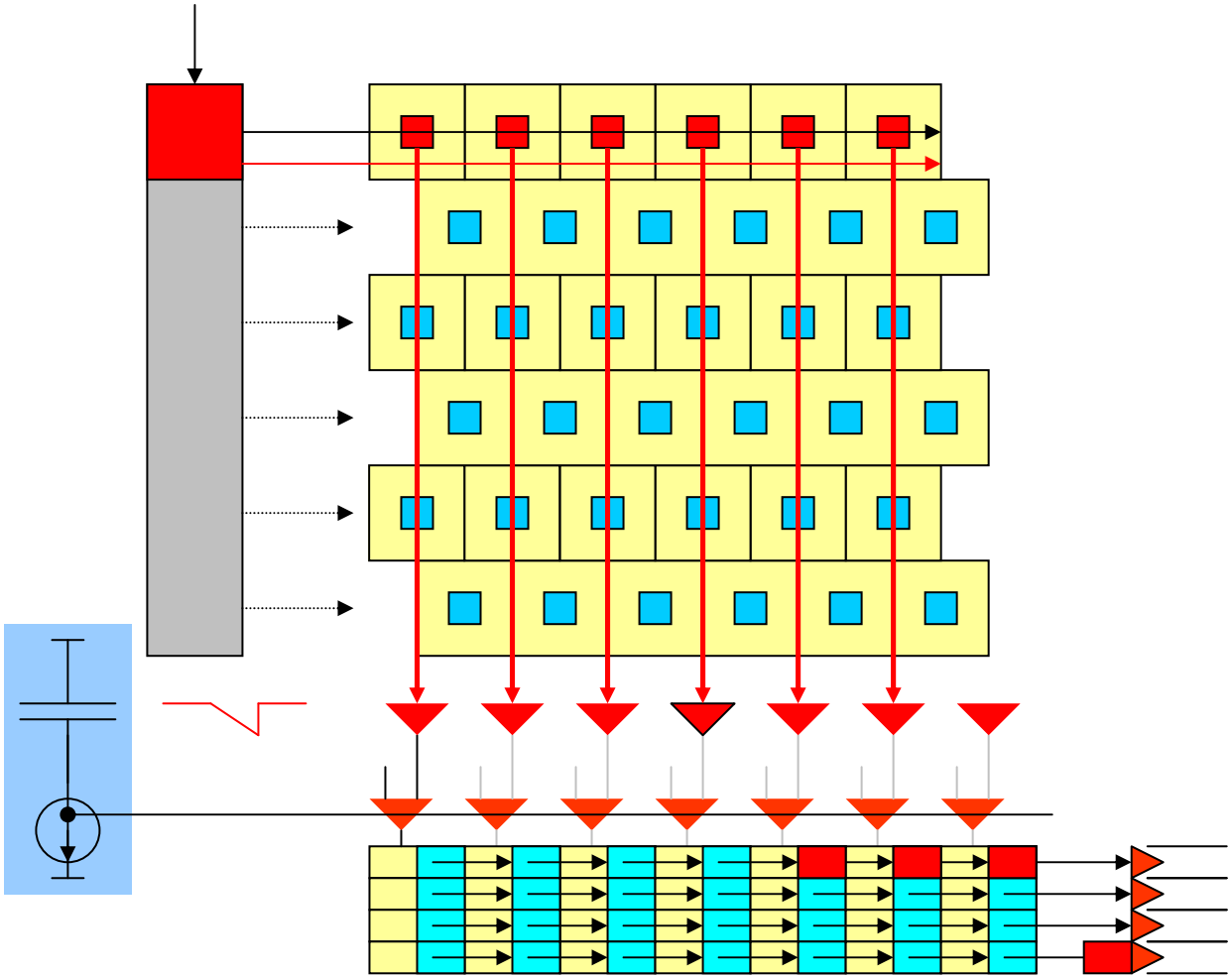
Shift out of time stamps



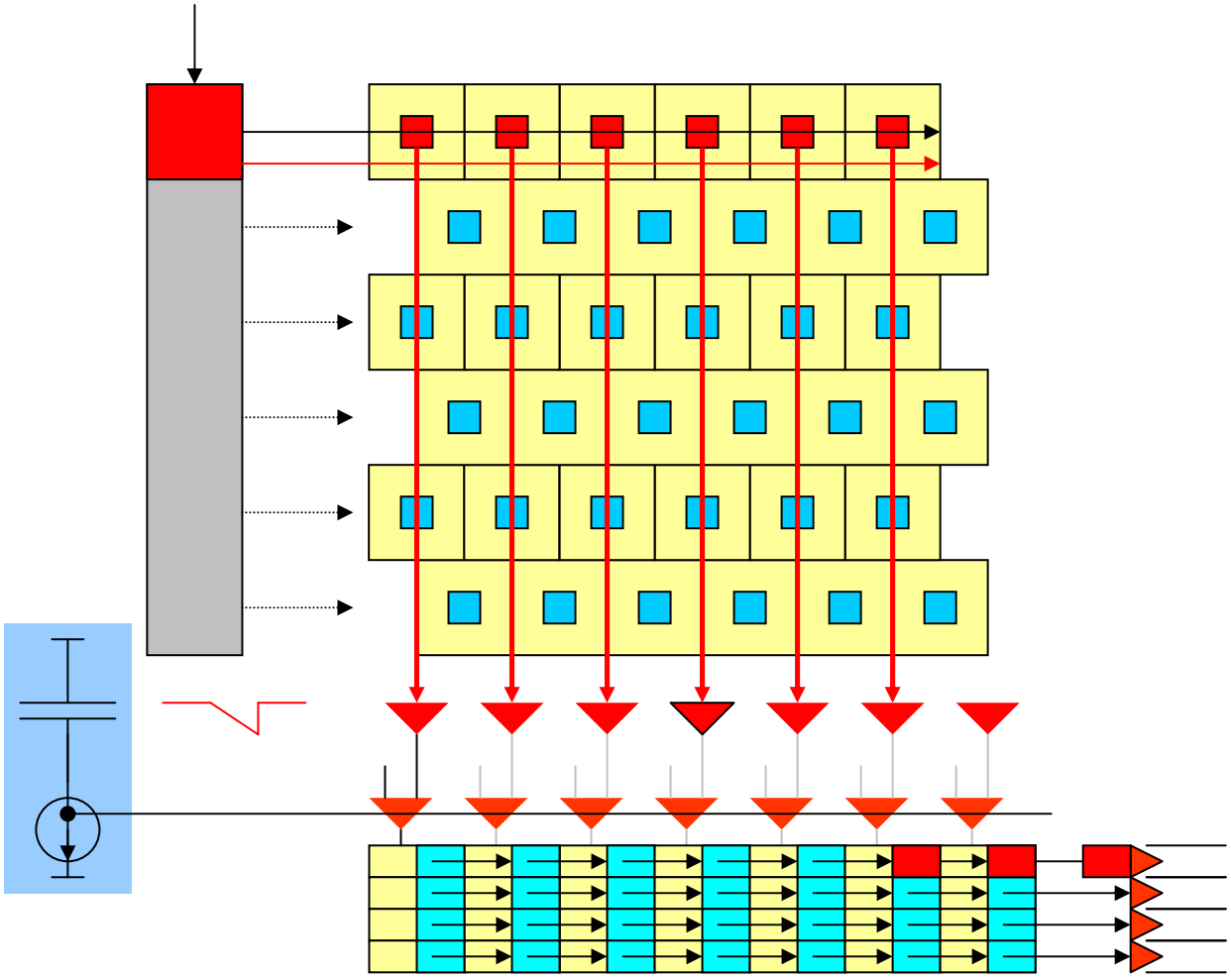
Shift out of time stamps



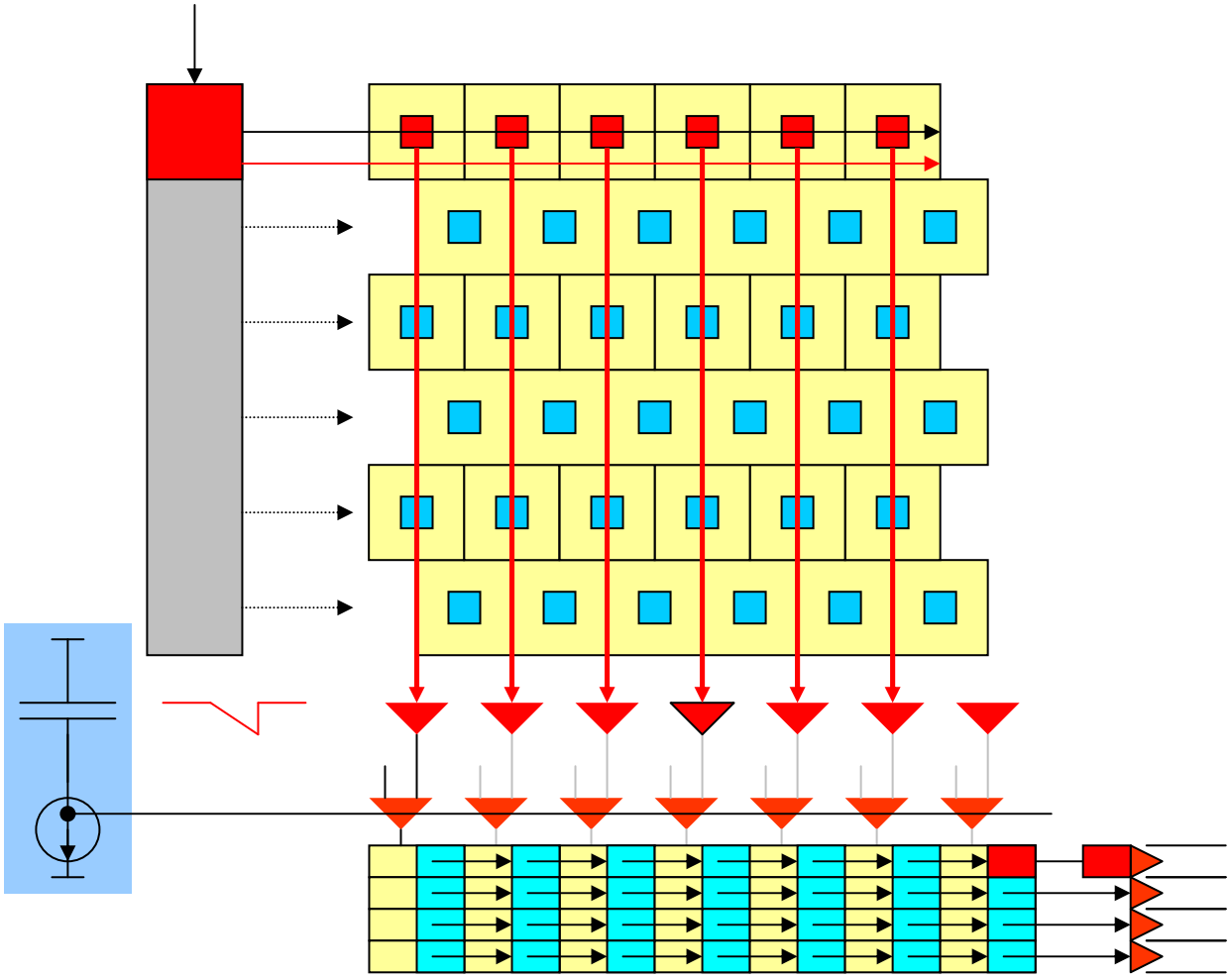
Shift out of time stamps



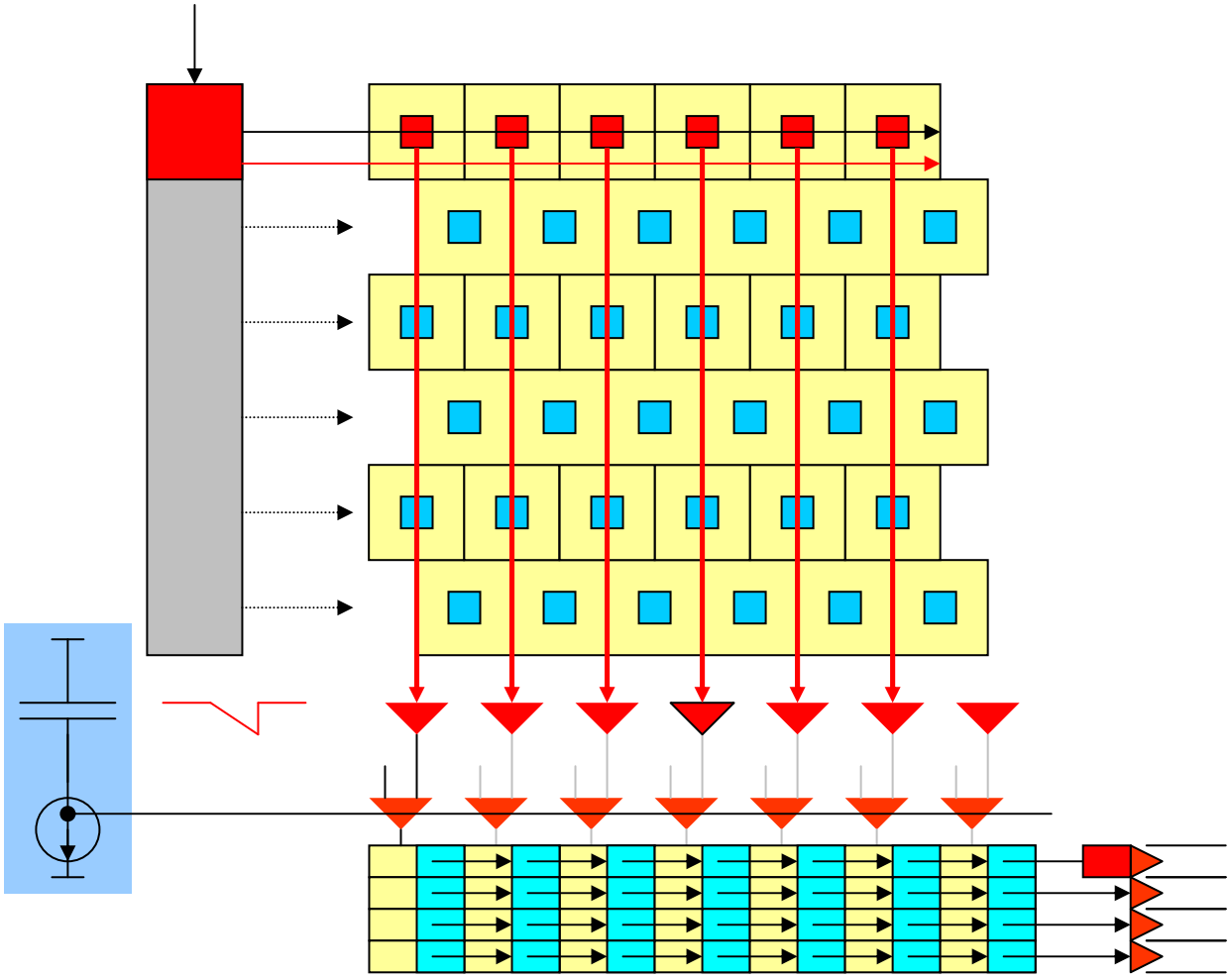
Shift out of time stamps



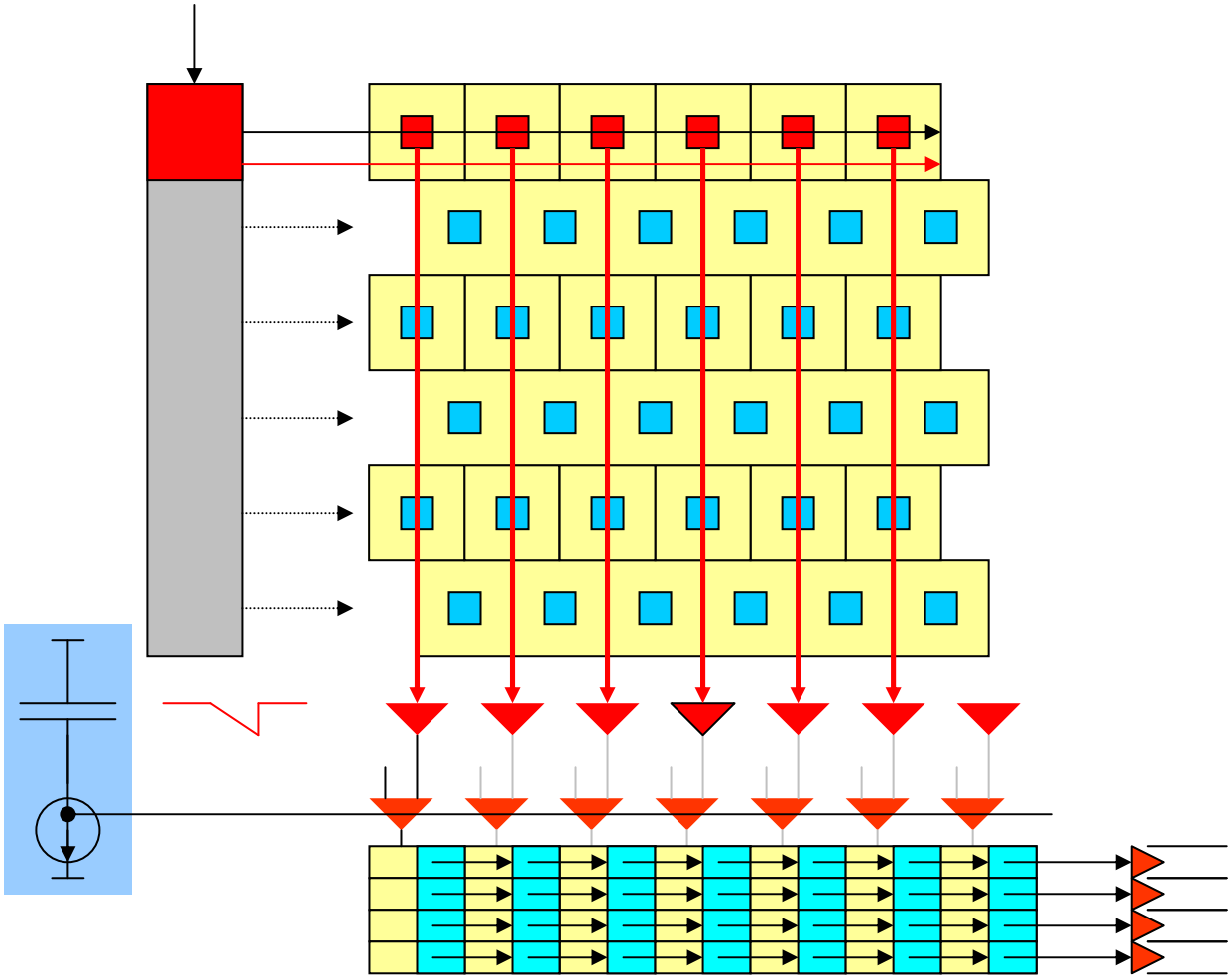
Shift out of time stamps



Shift out of time stamps

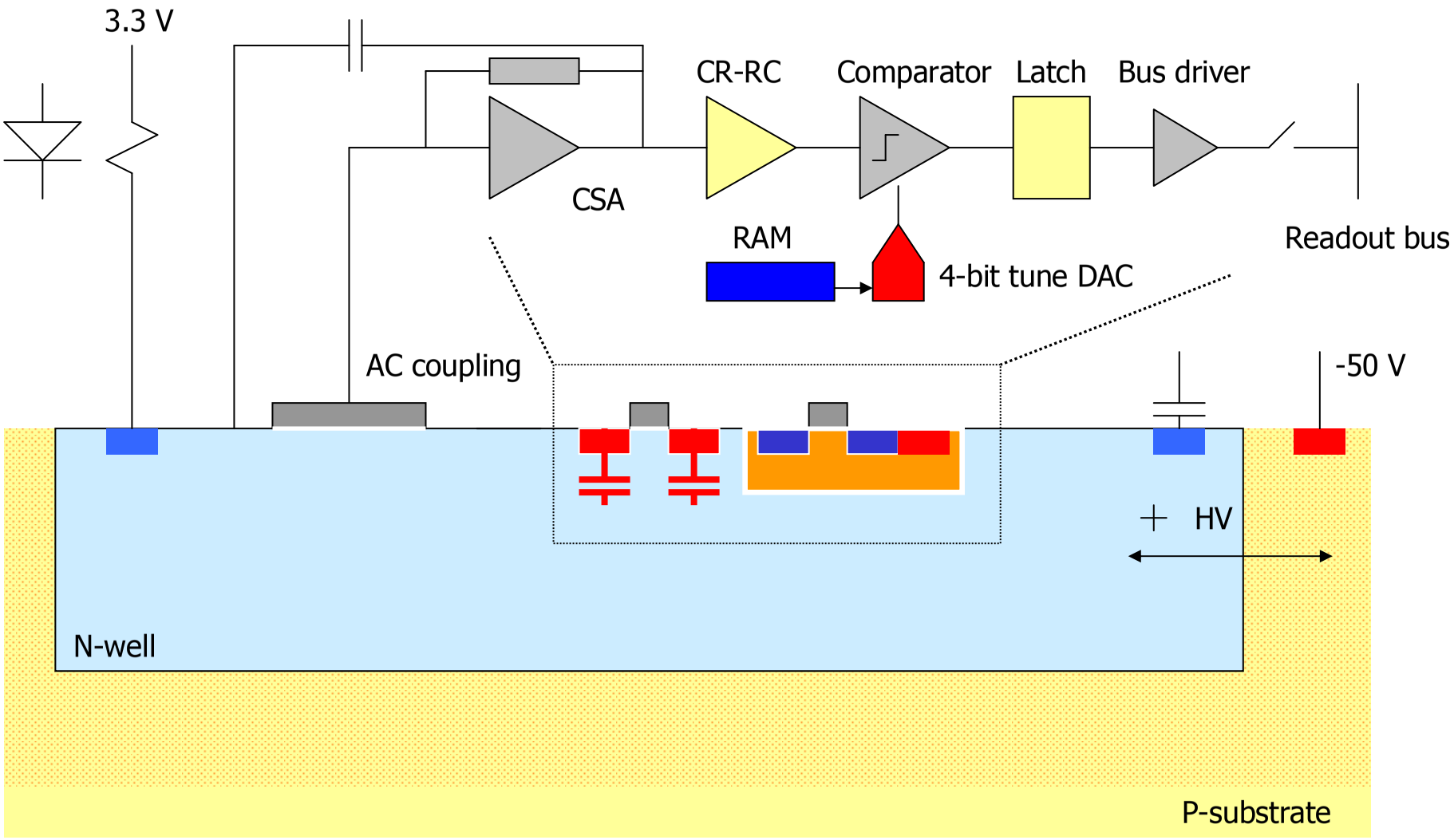


Shift out of time stamps



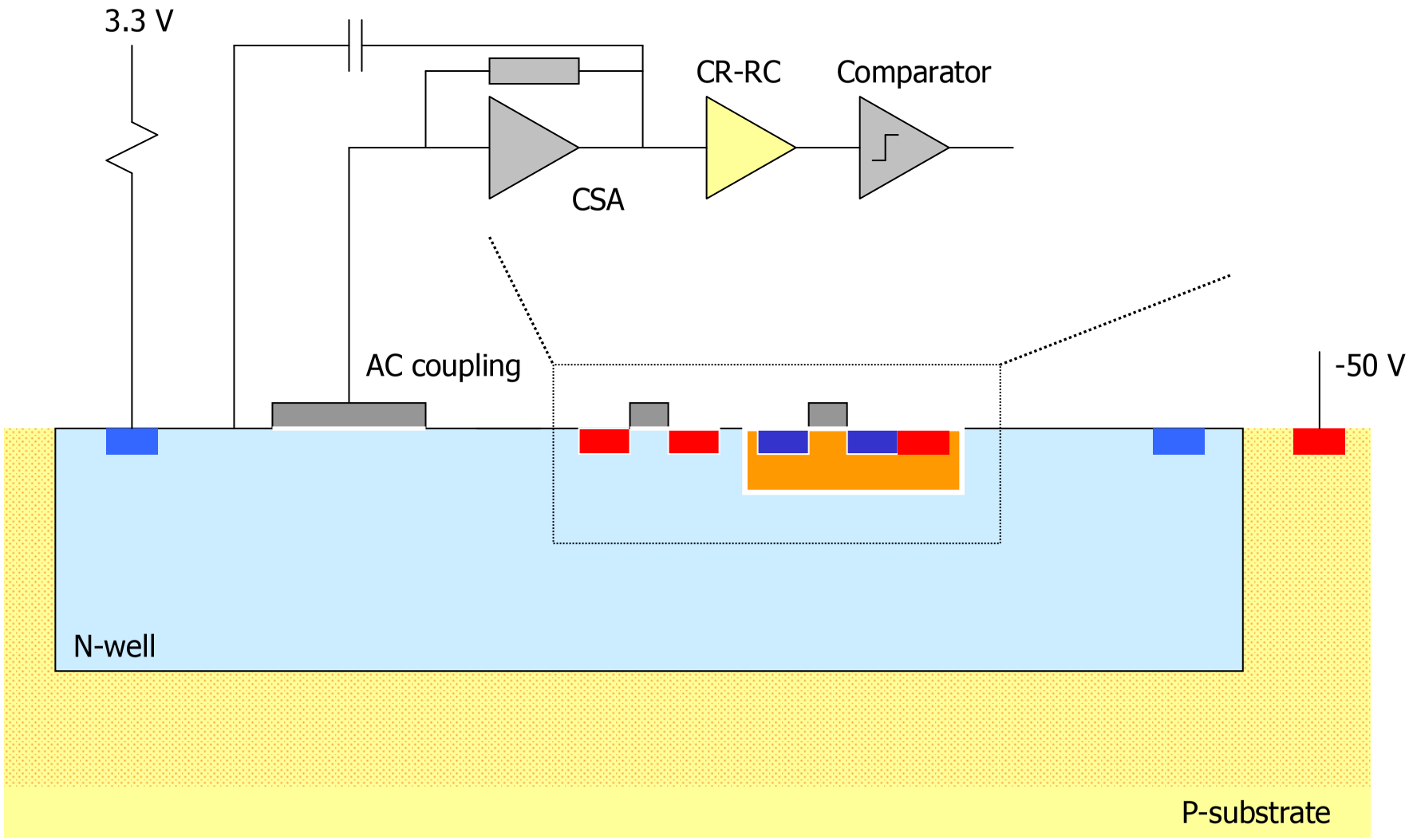
Smart diode sensor – the variant with intelligent pixels and sparse readout

Intelligent pixel

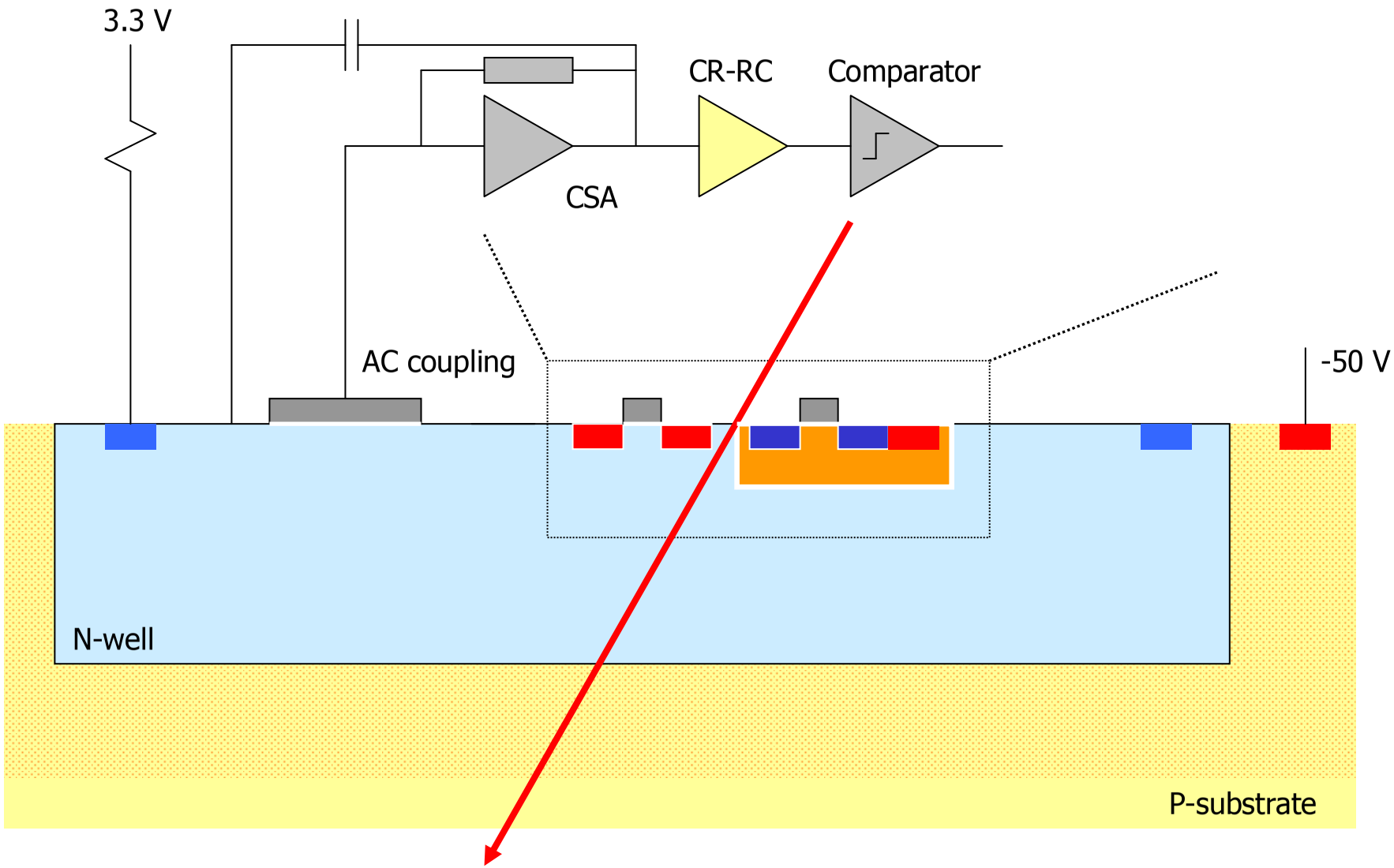


N-well is the sensor cathode and, at the same time, the body of the PMOS transistors

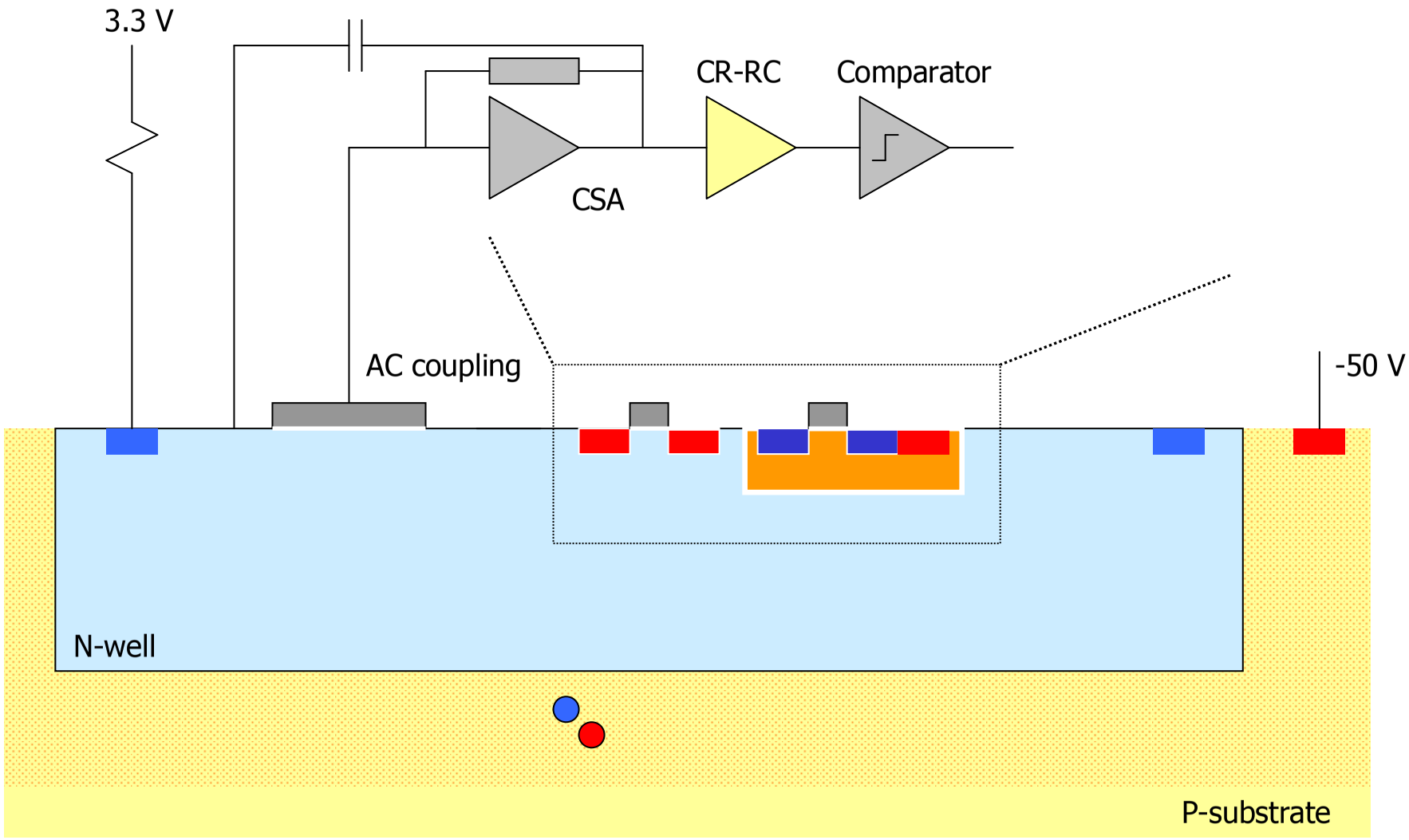
Intelligent pixel



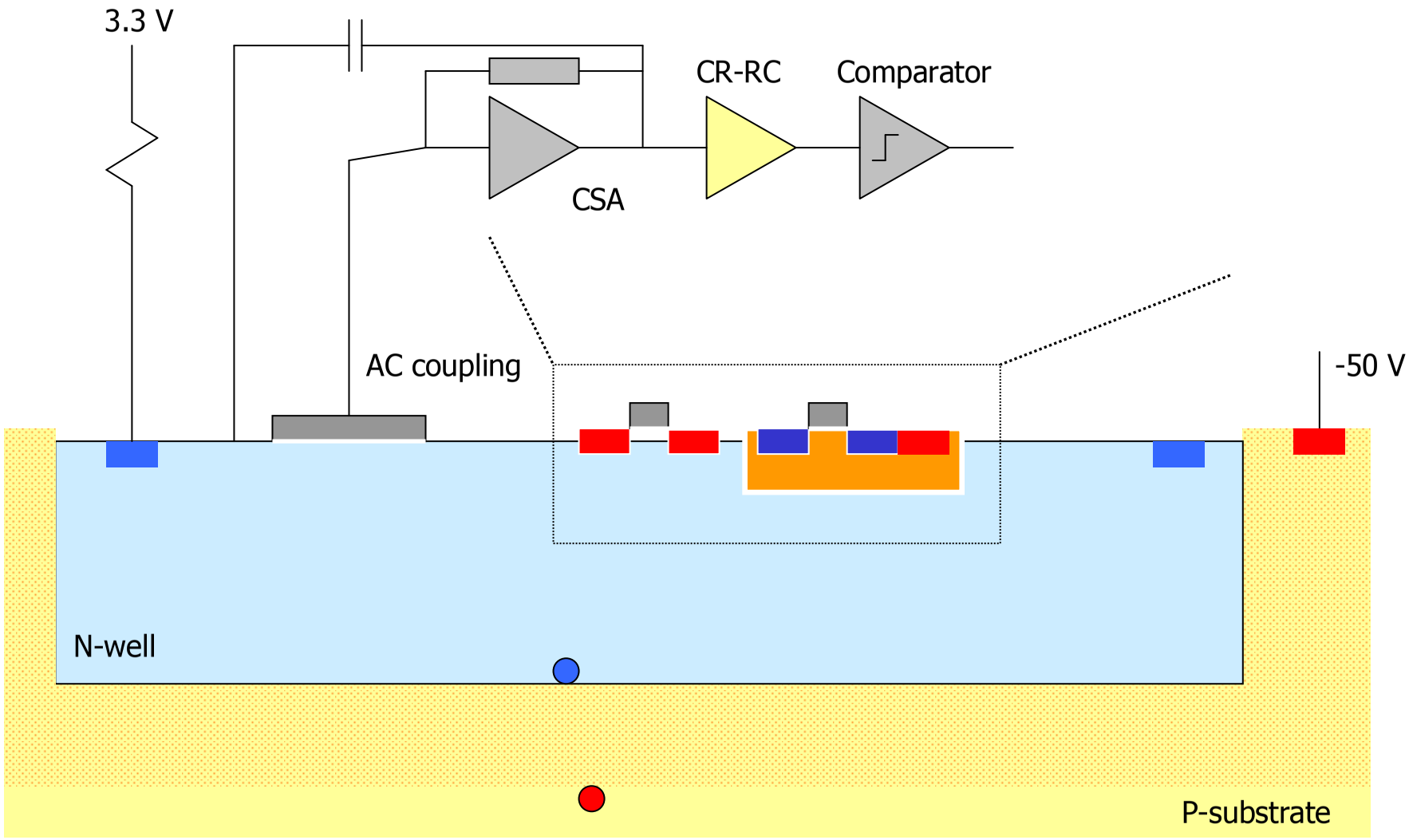
Intelligent pixel



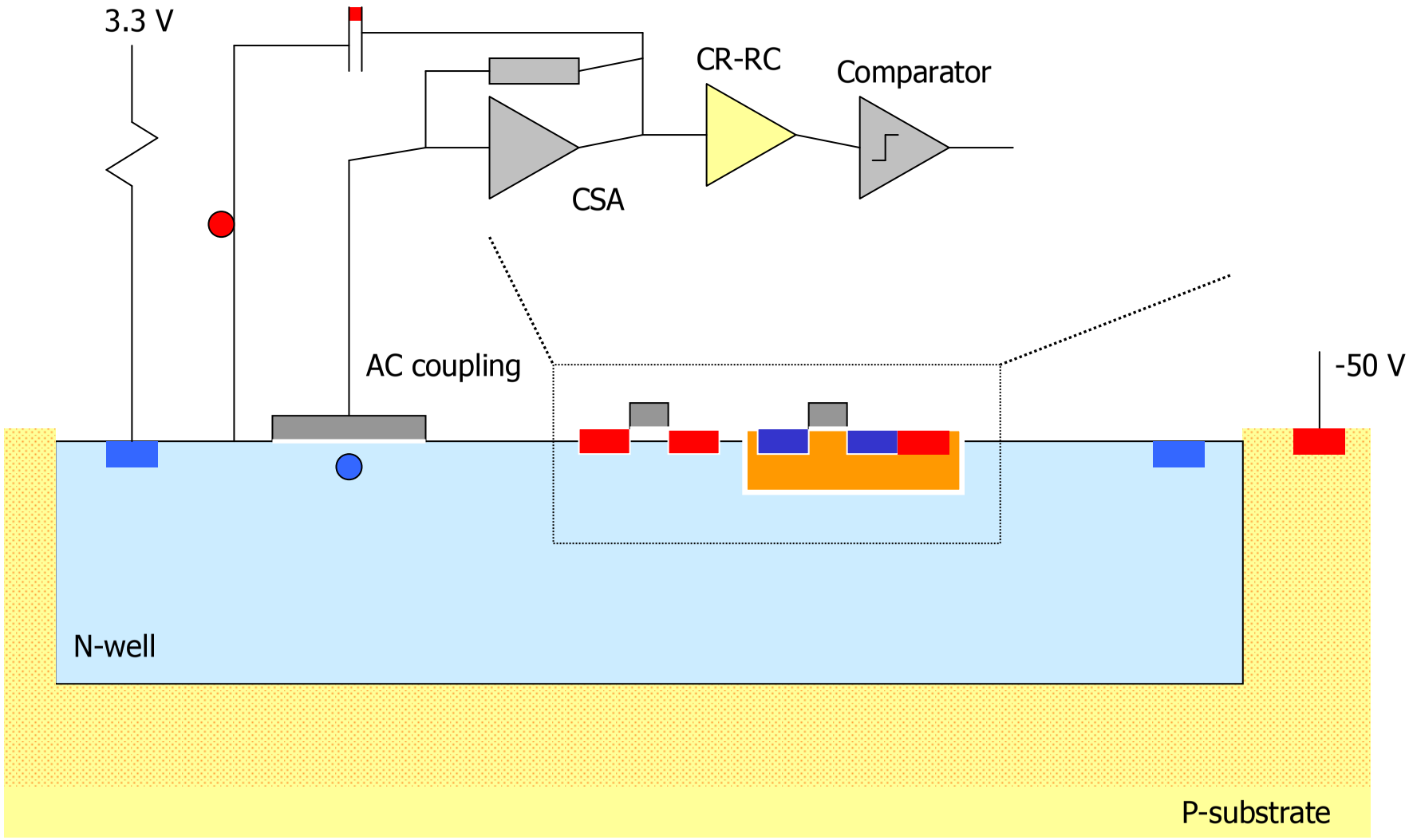
Intelligent pixel



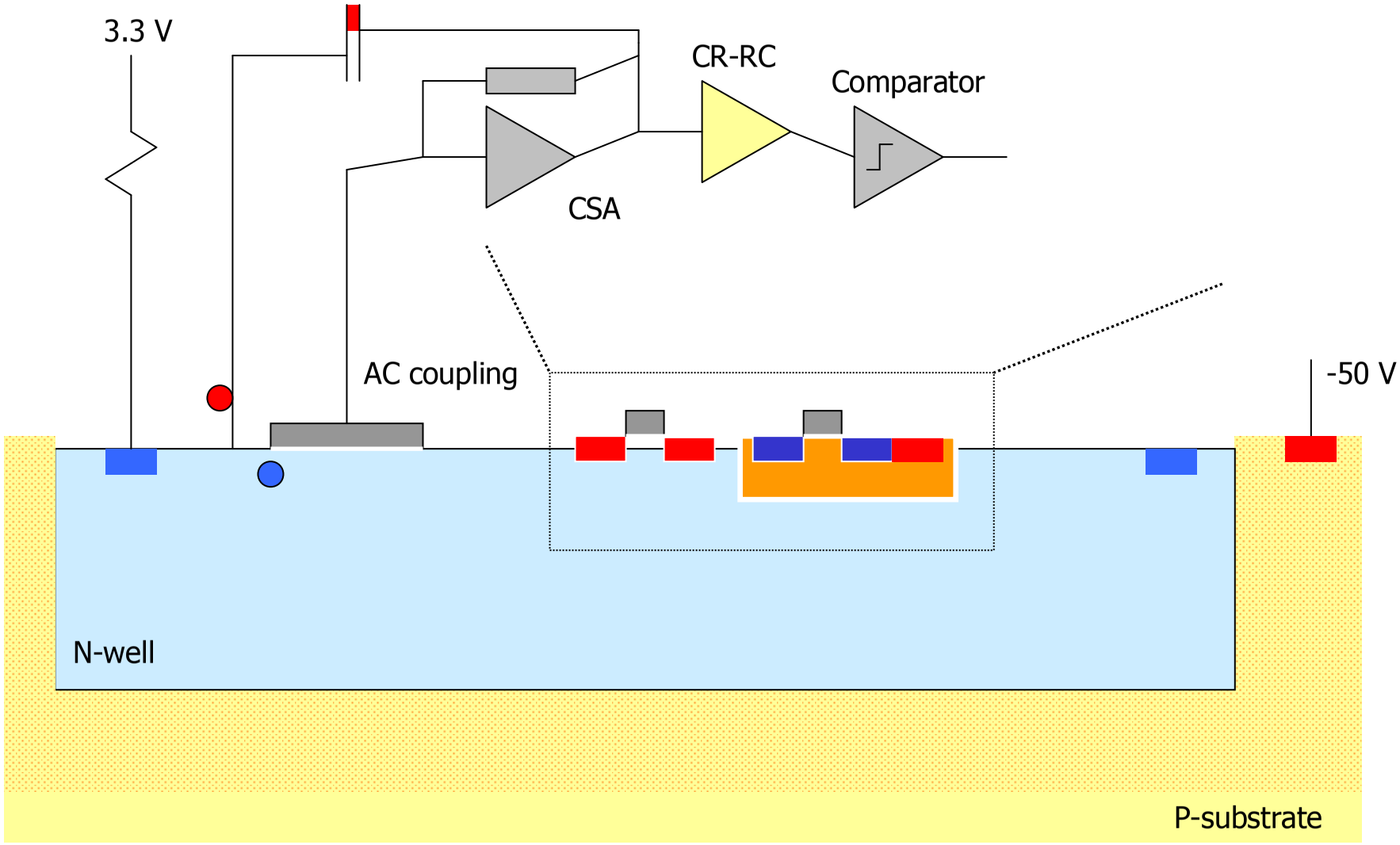
Intelligent pixel



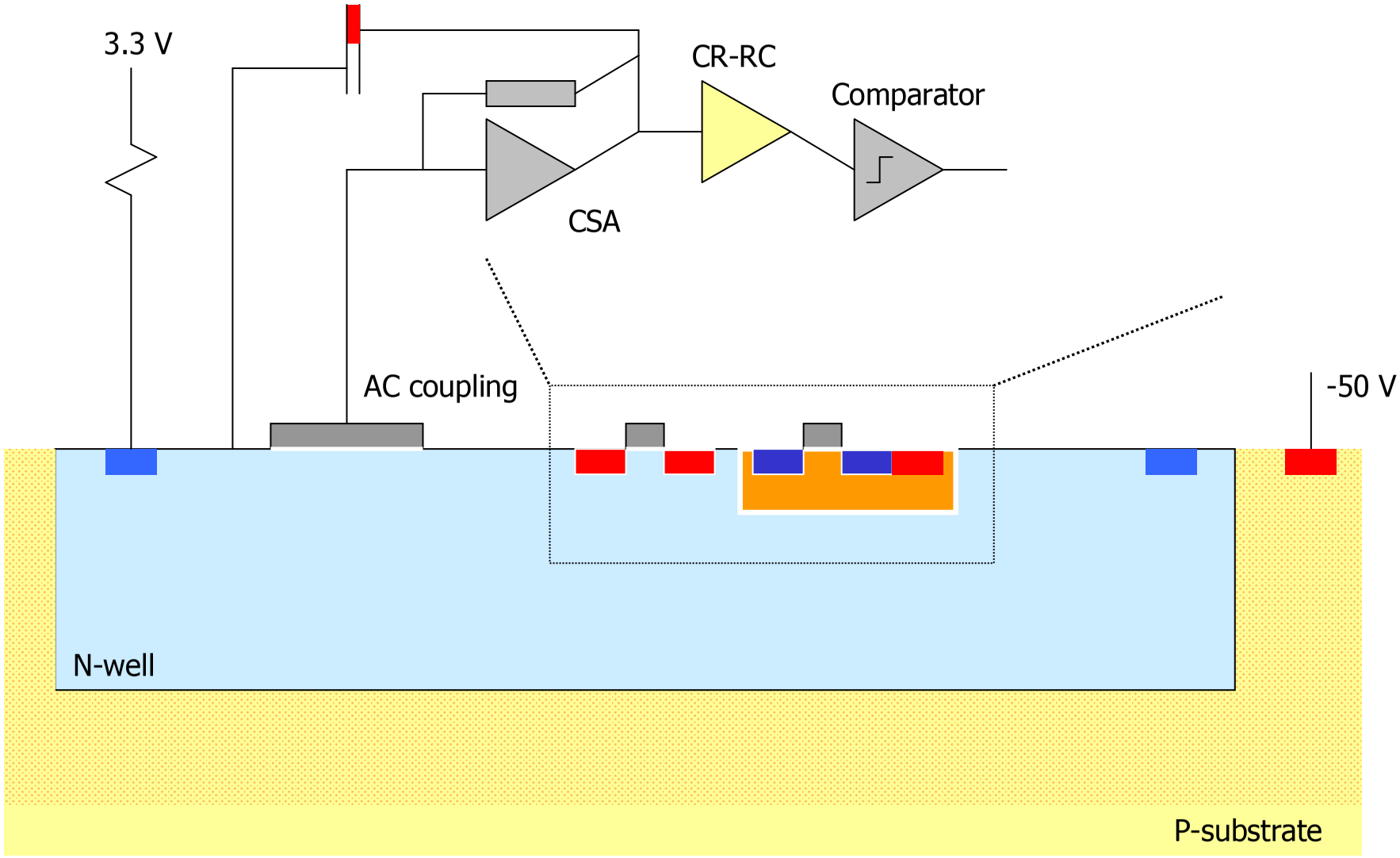
Intelligent pixel



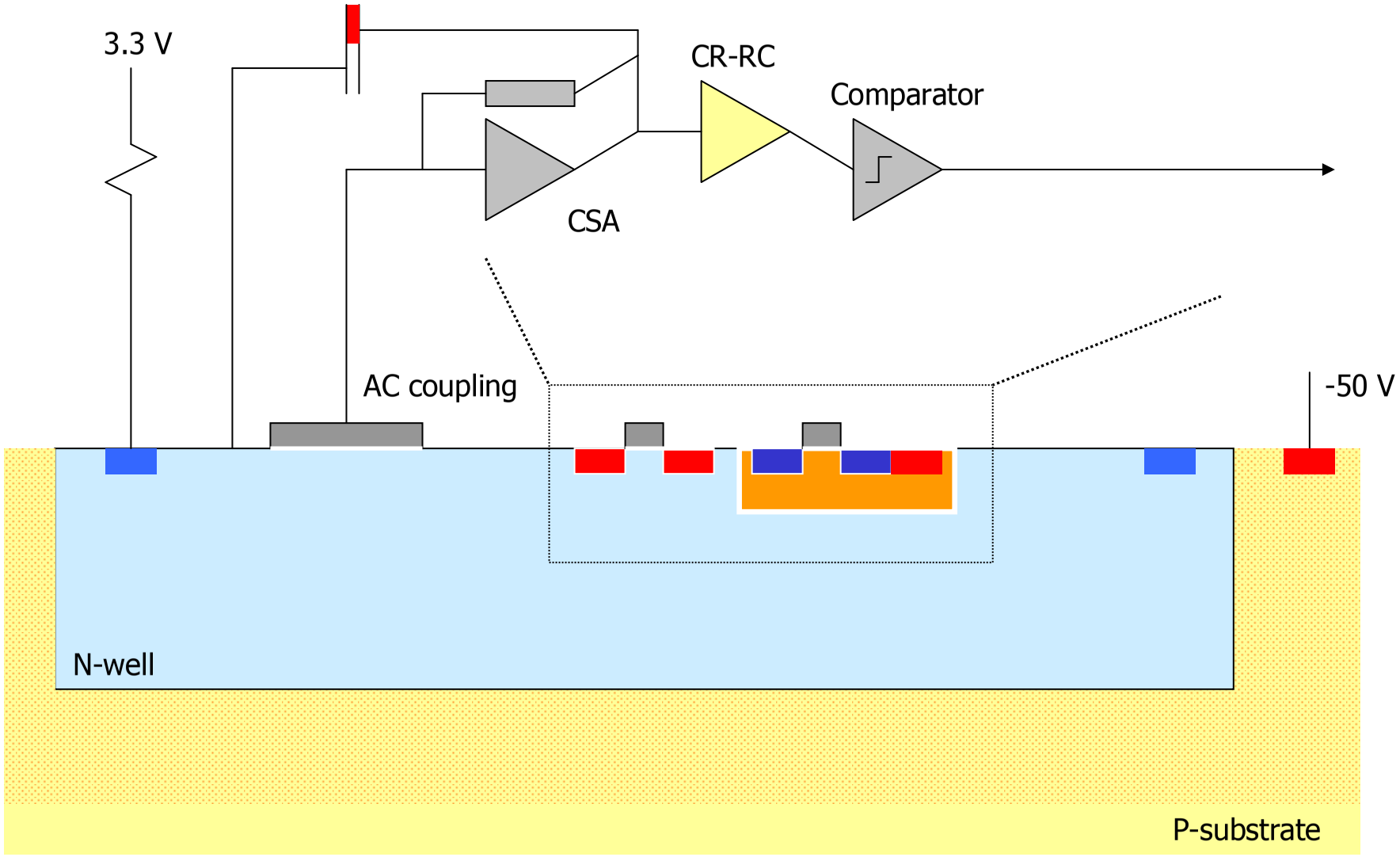
Intelligent pixel



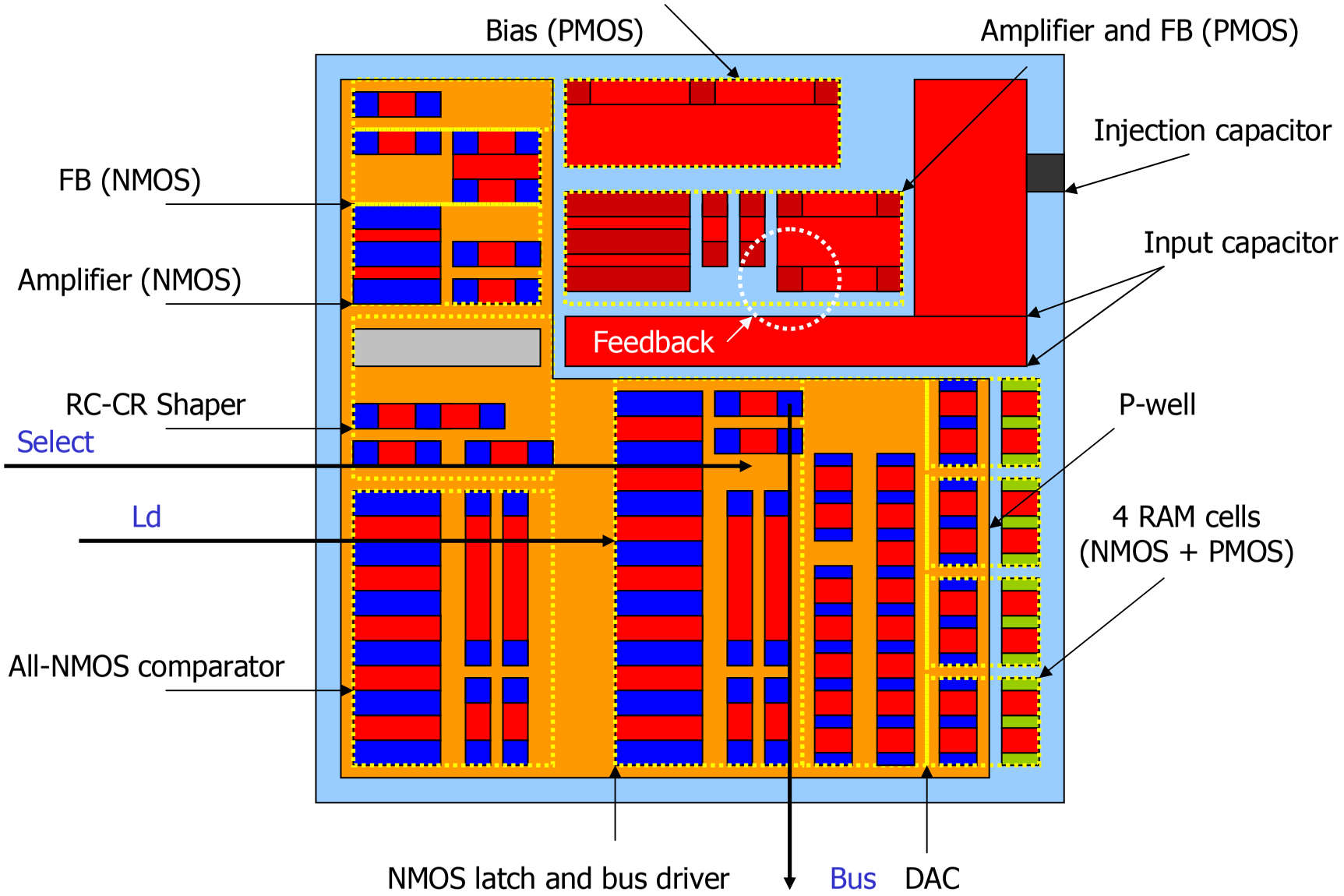
Intelligent pixel



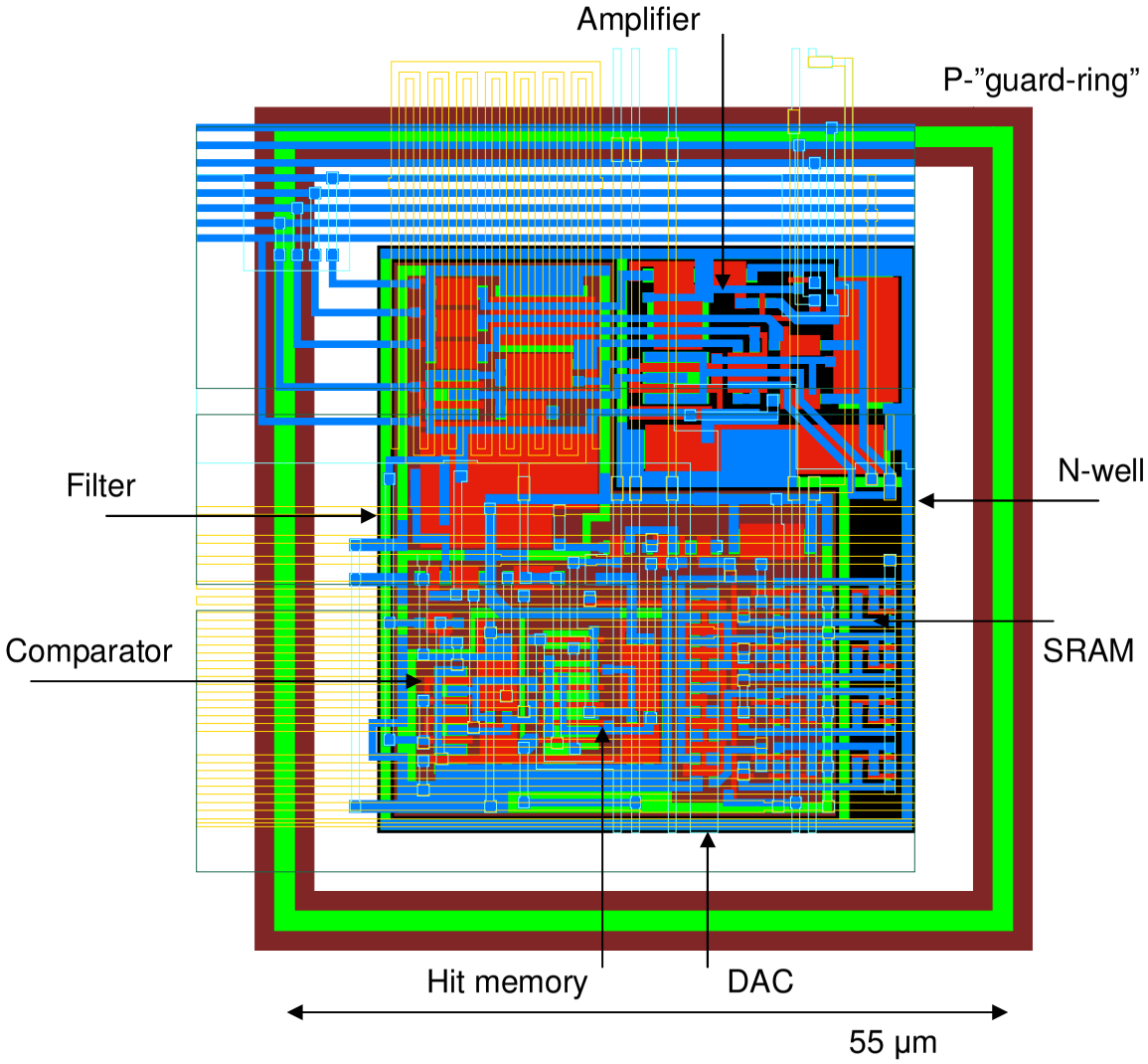
Intelligent pixel



HV2 pixel floorplan

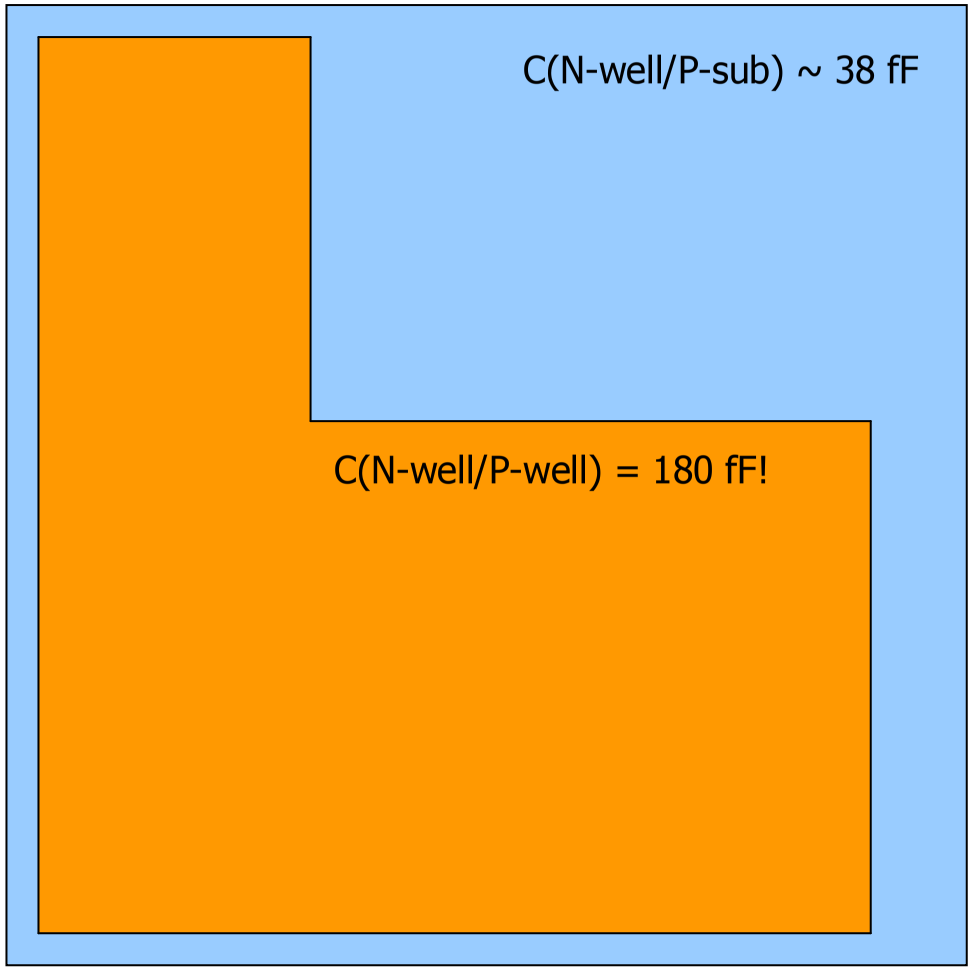


HV2 pixel layout

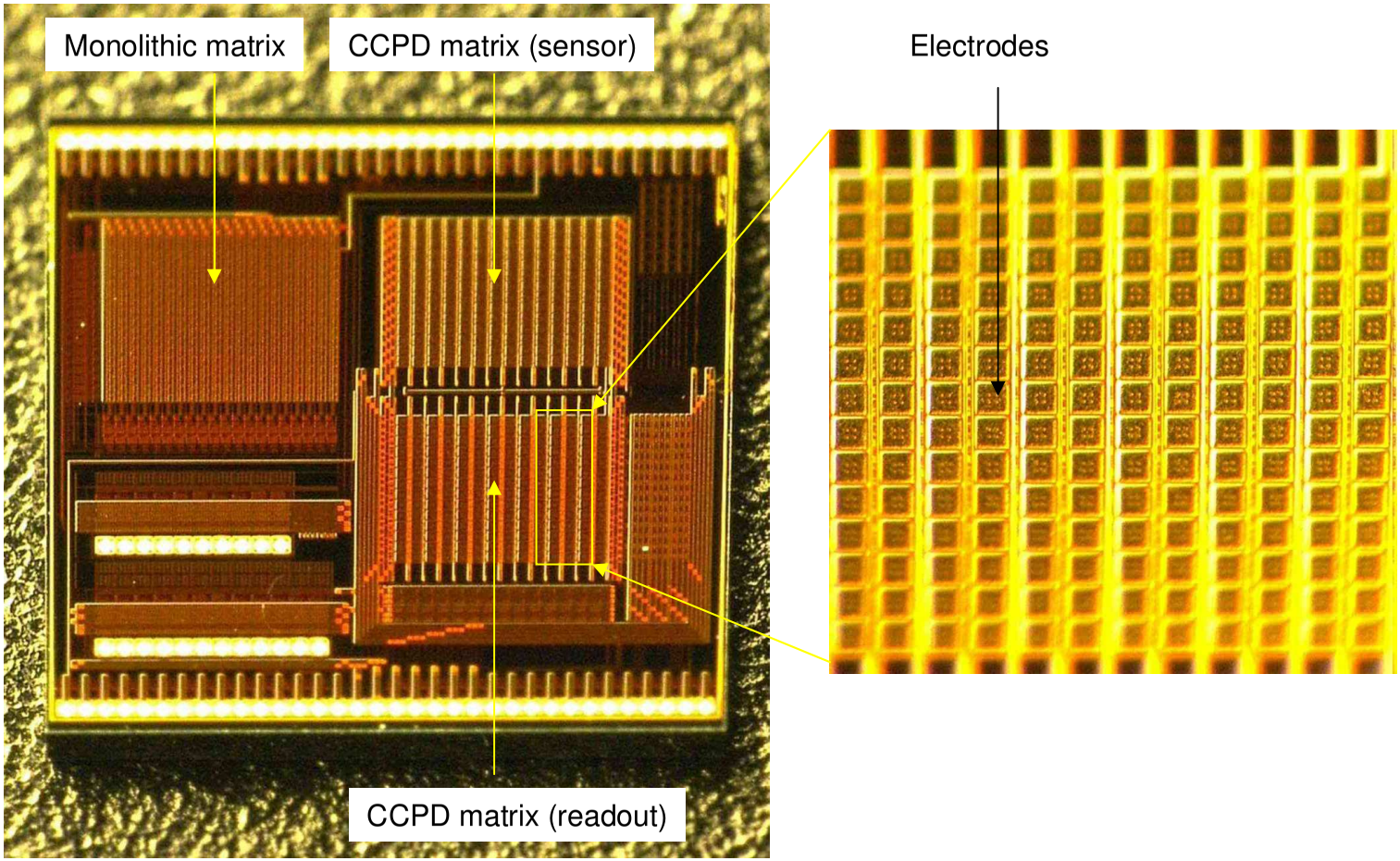


Detector capacitance

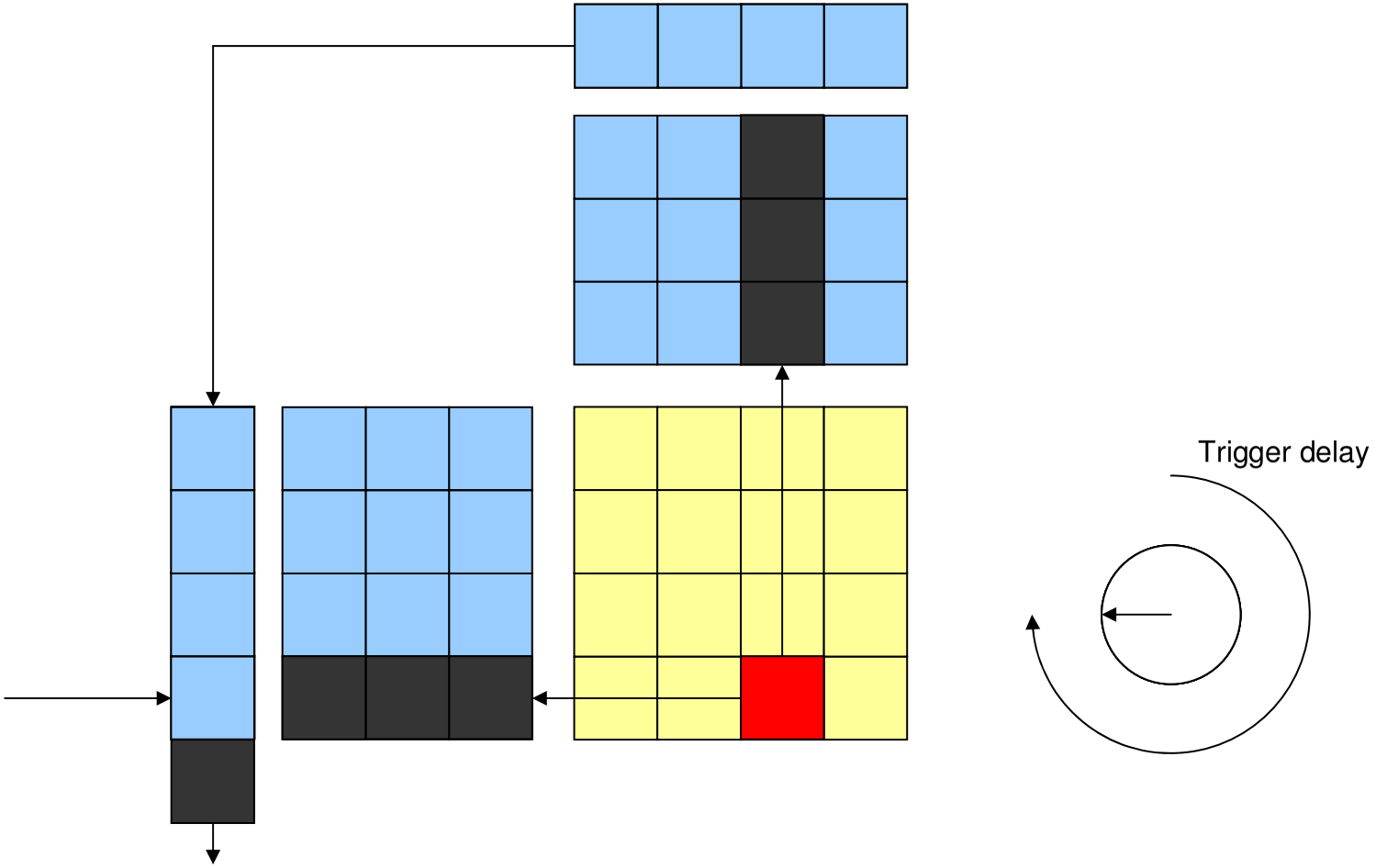
The large detector capacitance limits the performances of the detector



HV2 chip

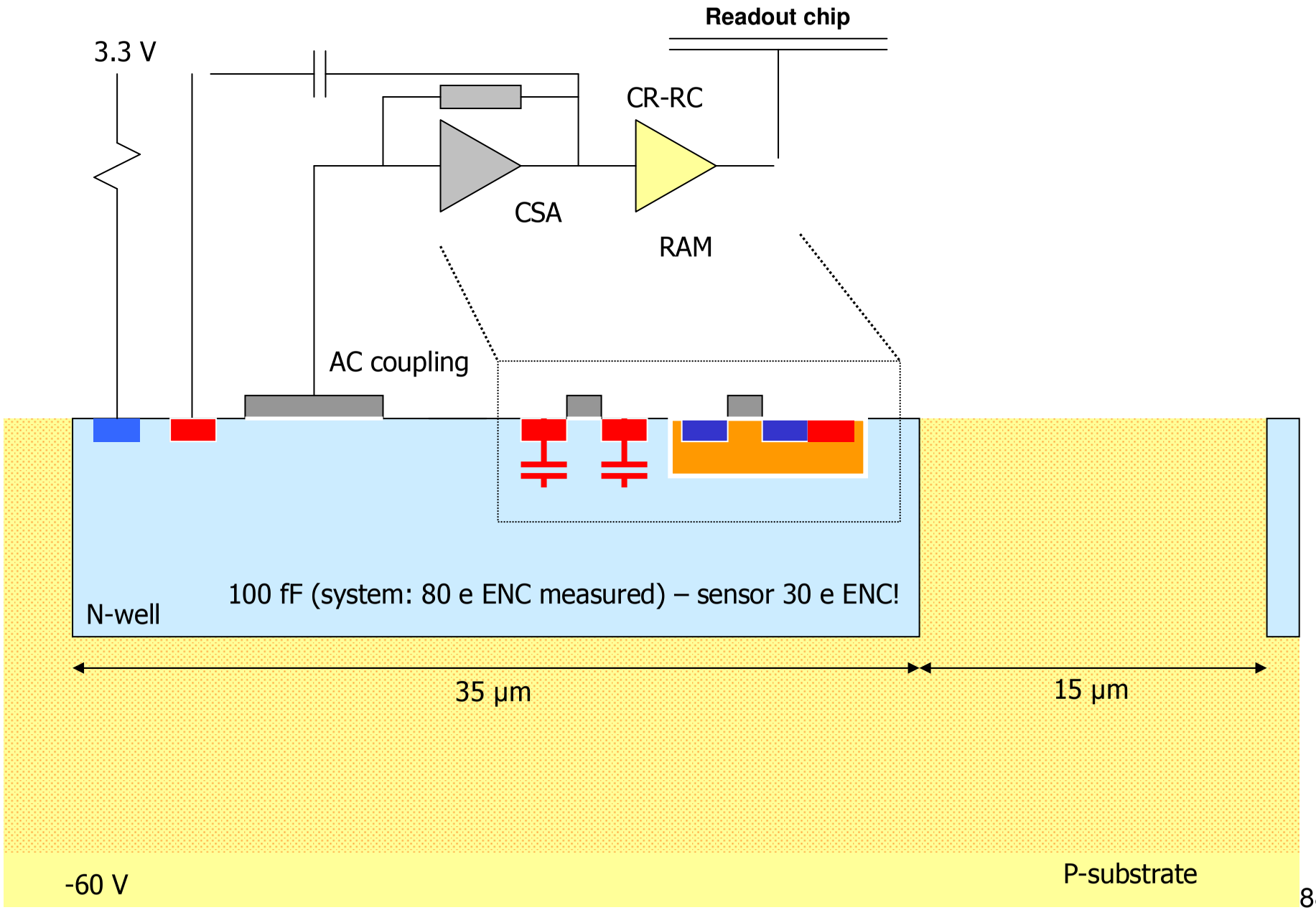

Monolithic matrix
CCPD matrix (sensor)
Electrodes
CCPD matrix (readout)

Sparse readout

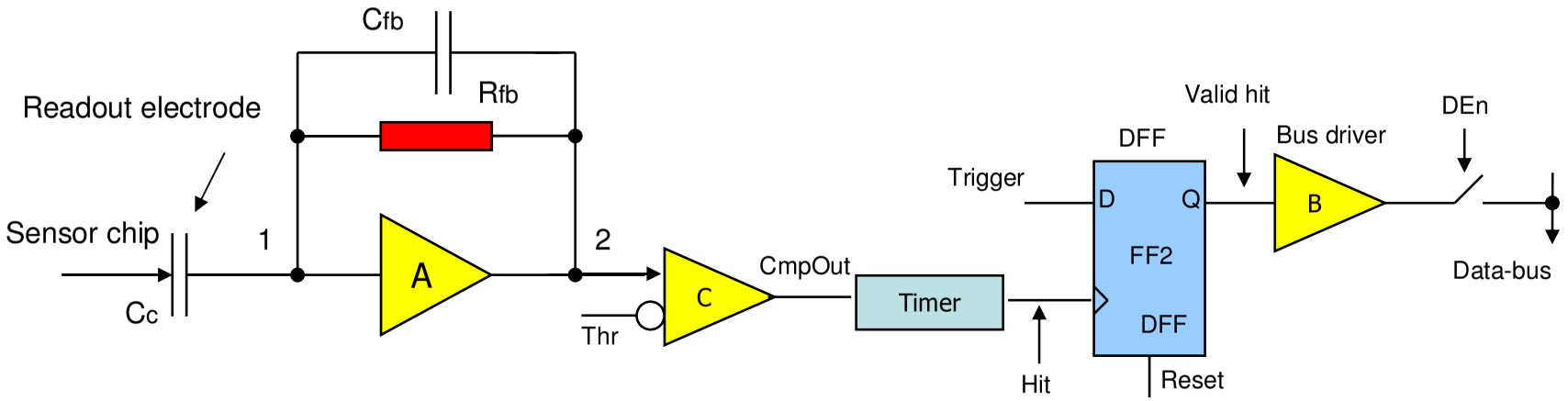


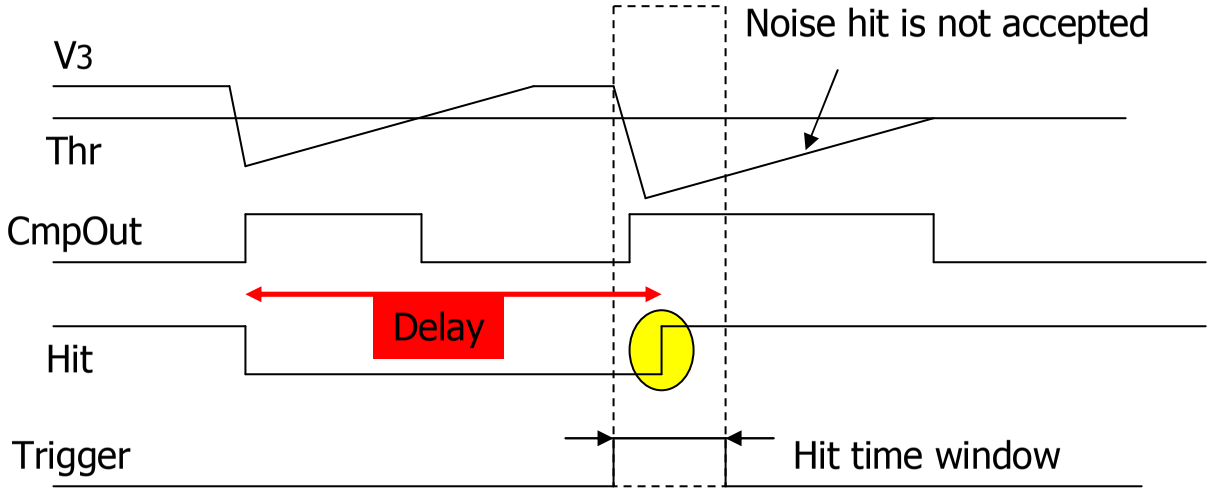
Smart diode sensor – the variant with intelligent pixels and capacitive readout 1.

SDS with capacitive readout - principle



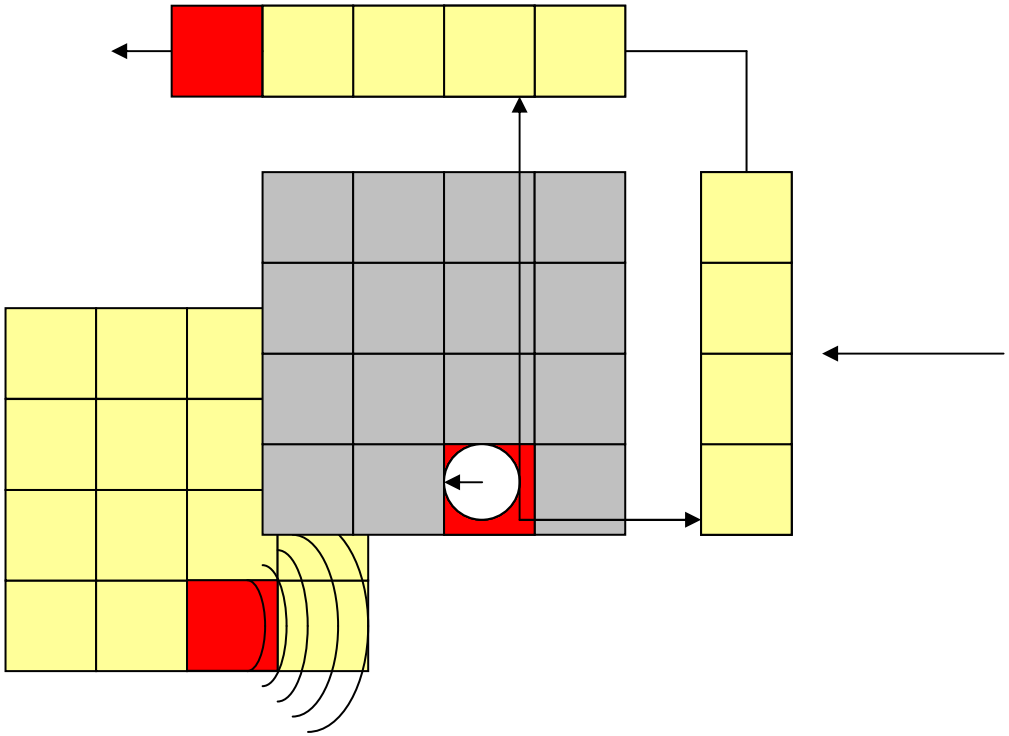
Trigger-based readout



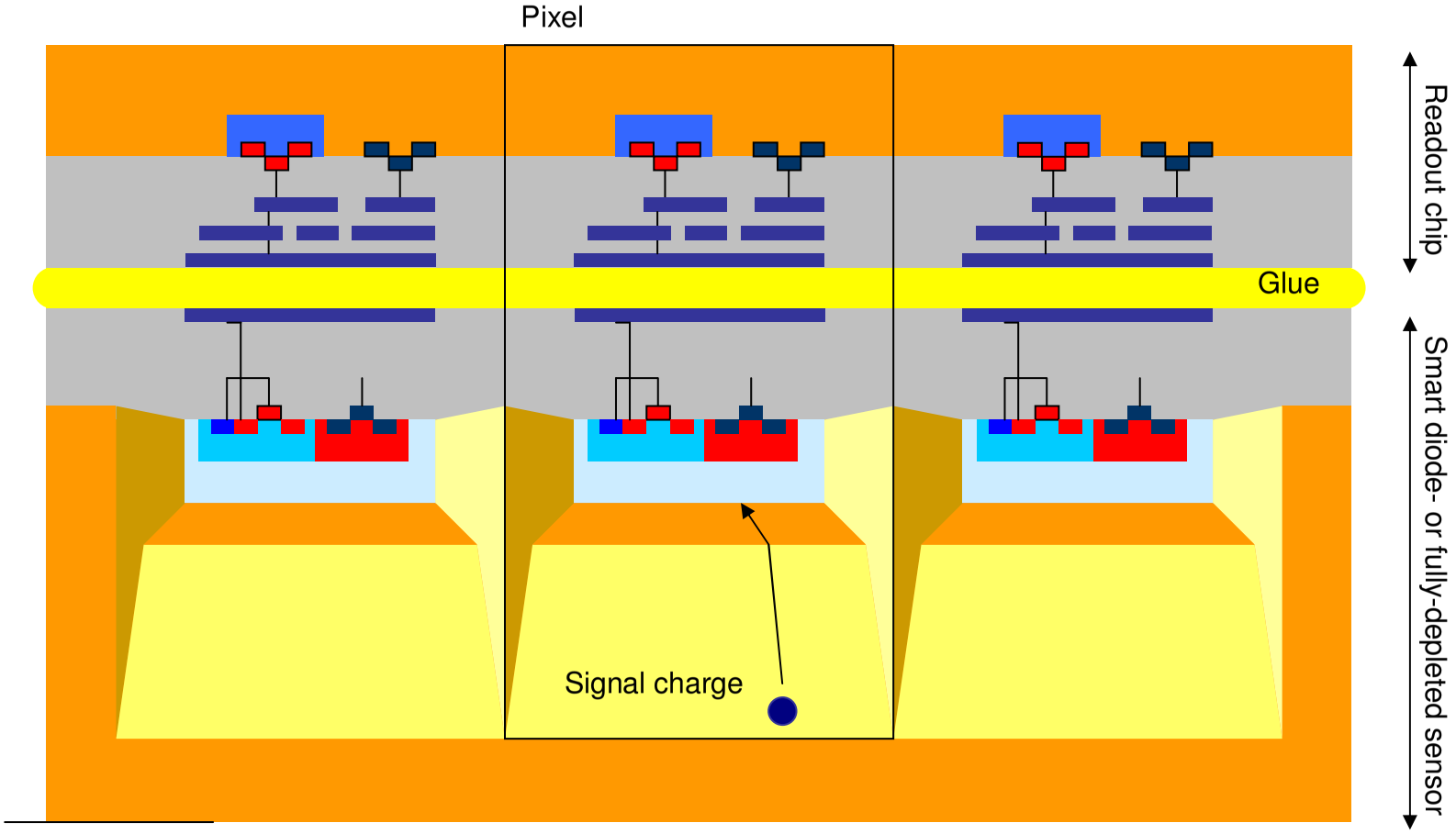


A – receiver CSA
C – comparator
- Timer generates *Hit* some defined time after the threshold crossing moment
- Only “in time signals” flagged as hits

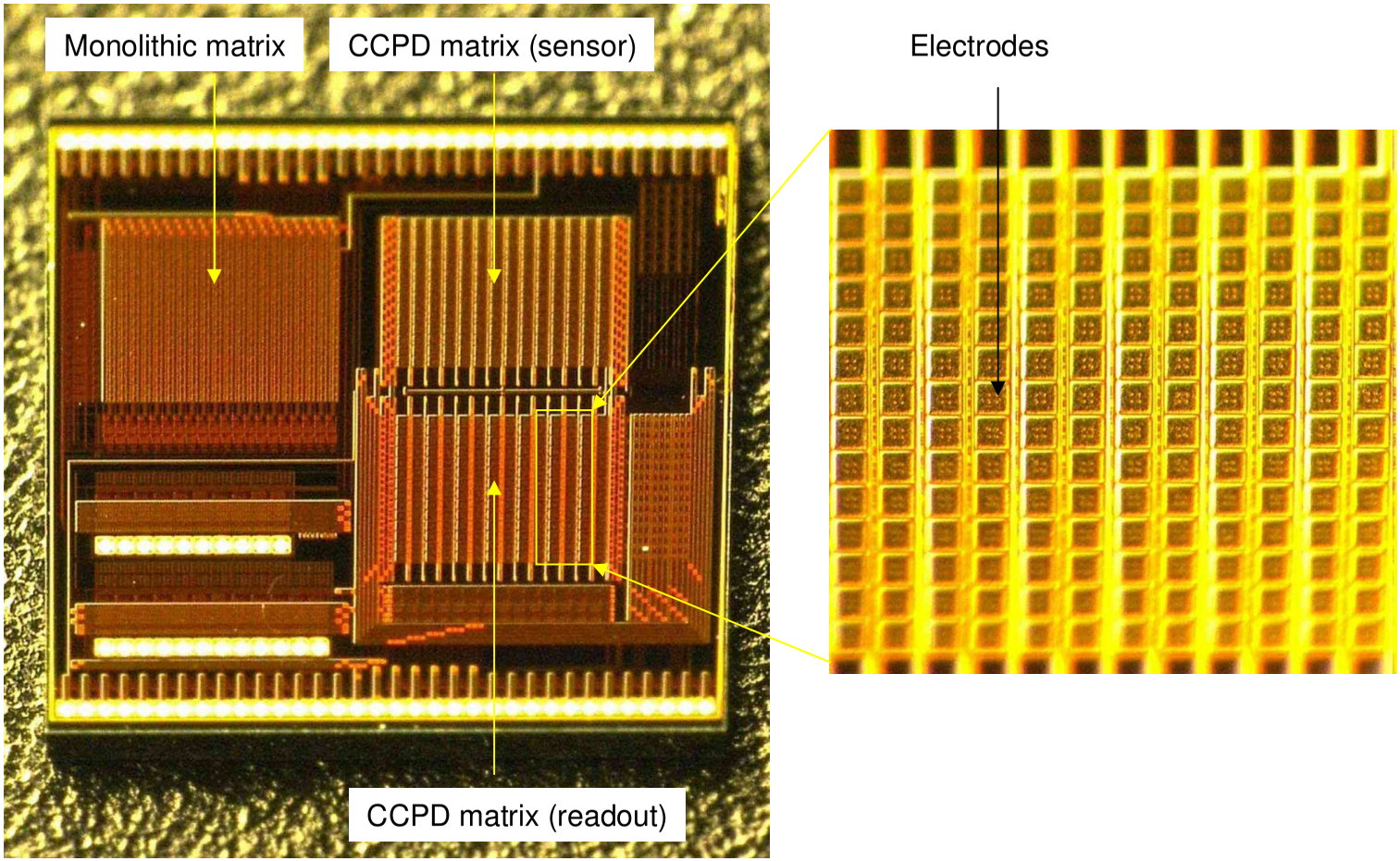
Sparse readout



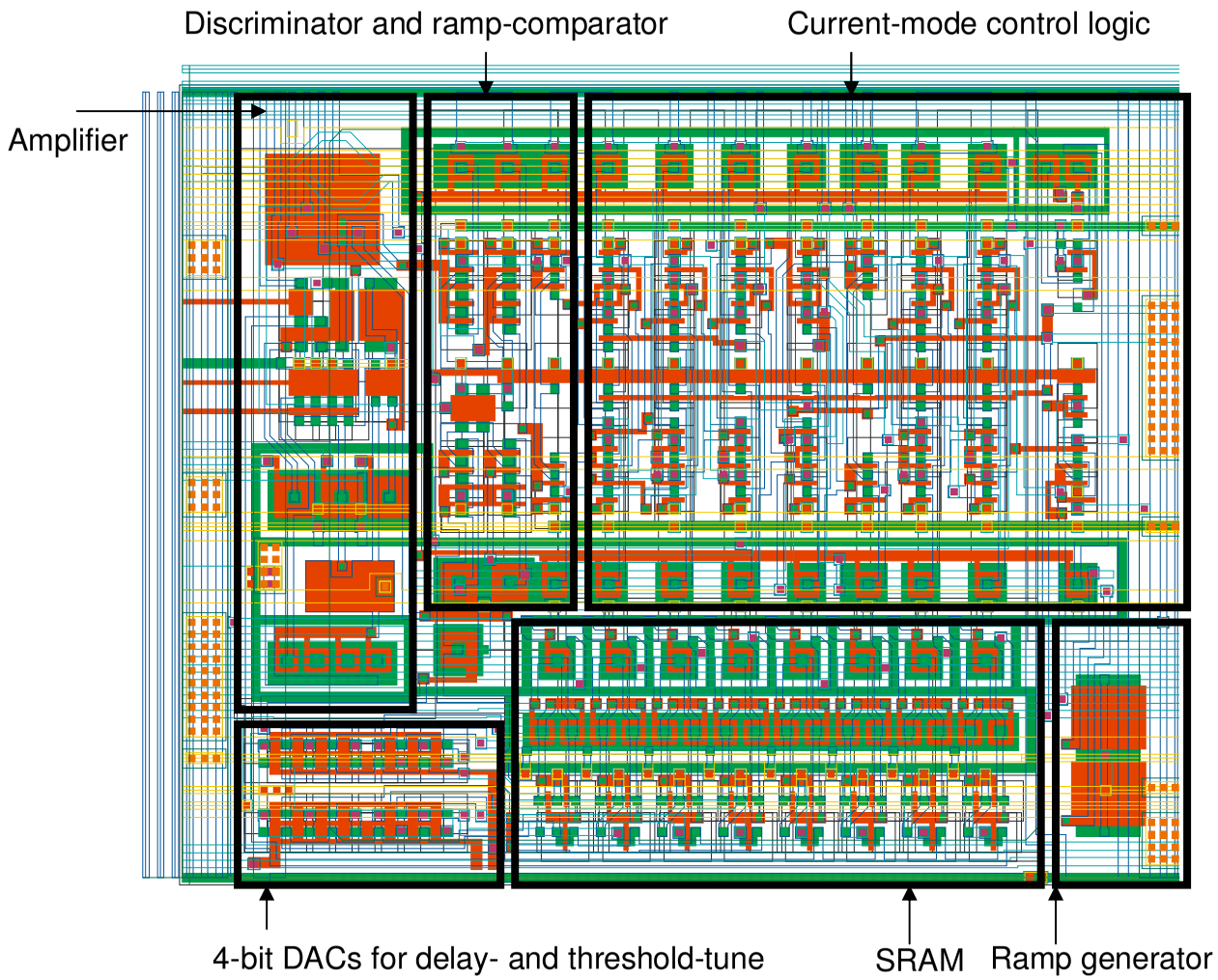
Smart diode sensor with capacitive readout (CCPD1)



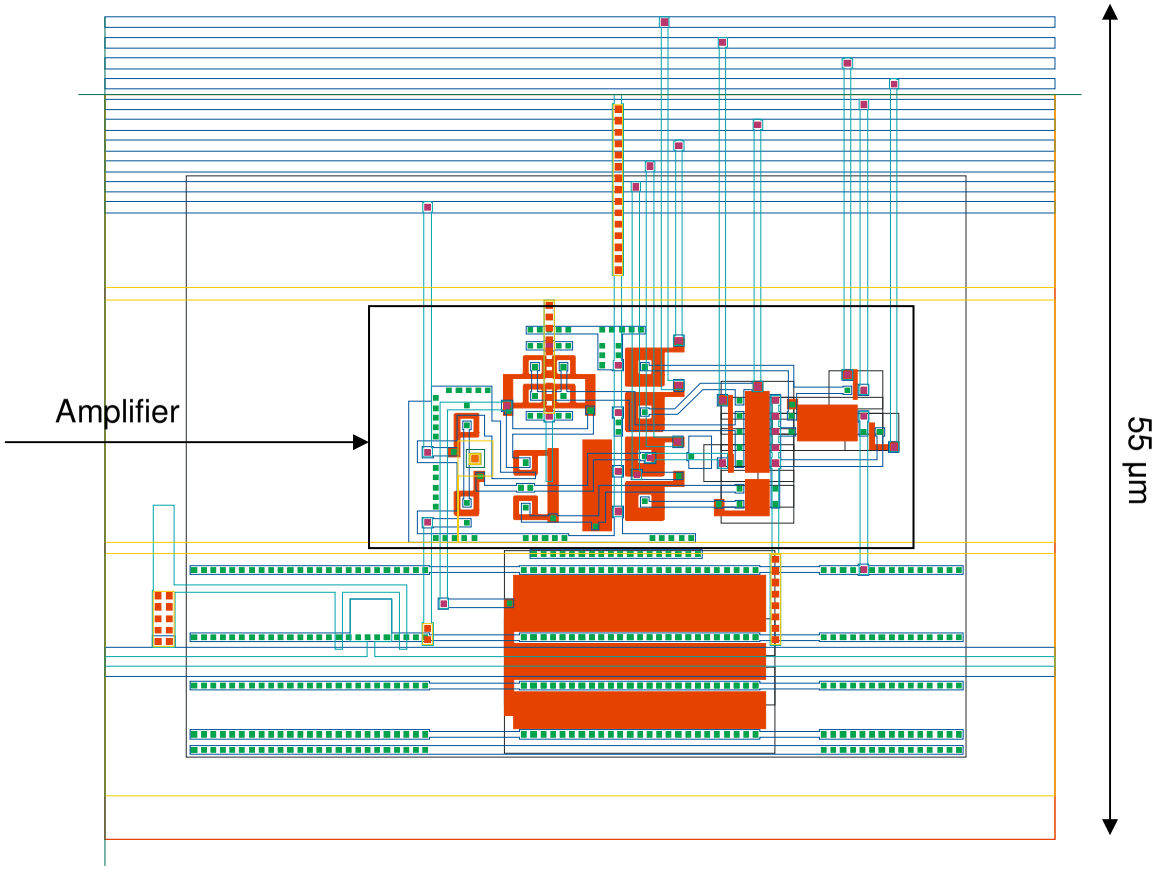
CCPD1 chip


Monolithic matrix
CCPD matrix (sensor)
Electrodes
CCPD matrix (readout)

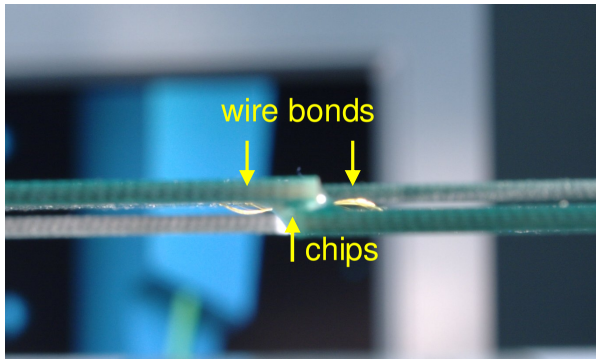
CCPD1 readout pixel layout

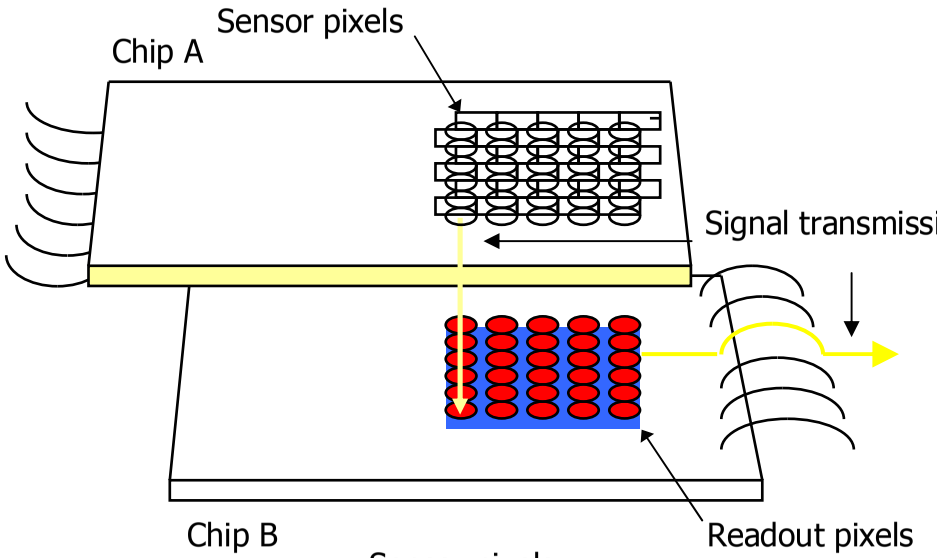


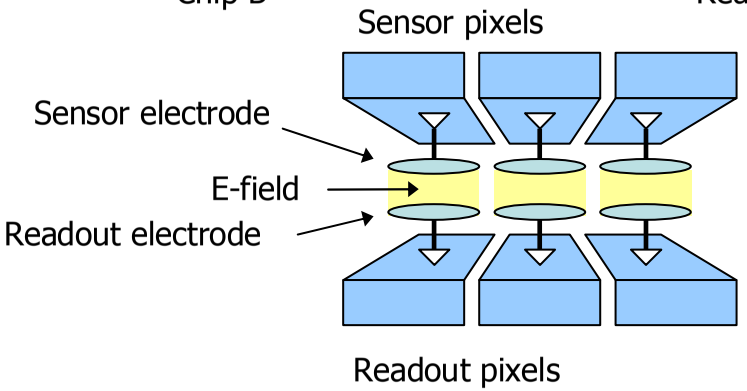
CCPD1 sensor pixel layout

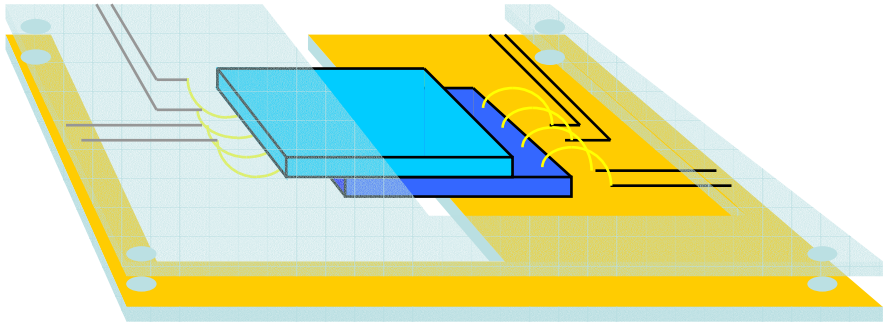


CCPD1 detector

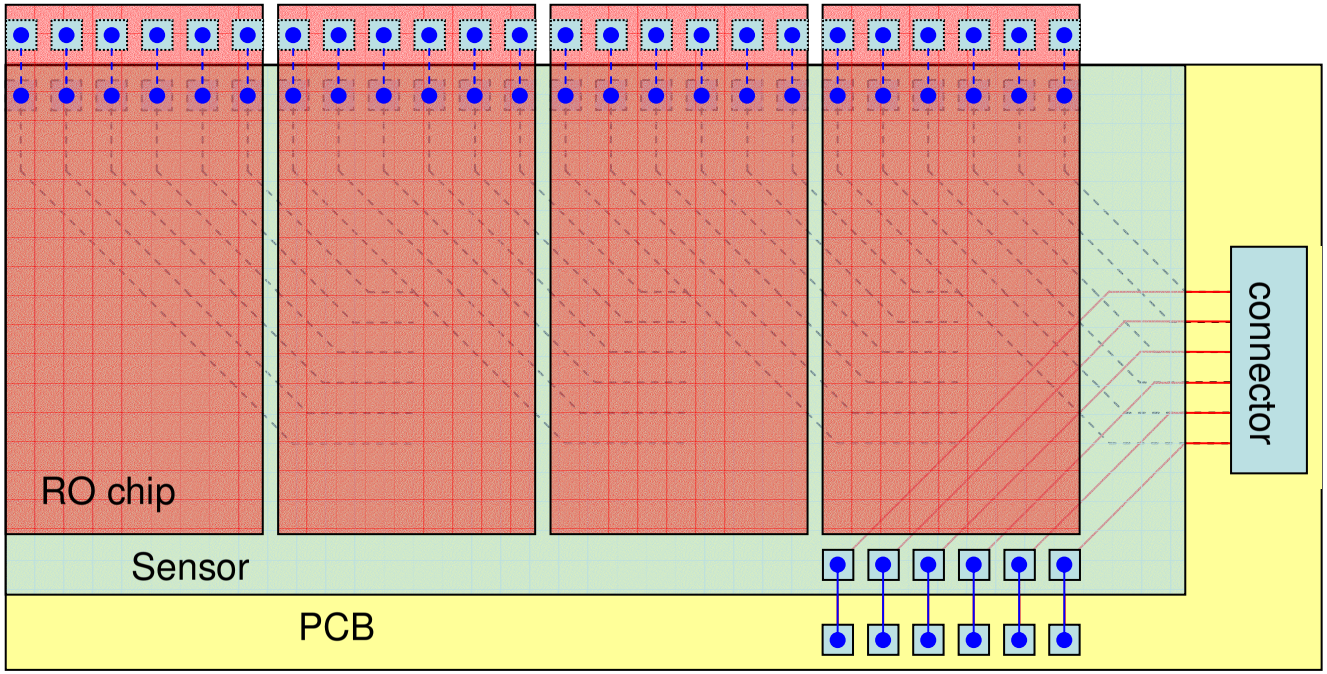








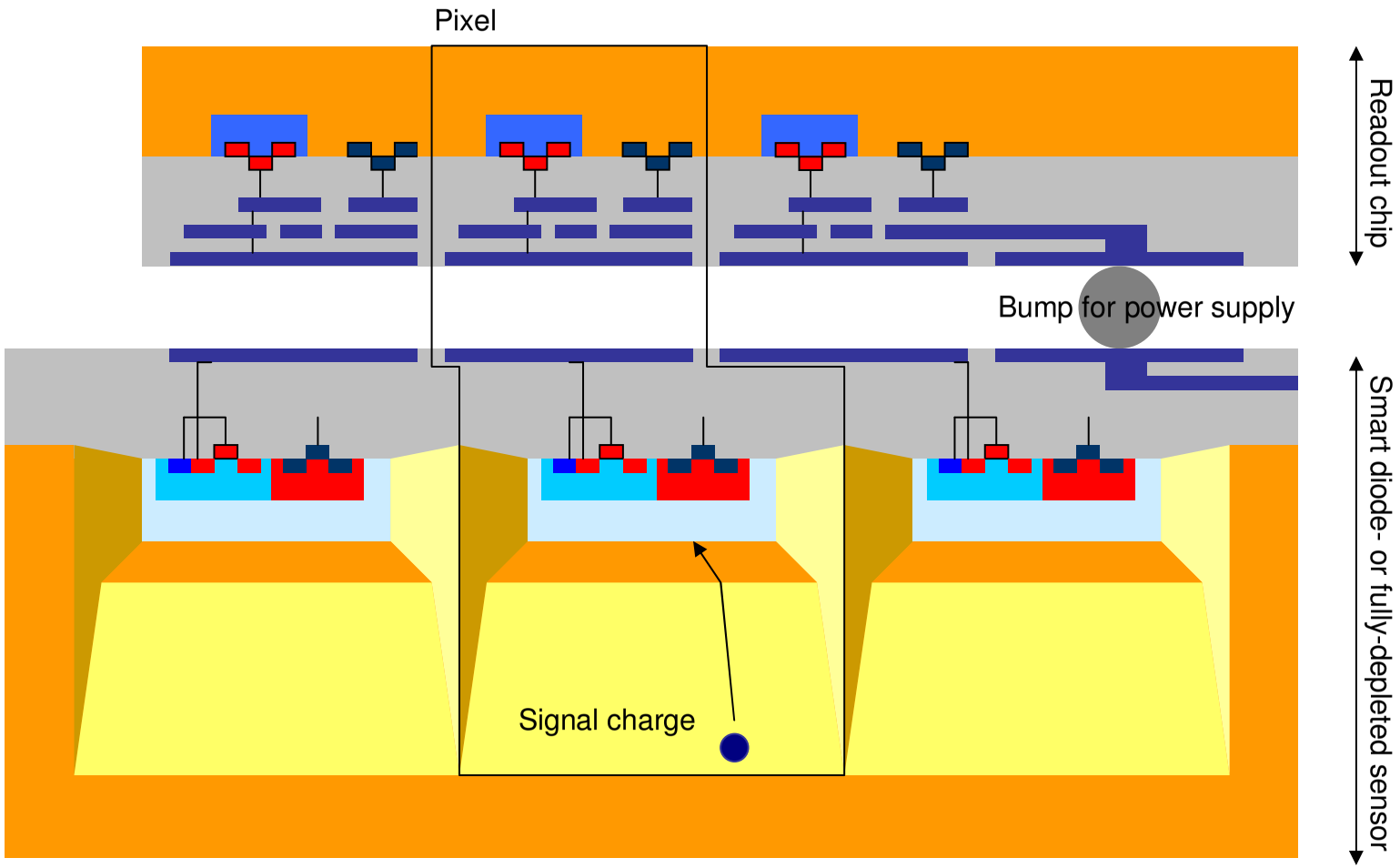
CCPD1 module concept



Wire bonds

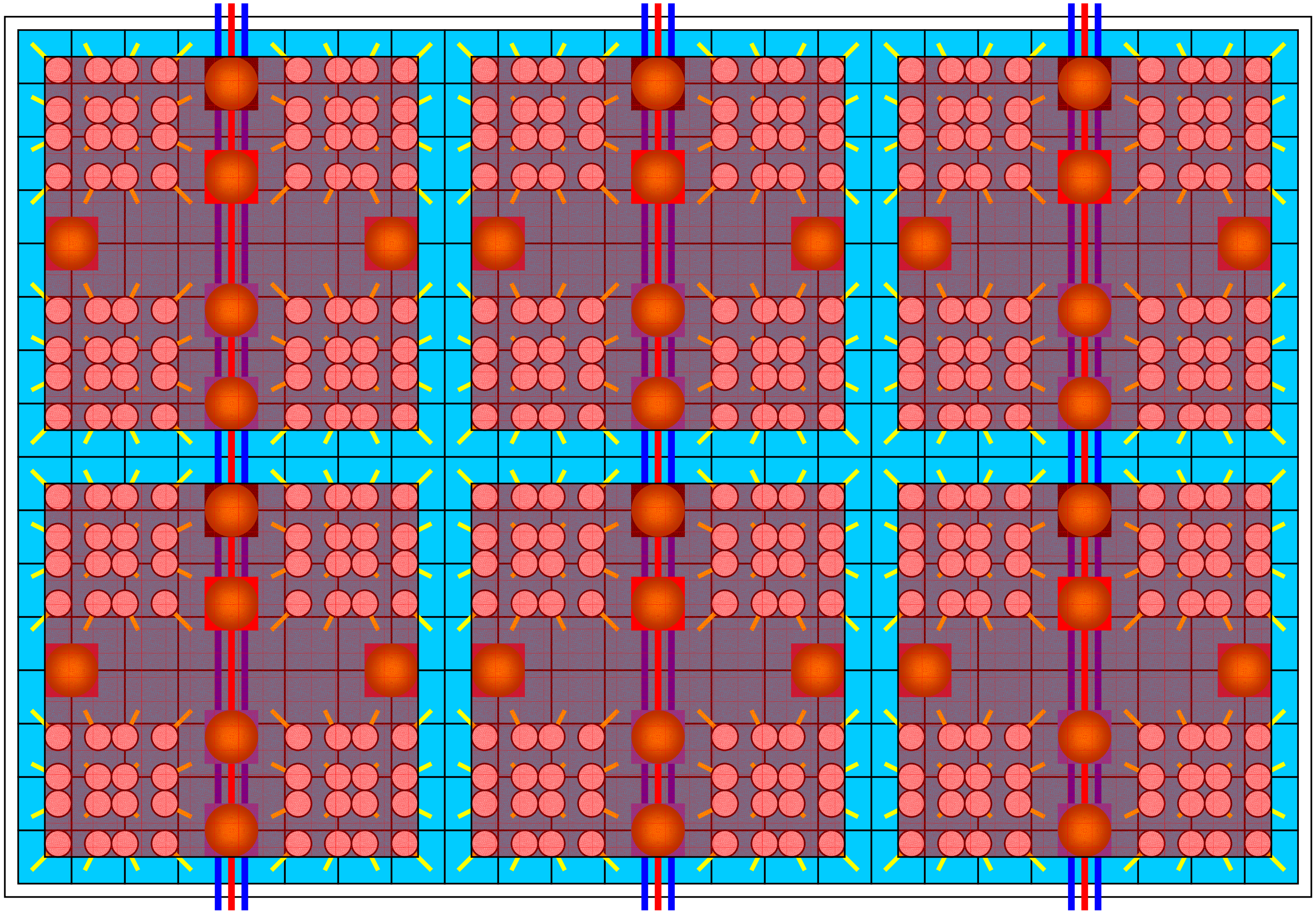
Smart diode sensor – the variant with intelligent pixels and capacitive readout 2.

Chip on the sensor concept (CCPD2)

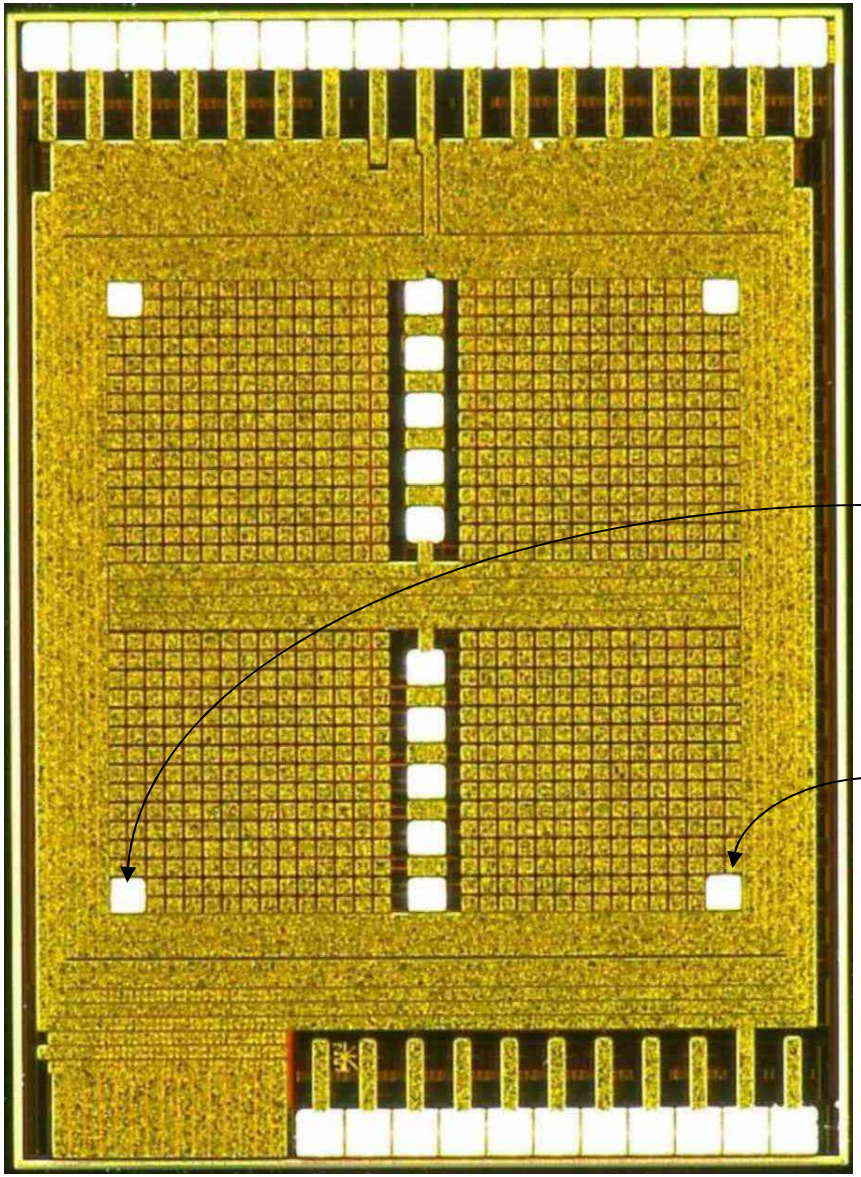


Sensor concept

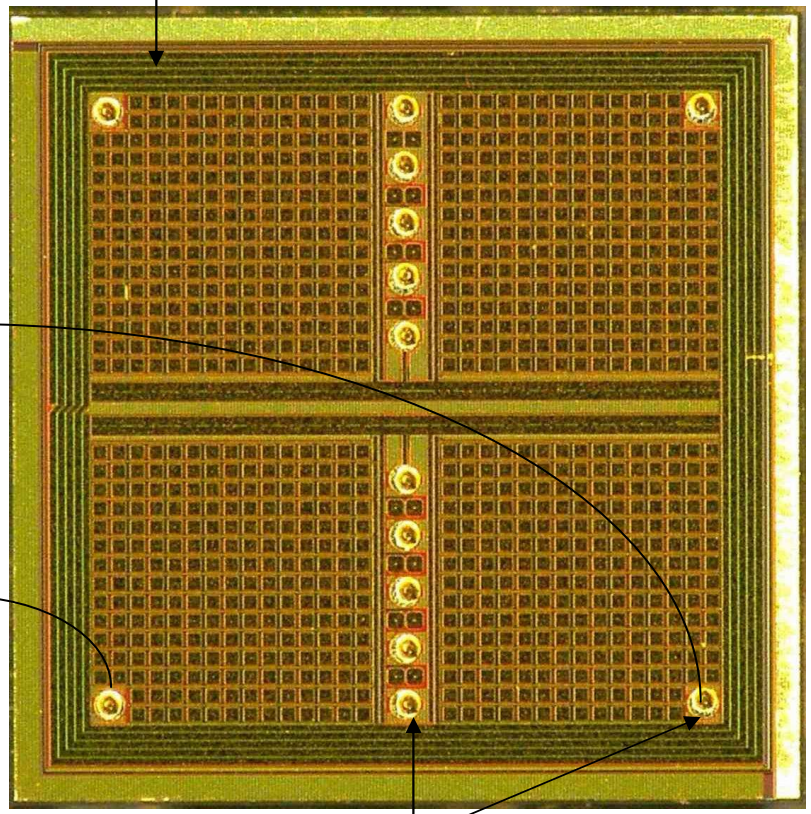
PRxelSensor elgctrbdes grouped/by flip-chip sensor aspacedy famerpsby ROCs



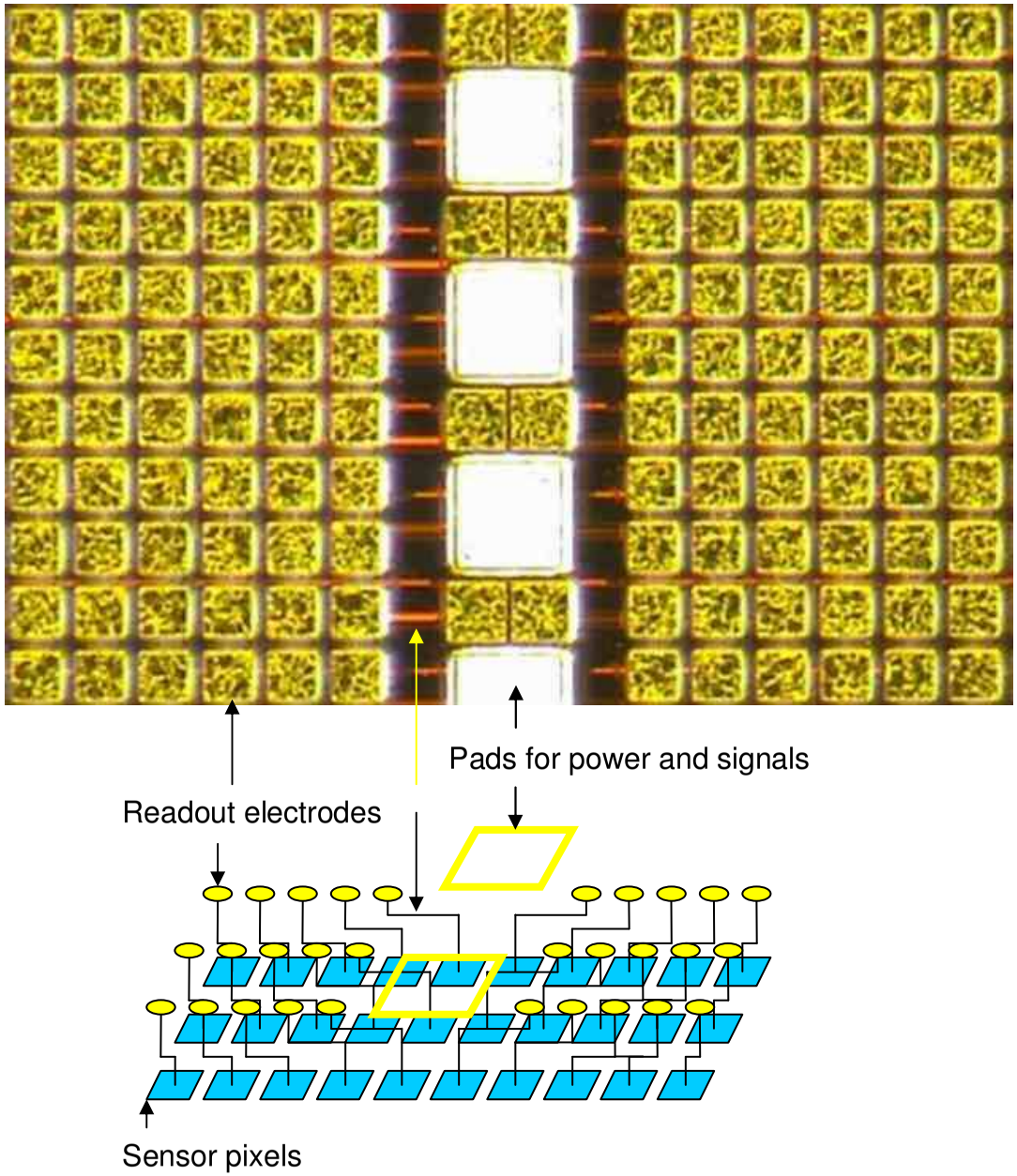
Chip on the sensor concept (CCPD2)



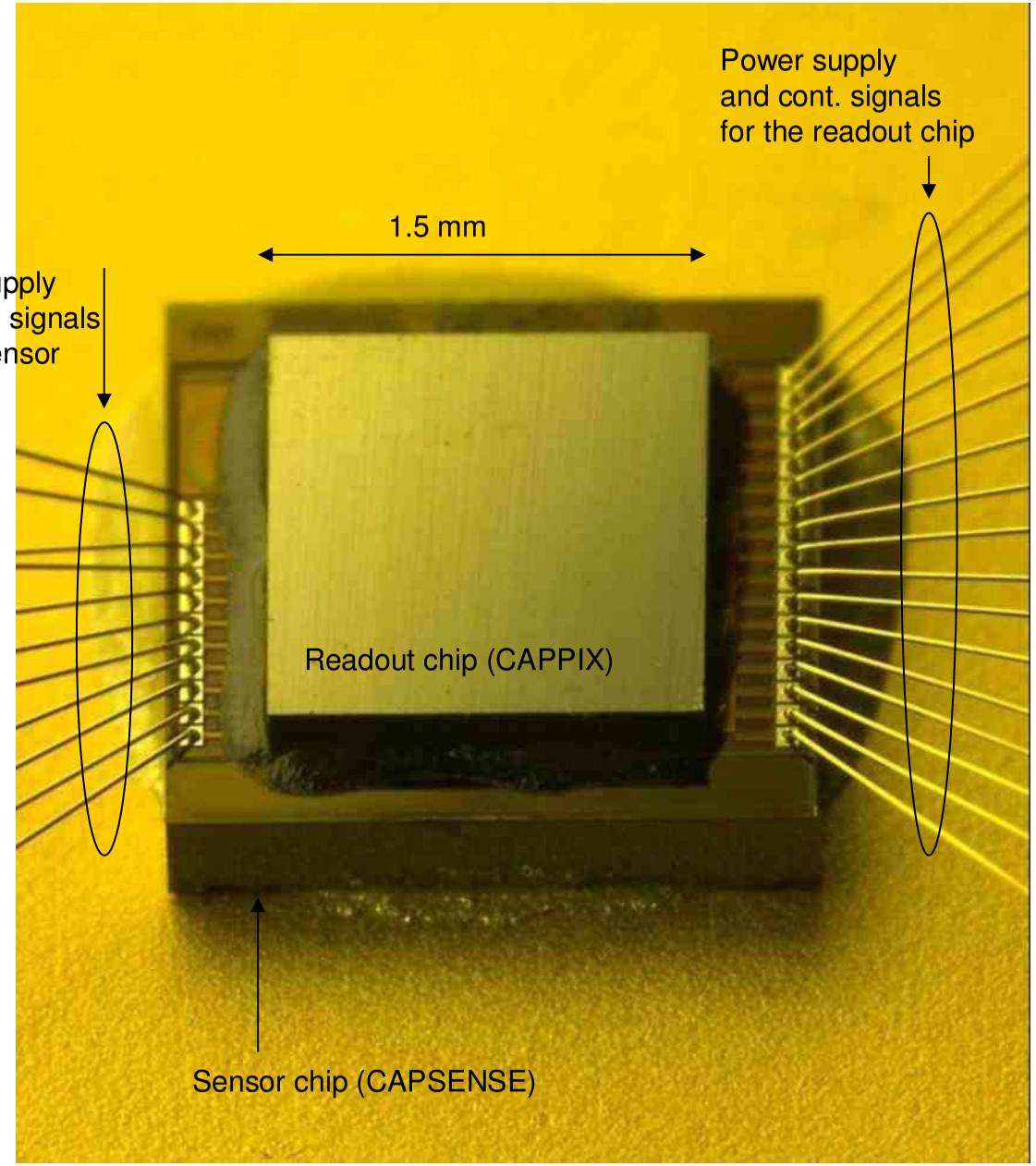
CAPSENSE



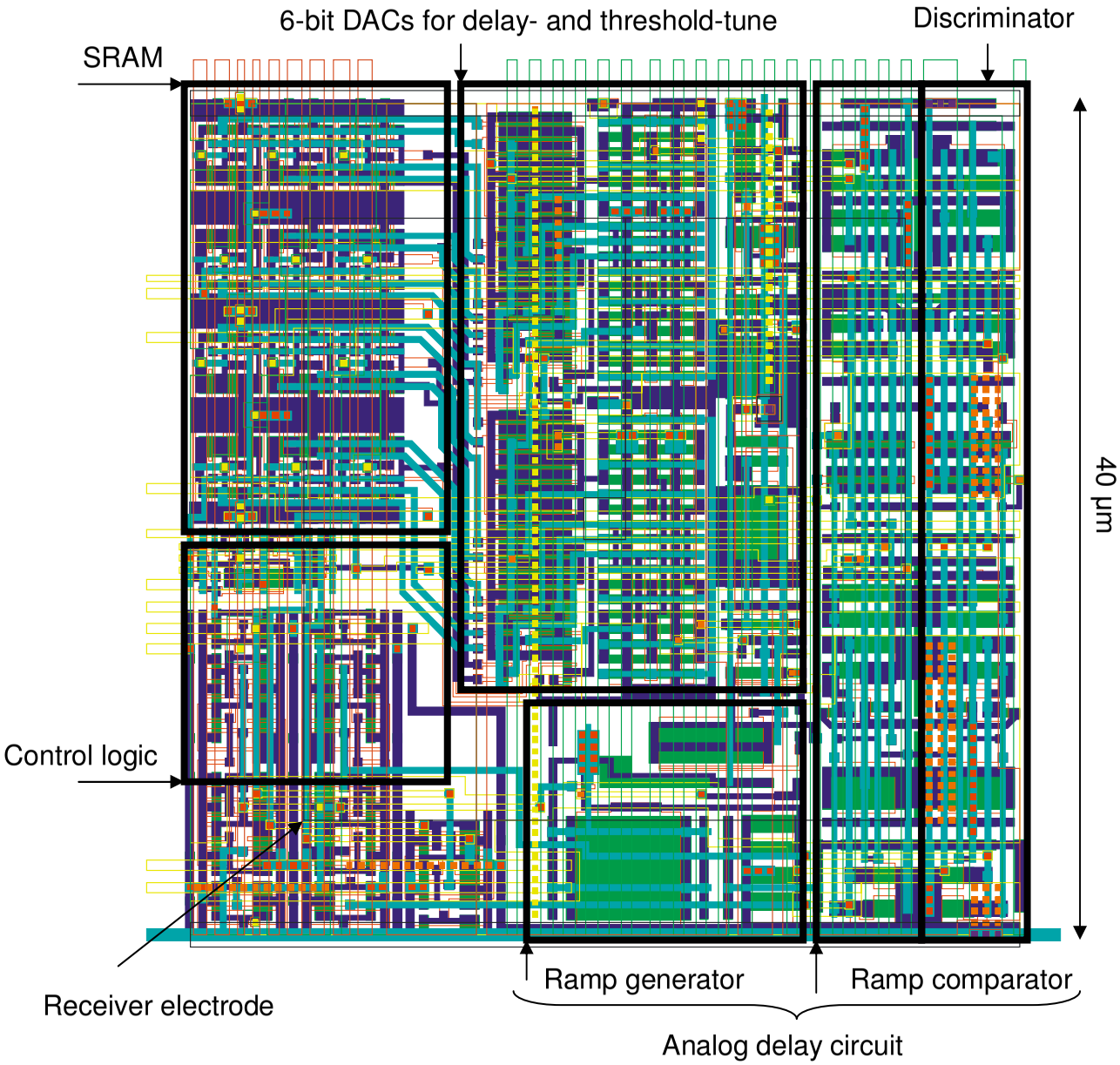
Chip on sensor concept



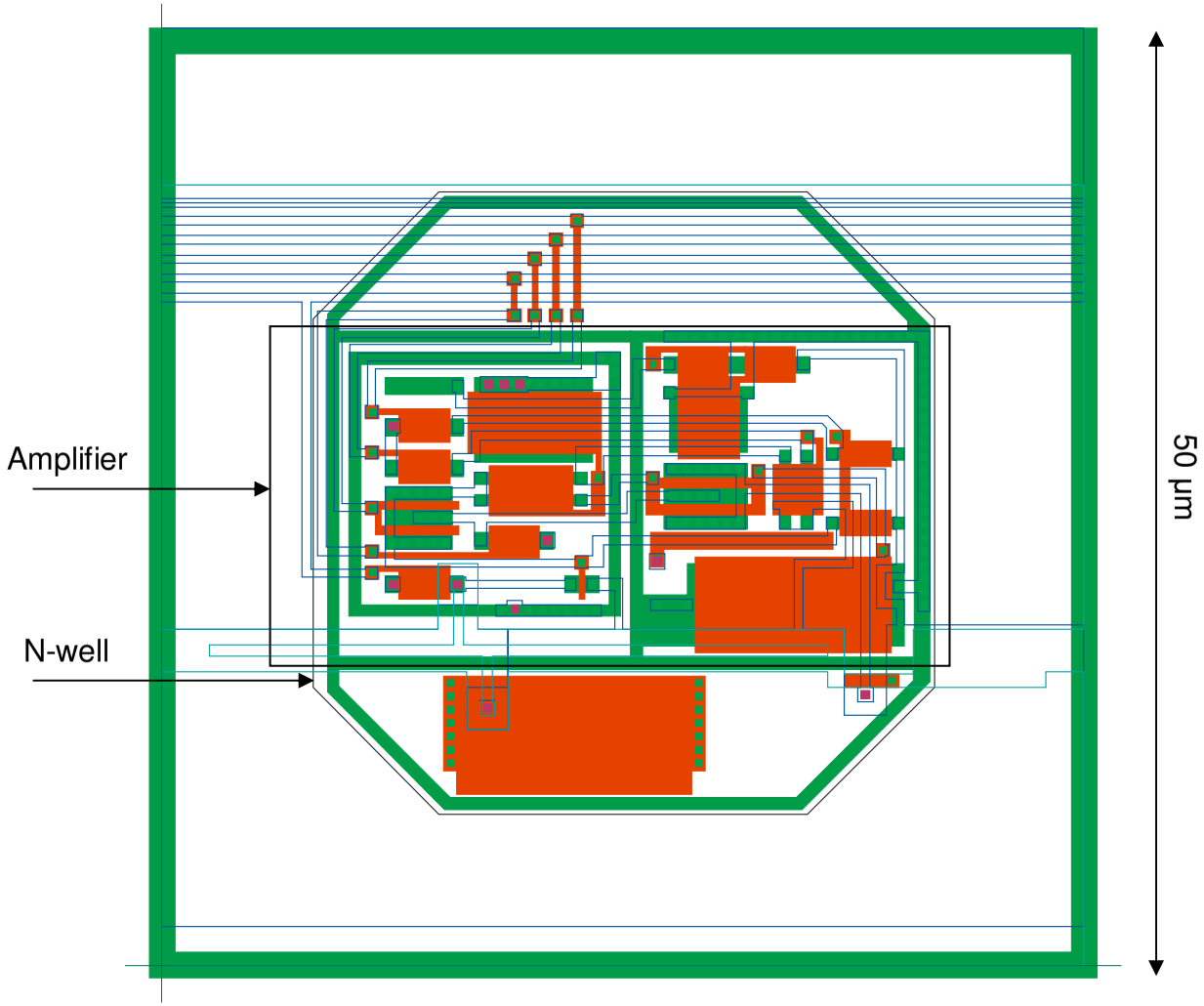
CCPD2 detector



CCPD2 readout pixel layout

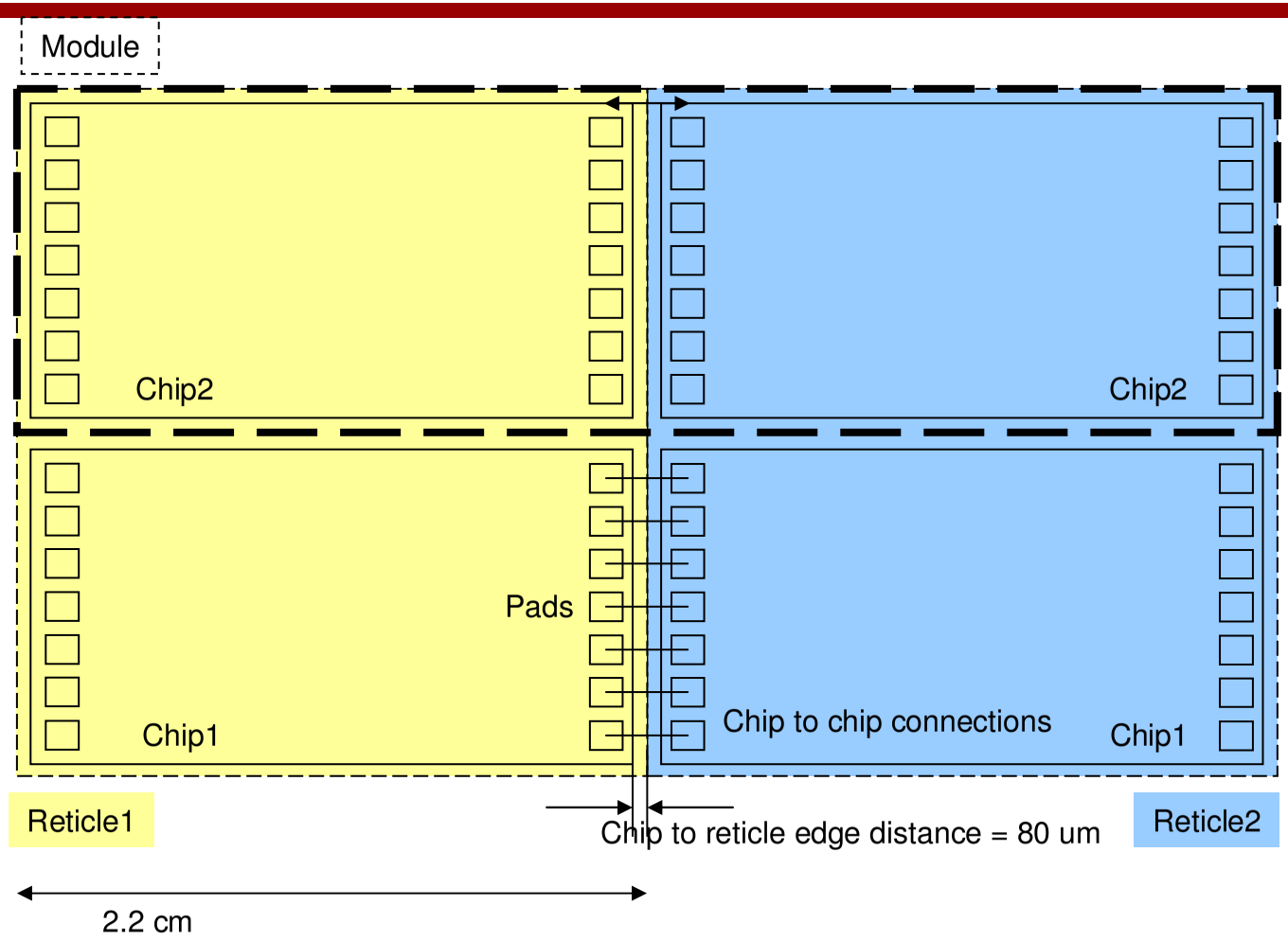


CCPD2 sensor pixel layout



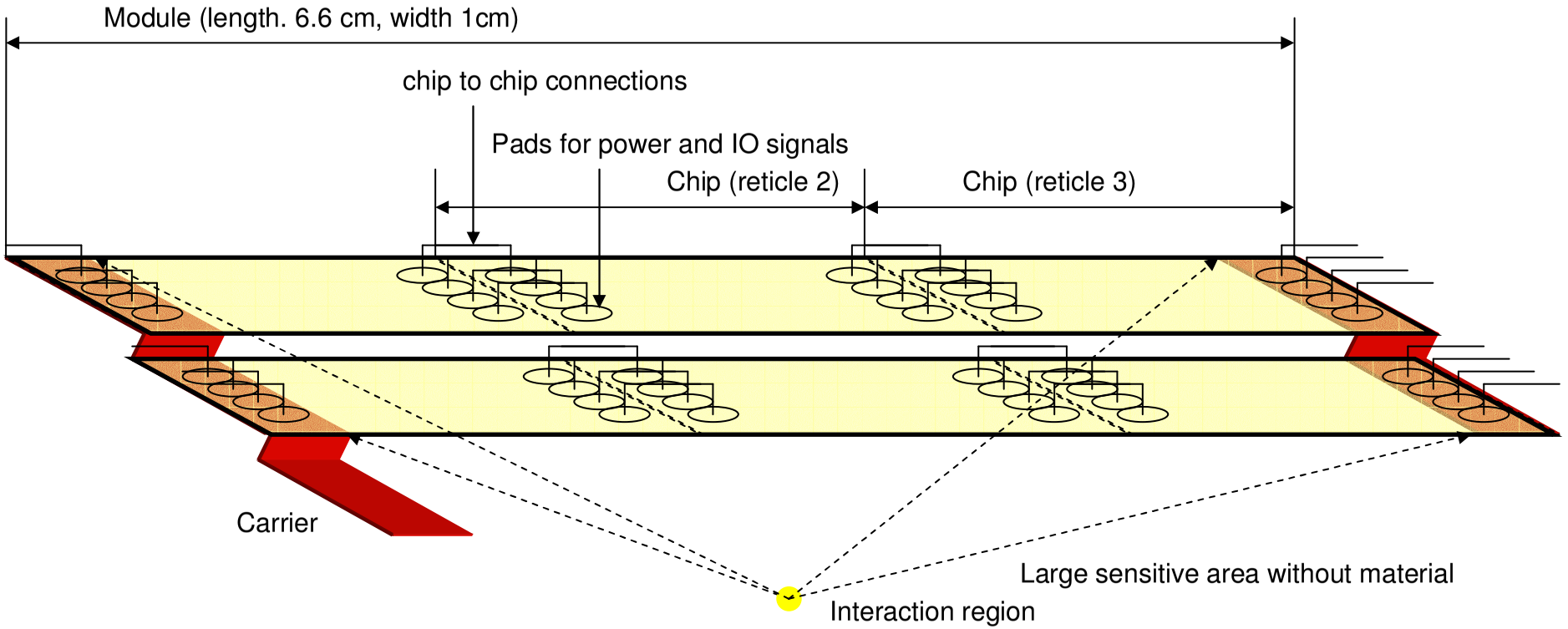
Large modules

Multi-reticle module



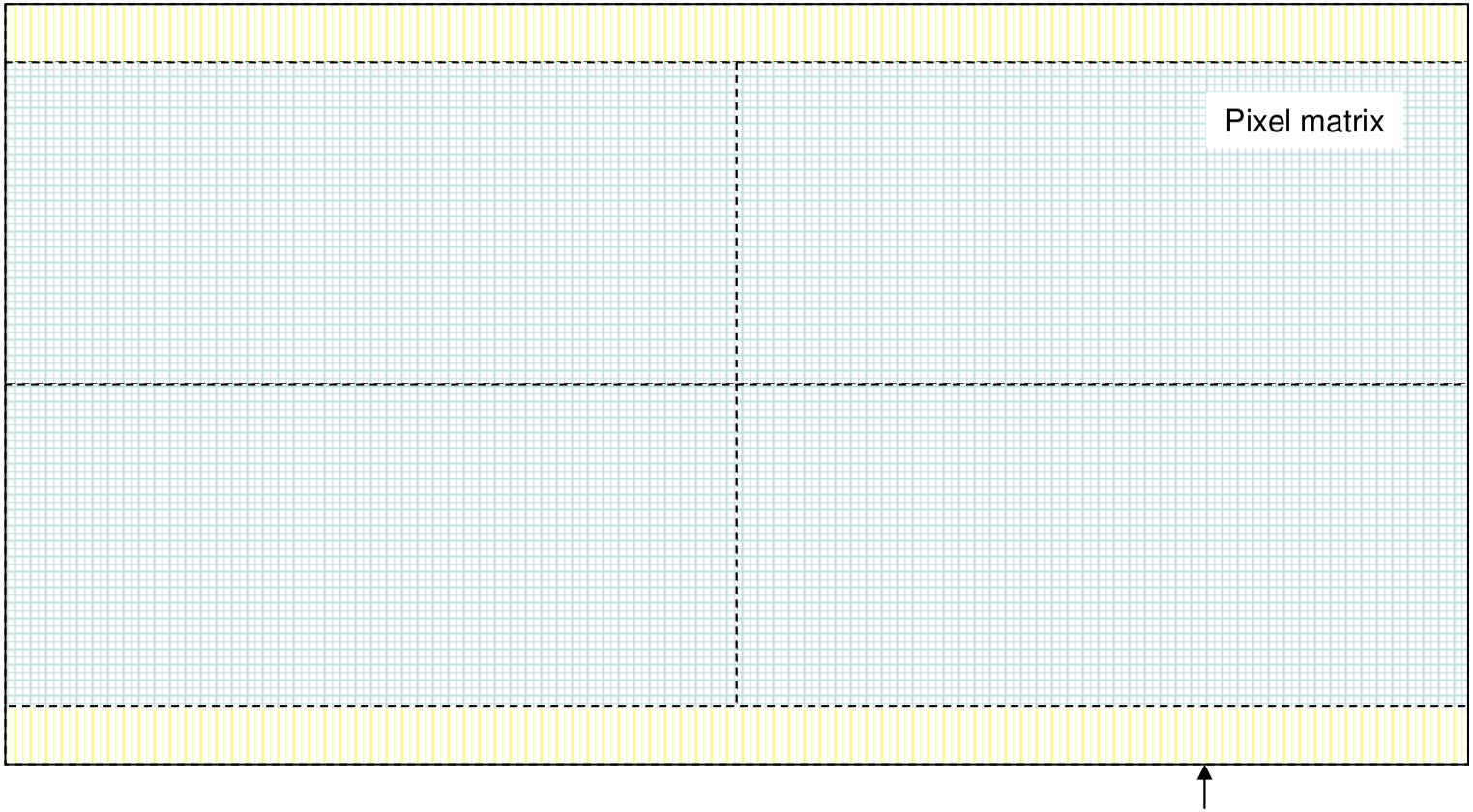
Very long low-cost pixel modules with (almost) no insensitive area can be produced
Reticle-reticle connections can be made easily by wire bonding
Instead of wire-bonding, an extra metal layer can be used as well

Multi-reticle module



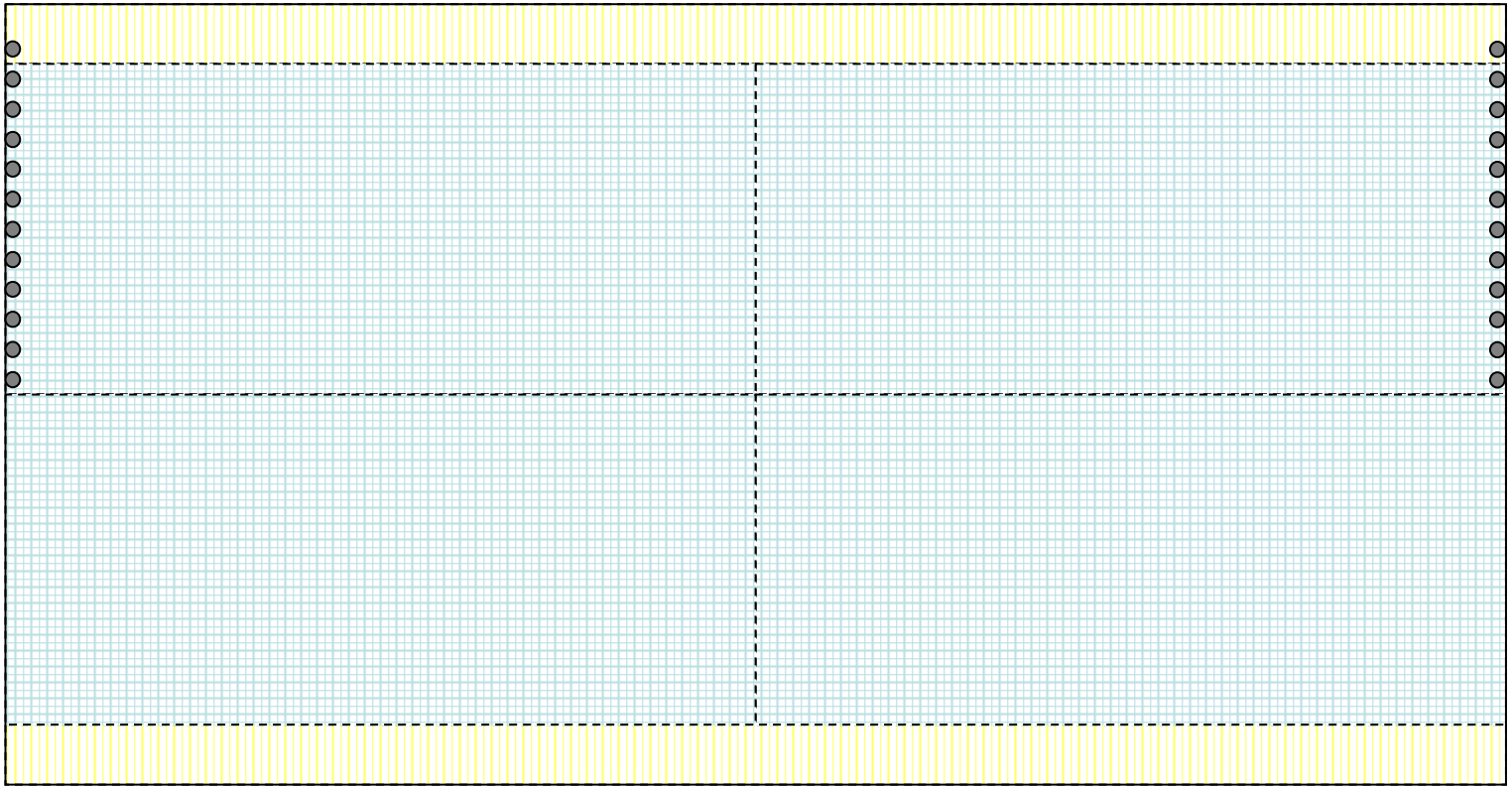
Very low-mass only silicon modules are possible as well (similar to DEPFET module for Belle II)

SDS long module



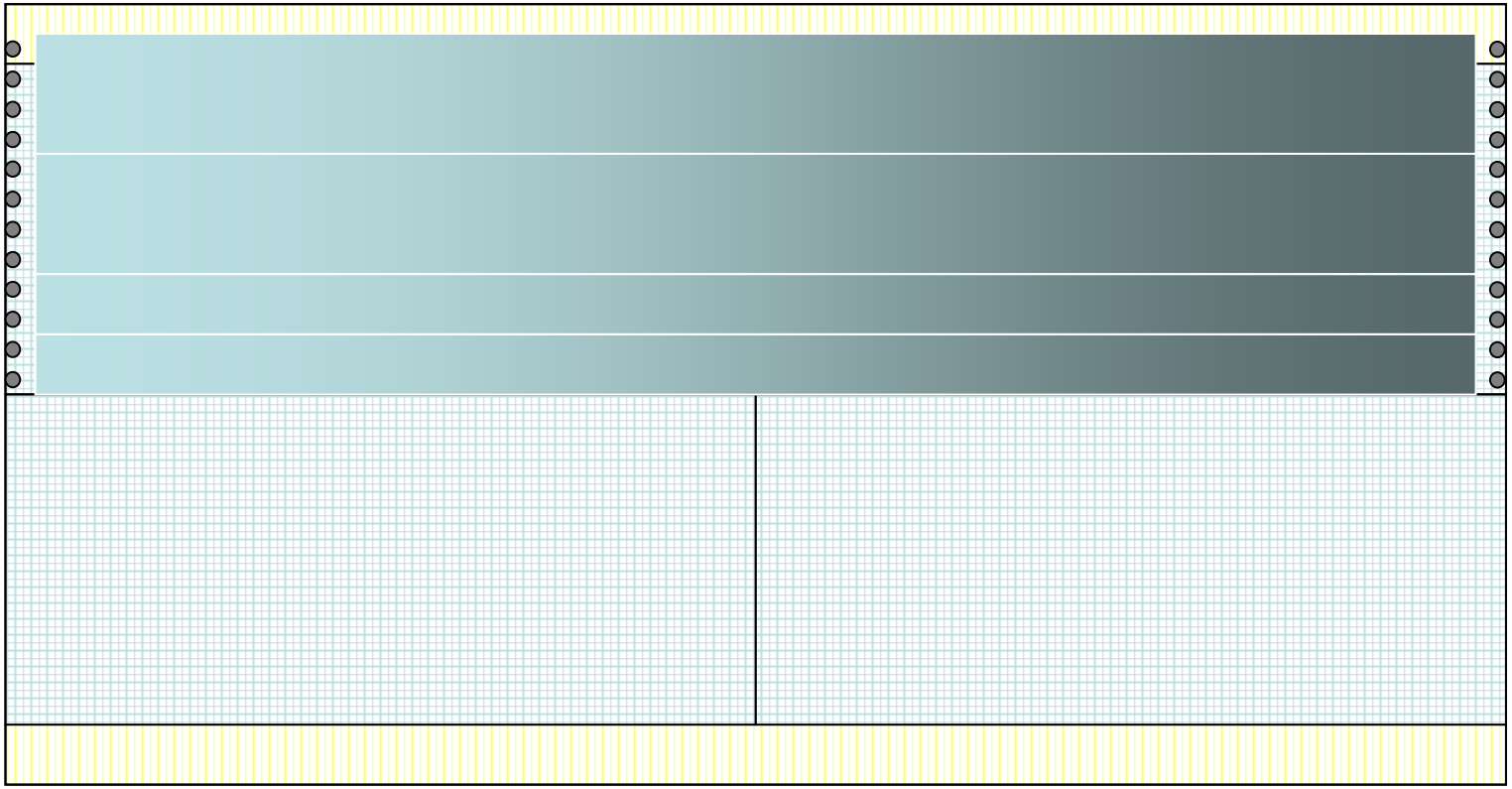
Pixel matrix and readout channels

SDS long module



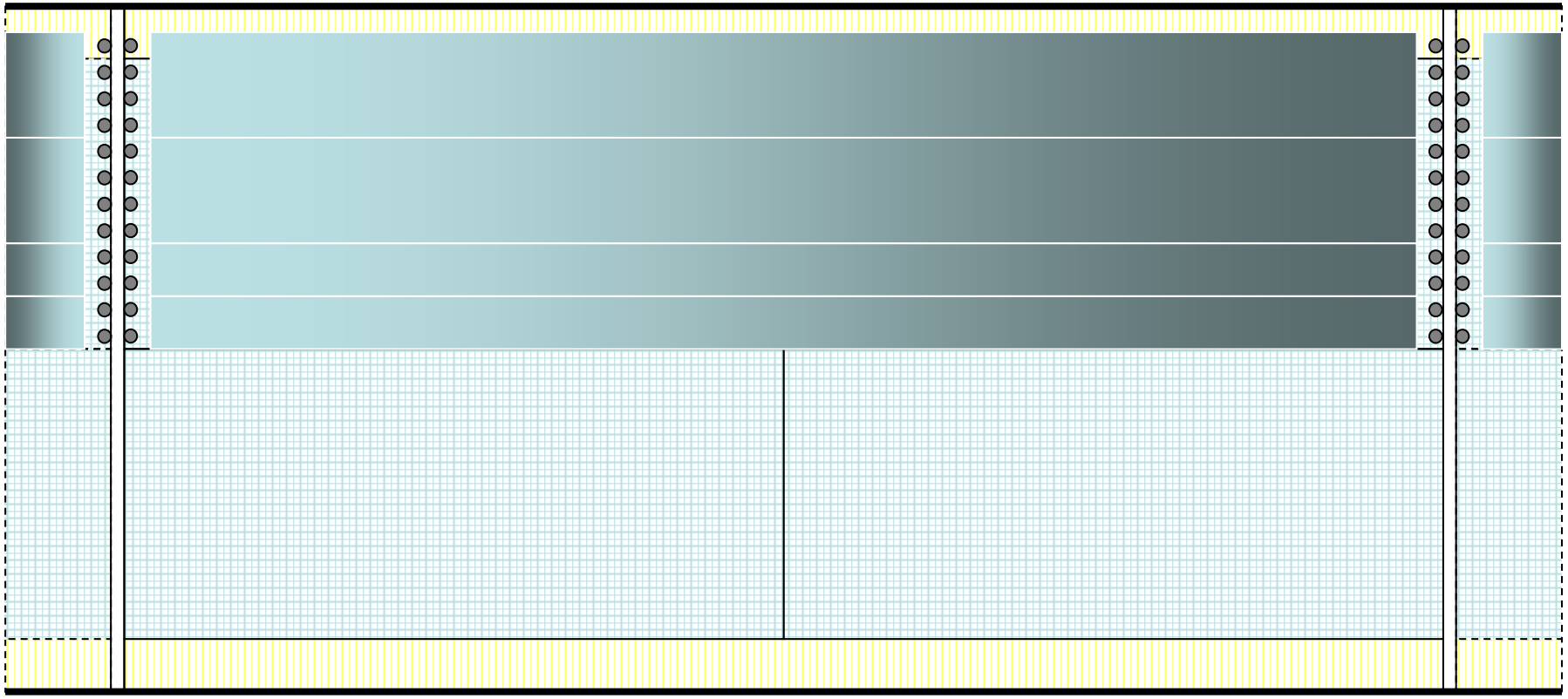
Pads for reticle-reticle connections

SDS long module



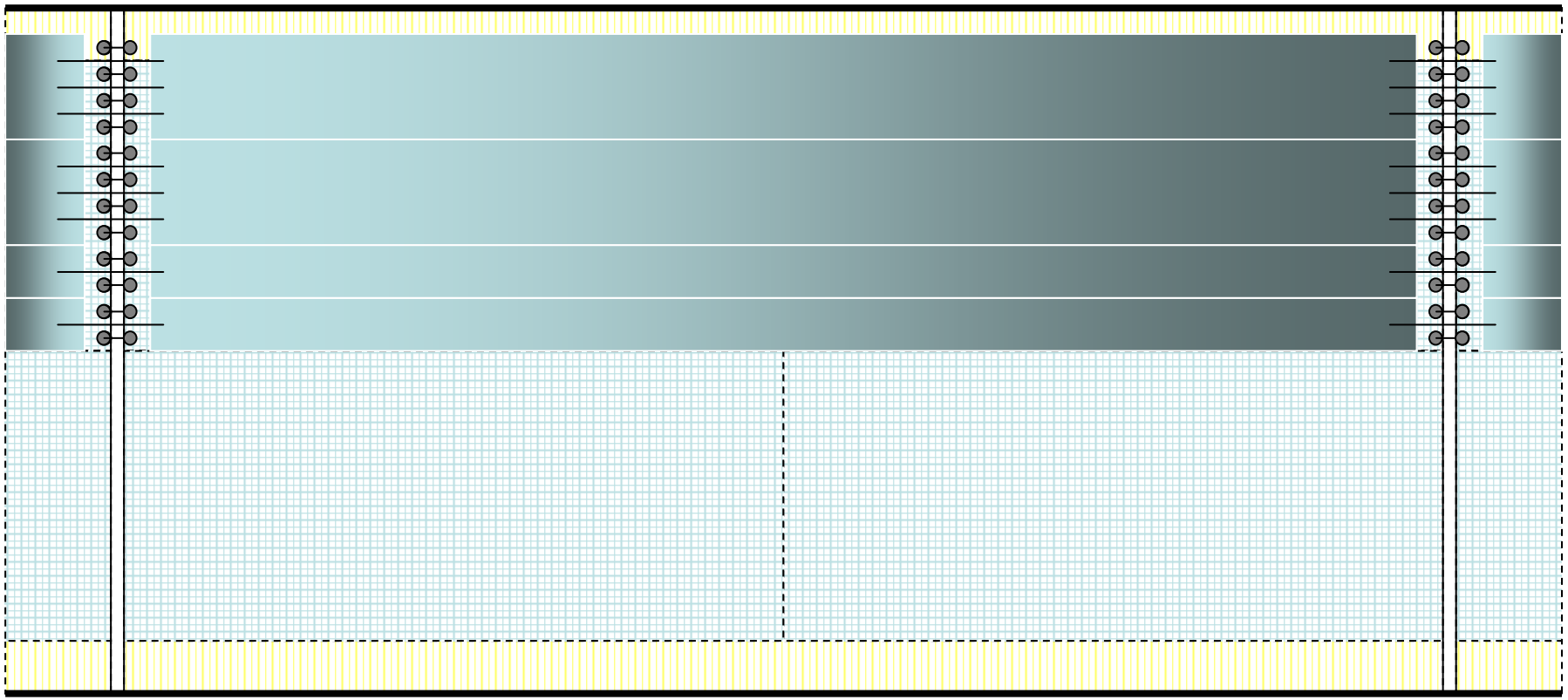
Power lines in the low-resistance last metal layer

SDS long module



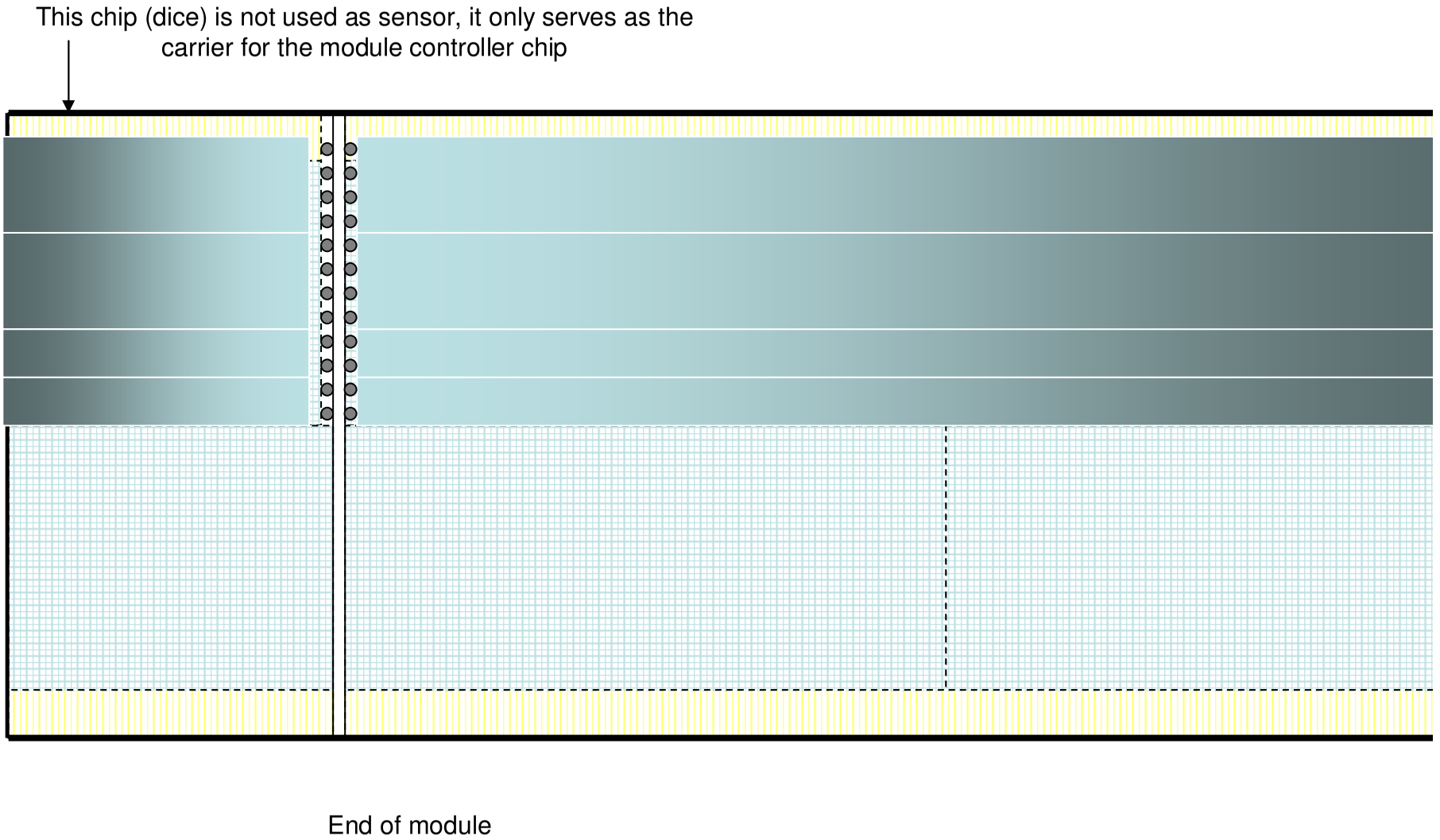
Pads for reticle-reticle connections

SDS long module

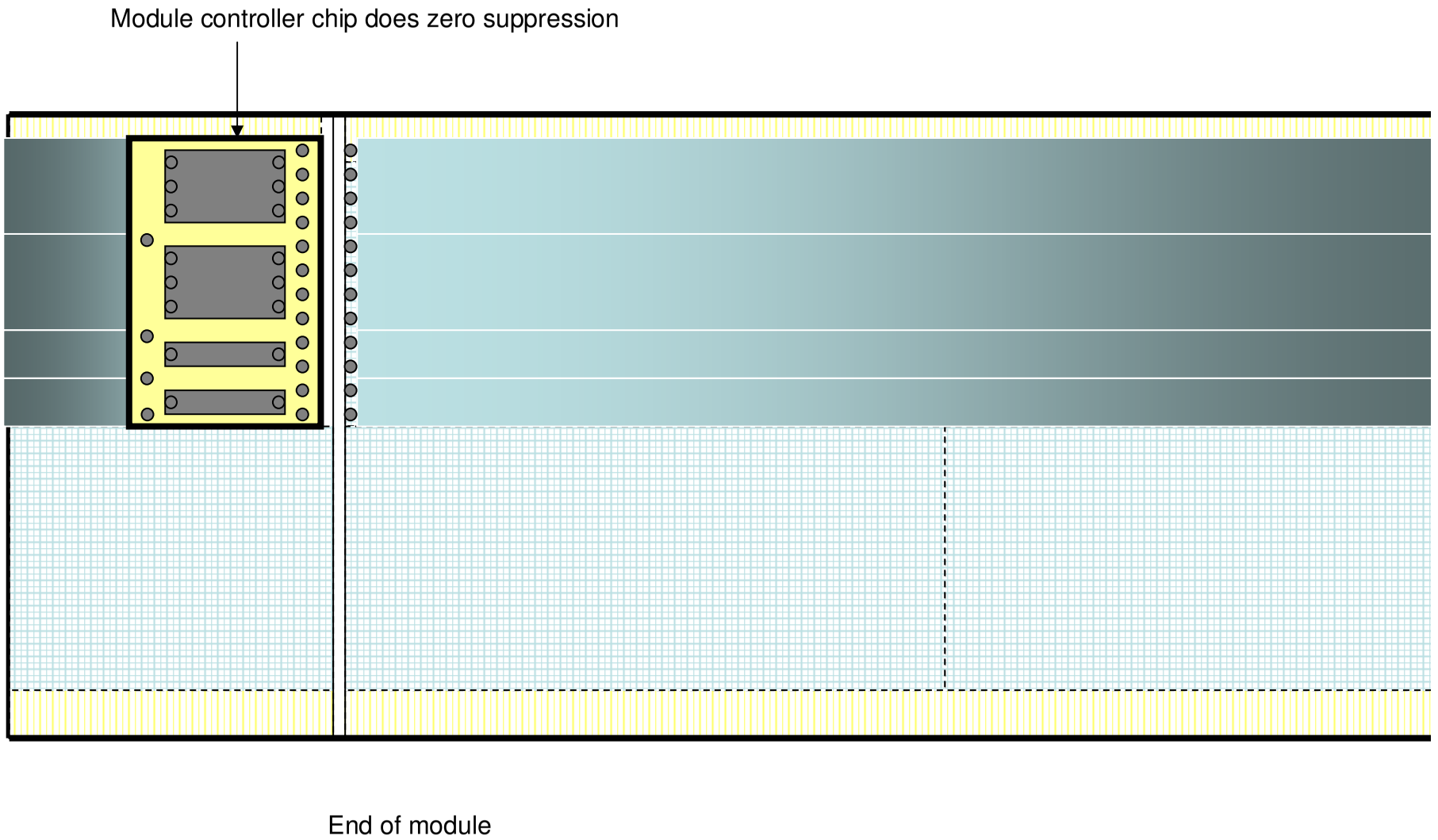


The pads can be connected by wire bonding or some more sophisticated technology

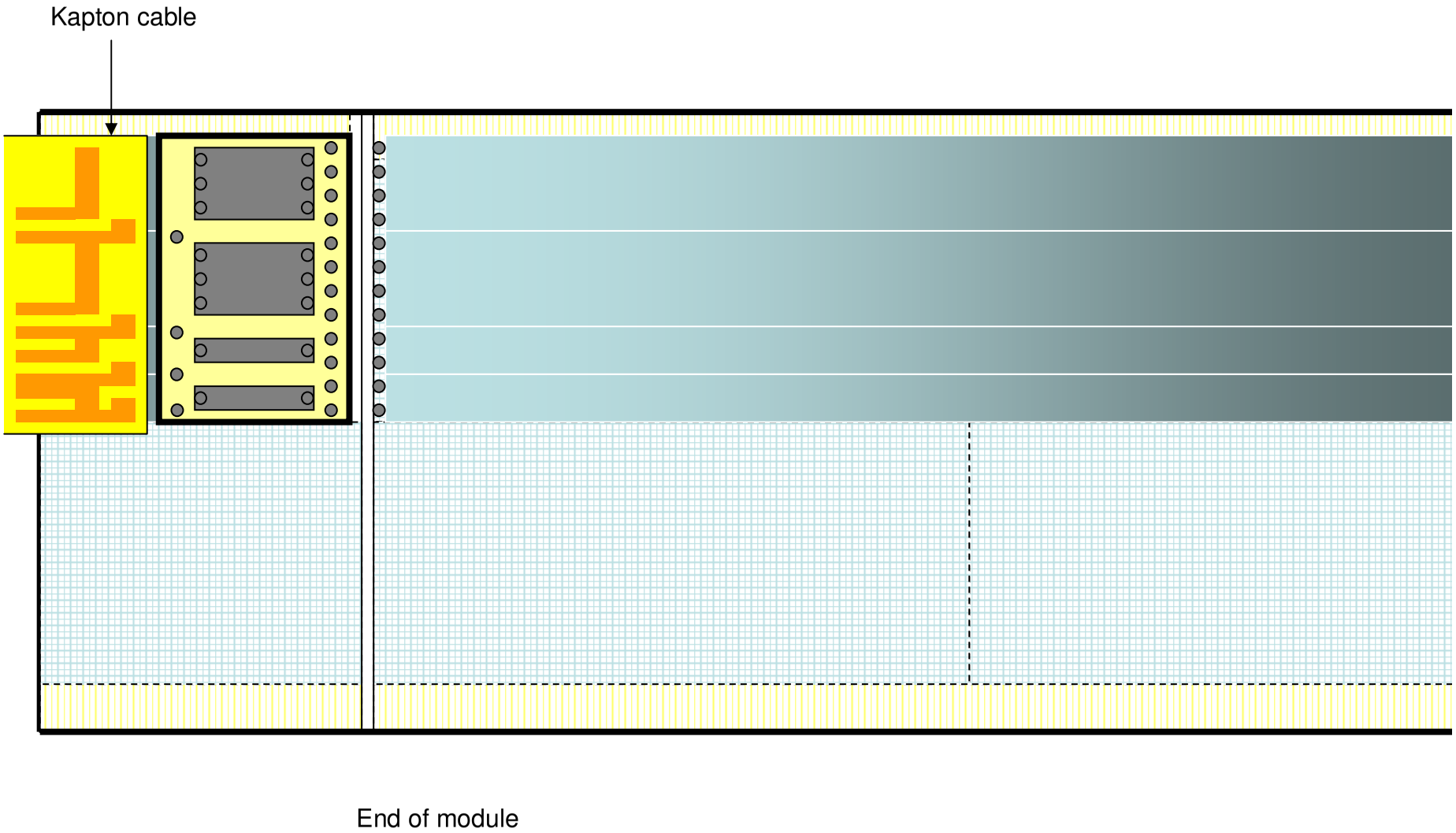
SDS long module



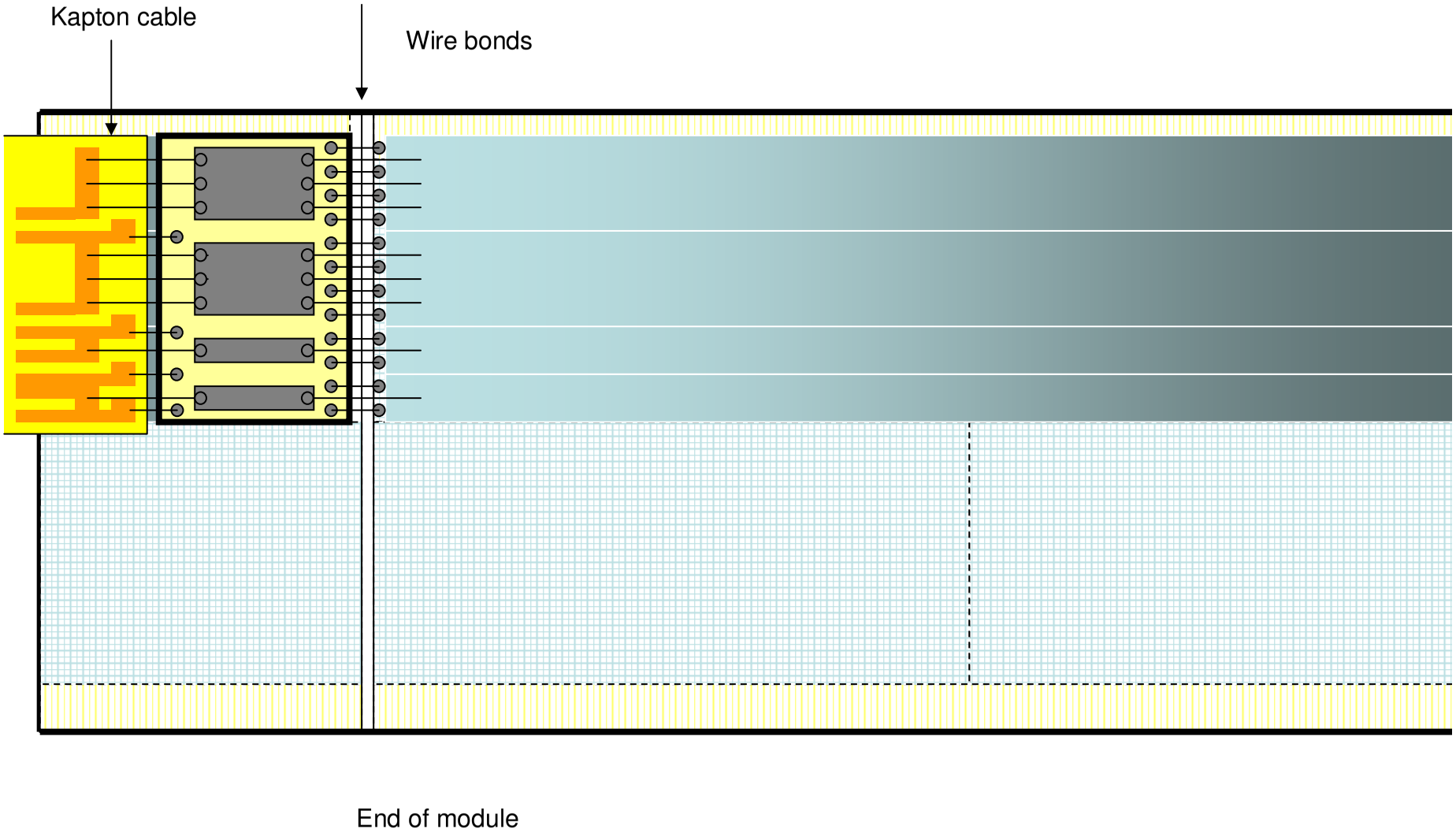
SDS long module



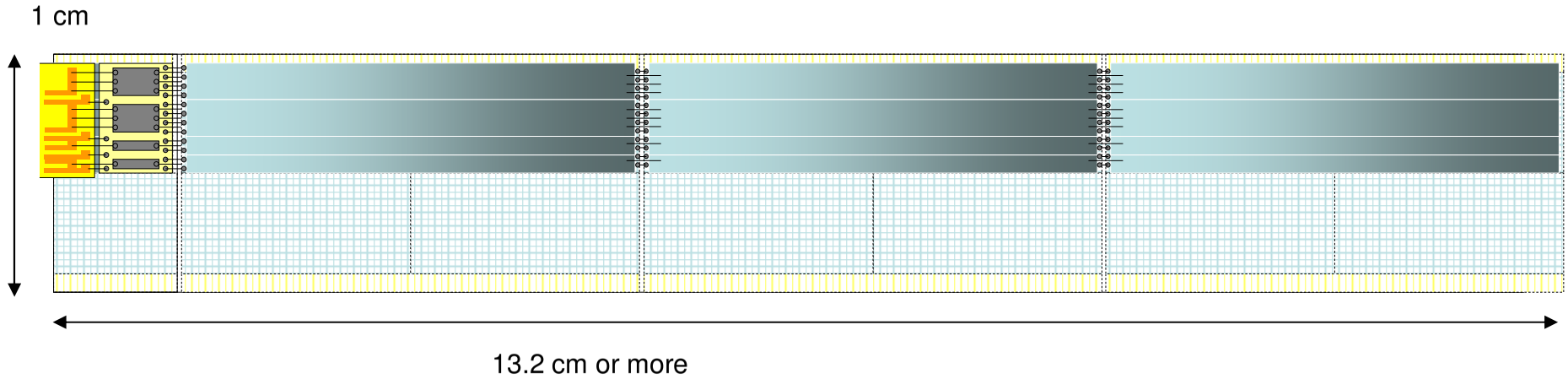
SDS long module



SDS long module

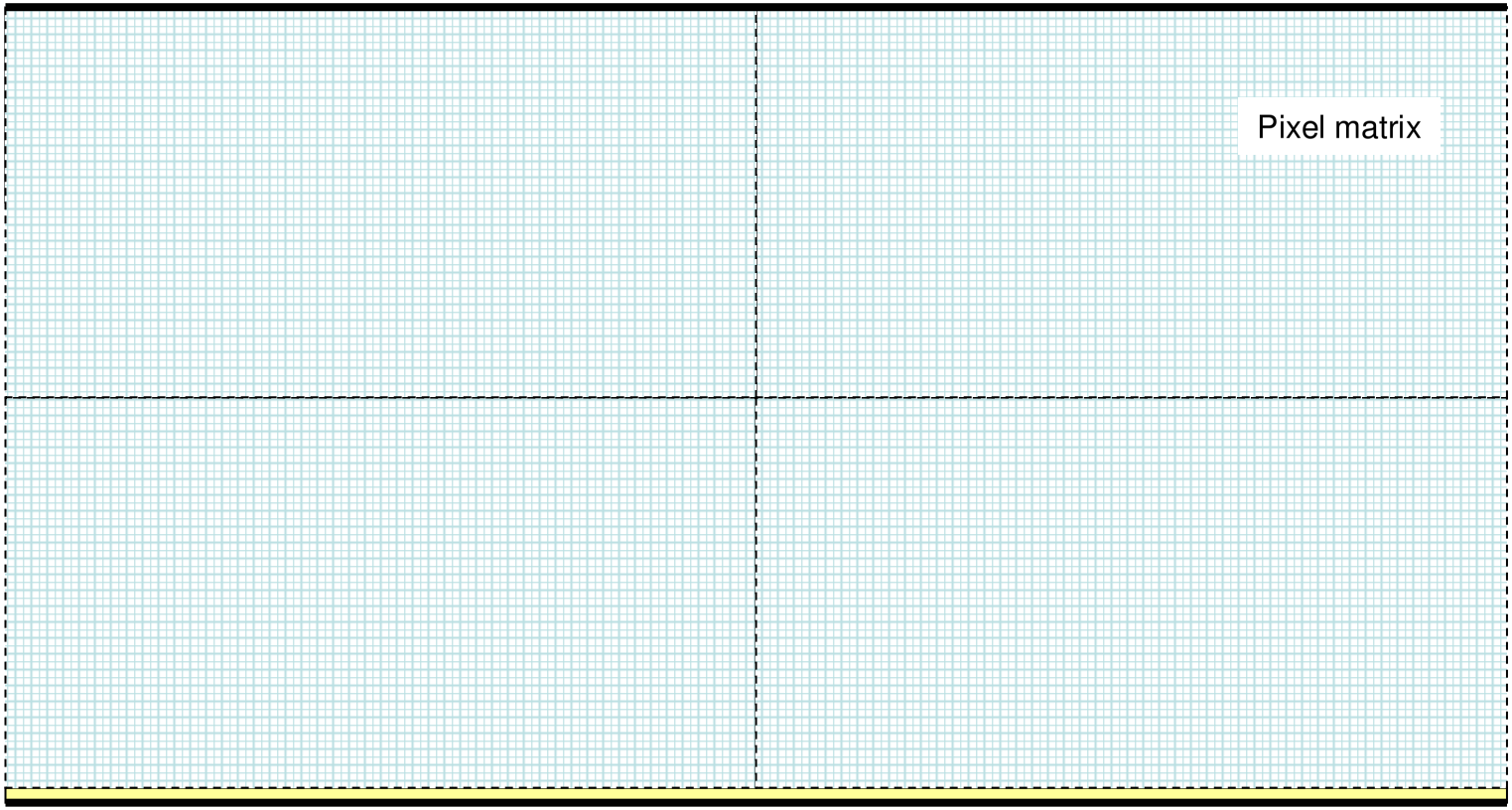


SDS long module



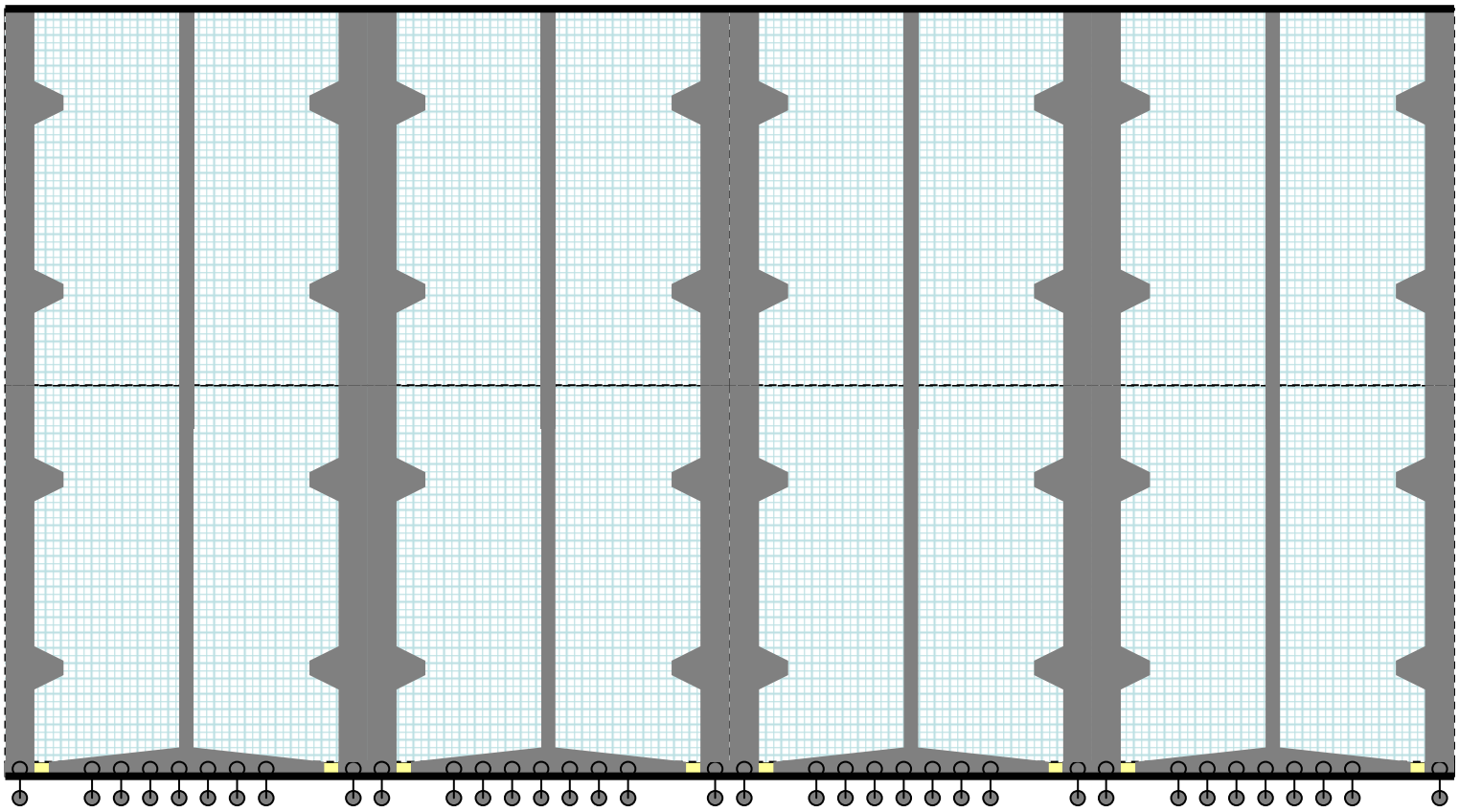
Thickness: below 50 μm possible
Easily achieved performances by scaling up of the present design:
Pixel size: 40 x 80 μm (or less)
Number of pixels: 256 x 768
Readout time: 40 μs
Radiation tolerance: at least 10^{15} n_{eq} and 60 Mrad
Power consumption (~frame rate): 2 W/module (10 μW/pixel)

CCPD long module



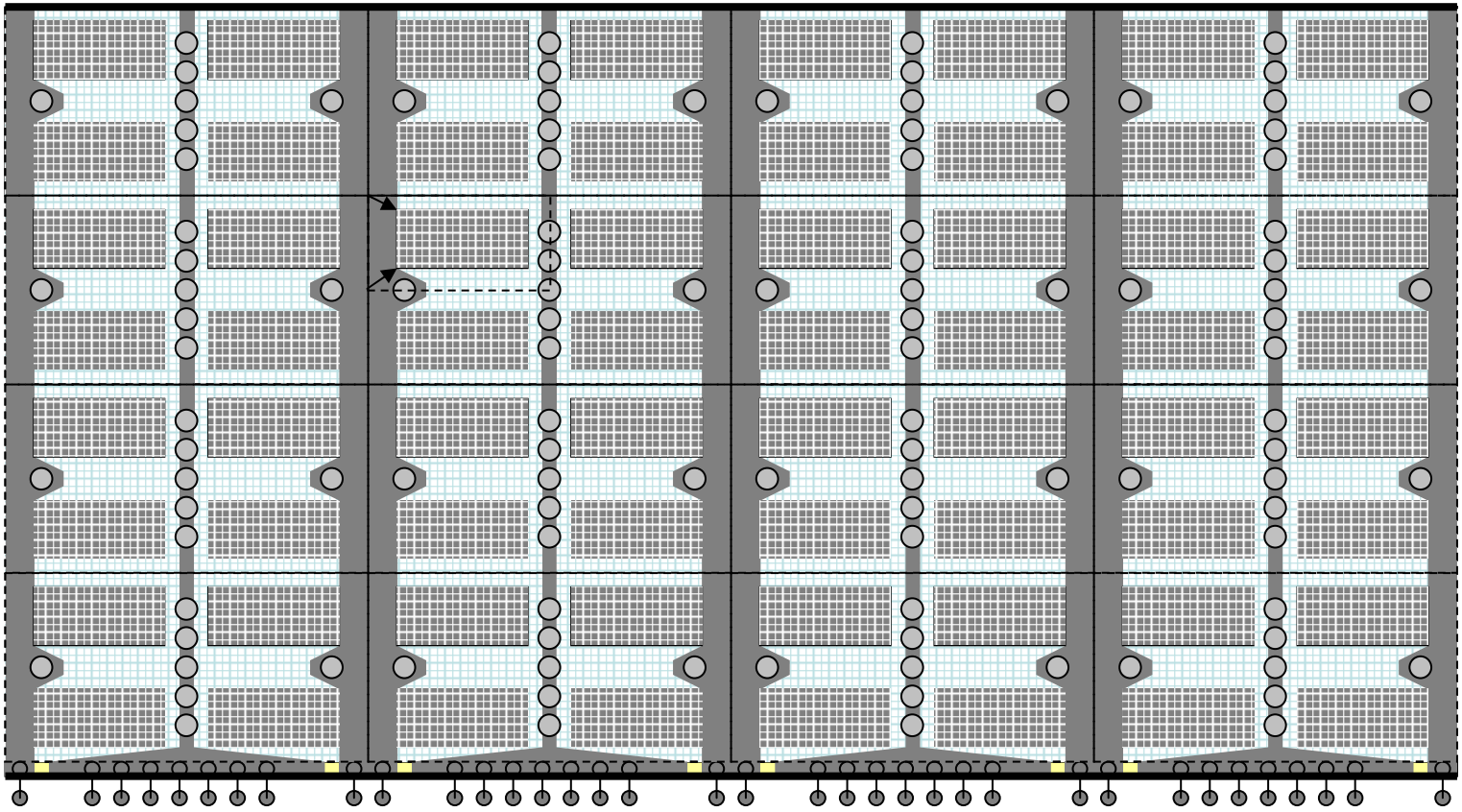
CCPD sensor matrix

CCPD long module



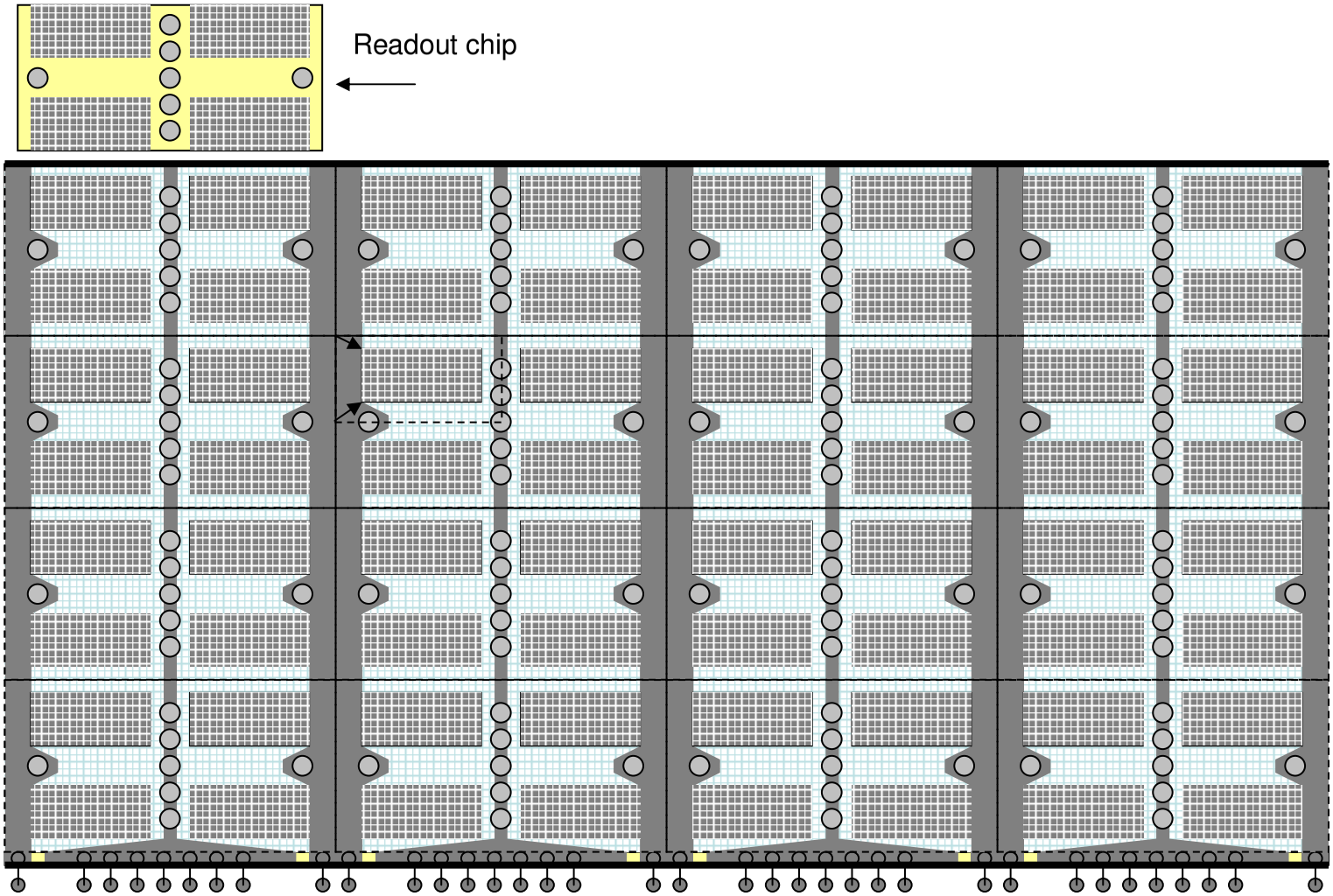
Connections for the power and signals

CCPD long module



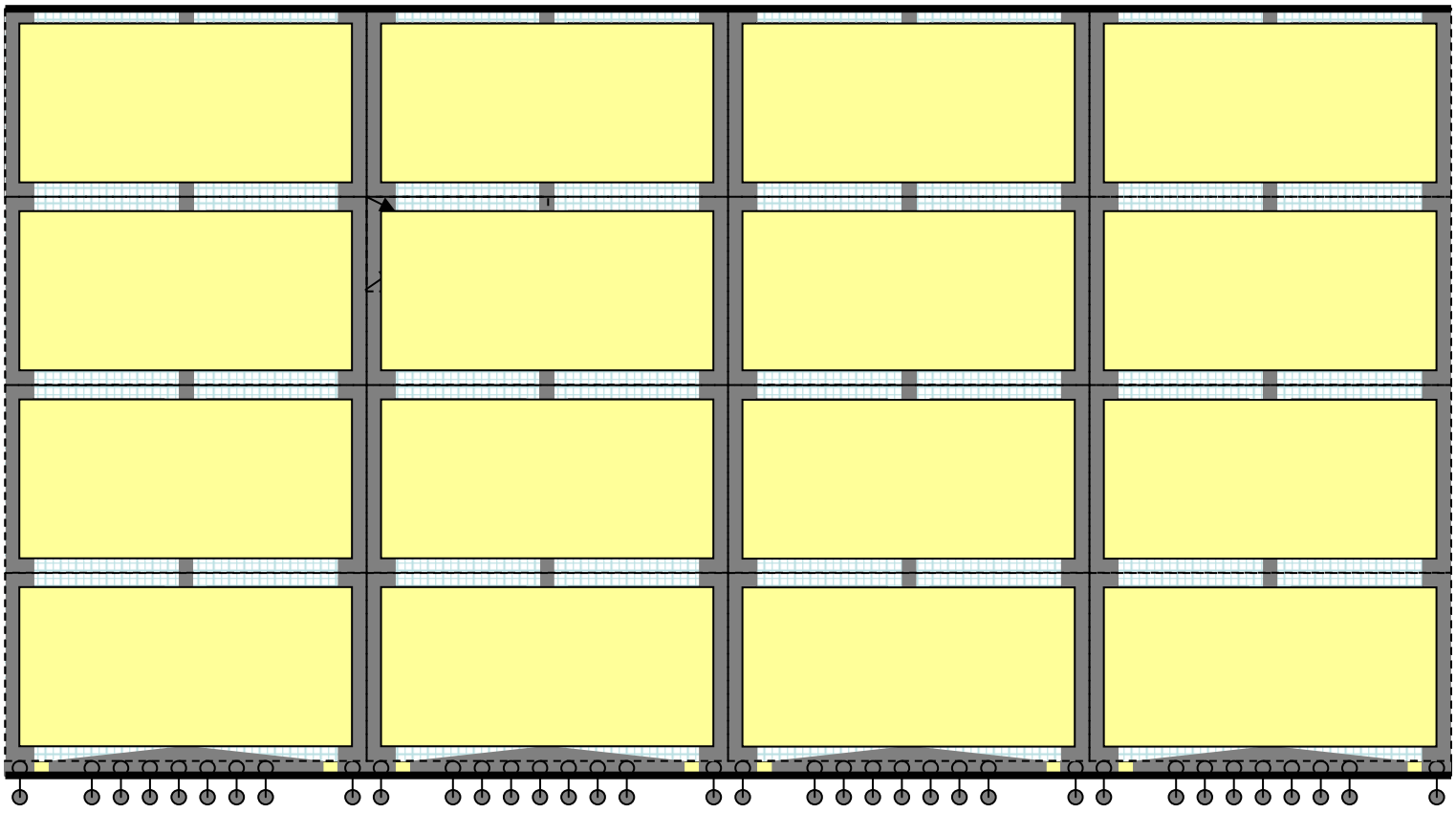
Arrays of electrodes for capacitive signal transmission

CCPD long module



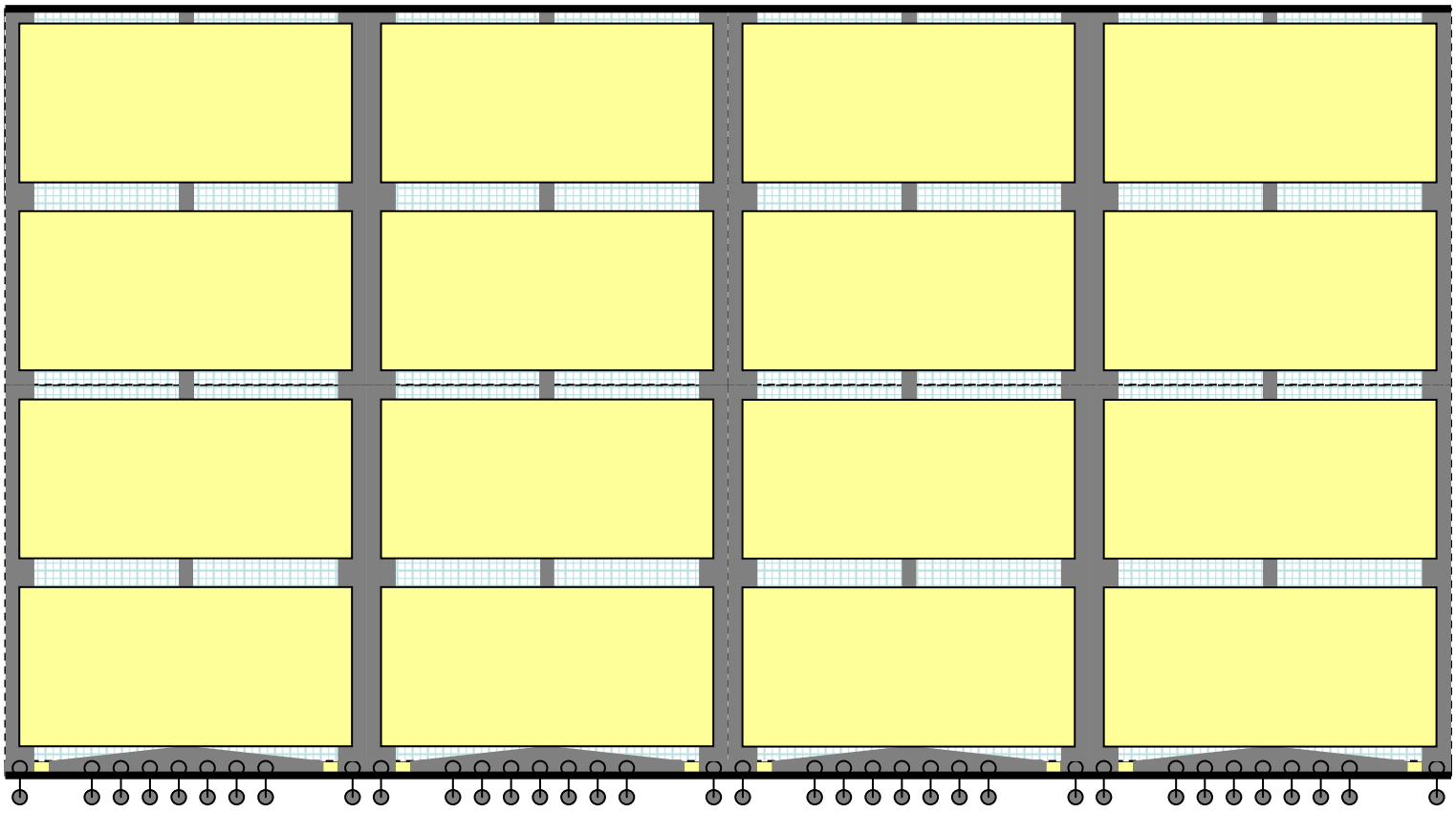
Readout chips are connected by a few bumps – typically 16/chip
Every readout chip has 64 x 64 pixels
Readout chips are produced in a deep submicron technology

CCPD long module



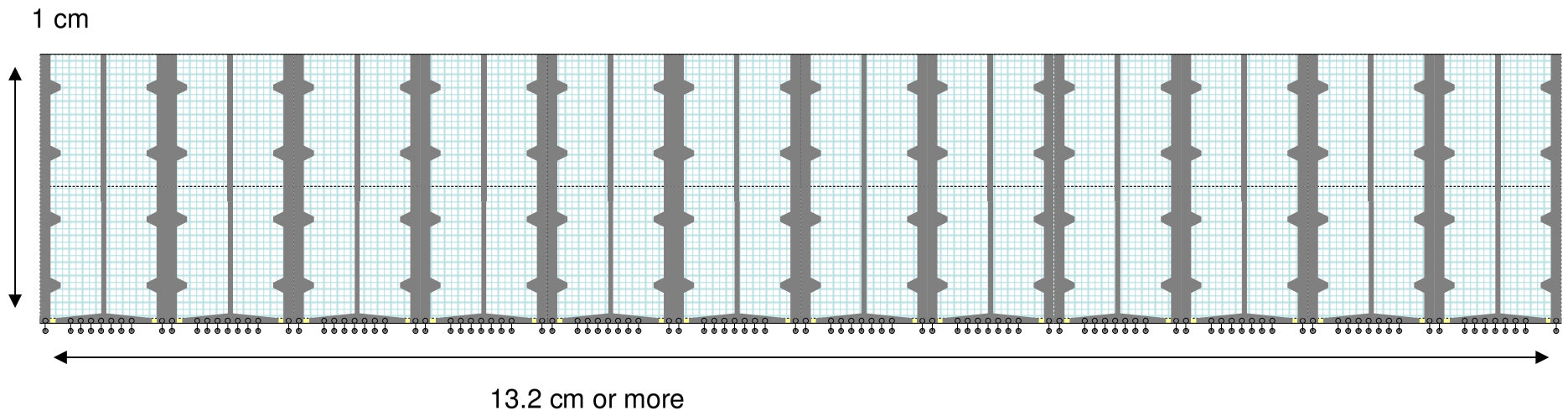
16 readout chips / module segment (reticle)

CCPD long module



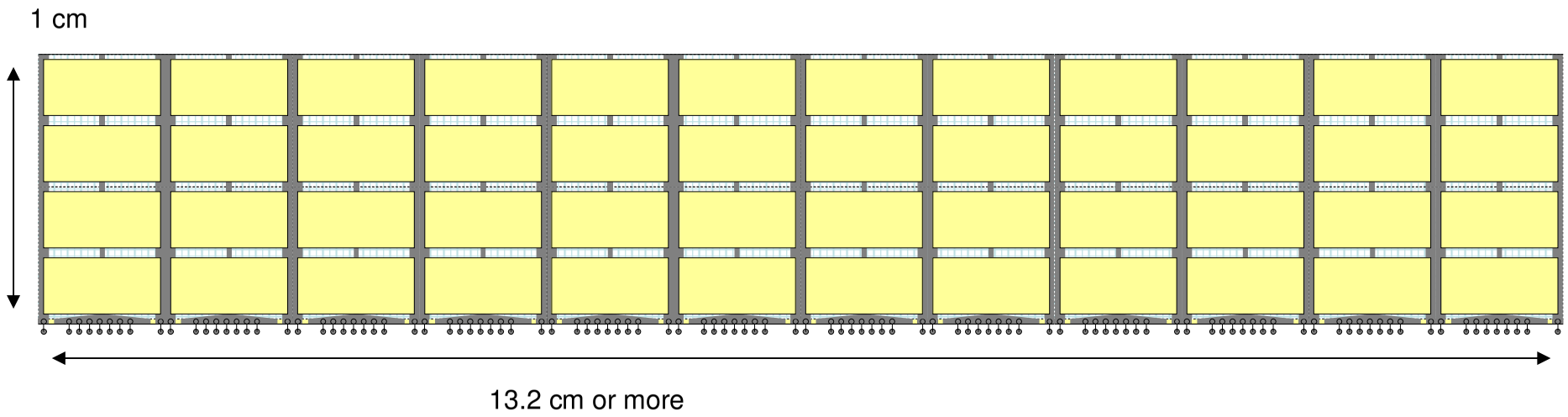
16 readout chips / module segment (reticle)

CCPD long module



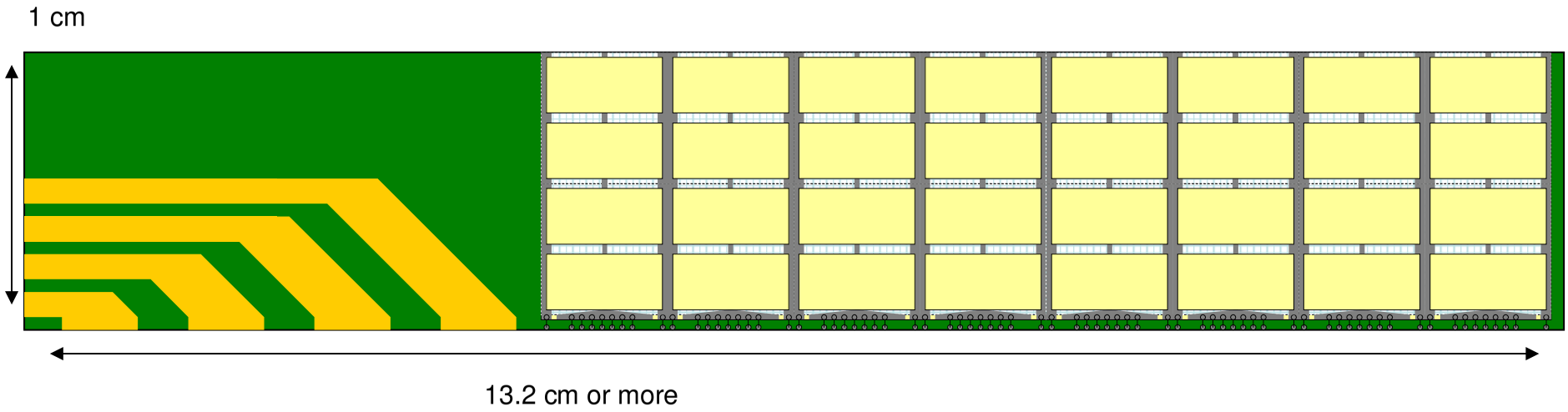
Full module consists of 3 reticles, no dead area

CCPD long module



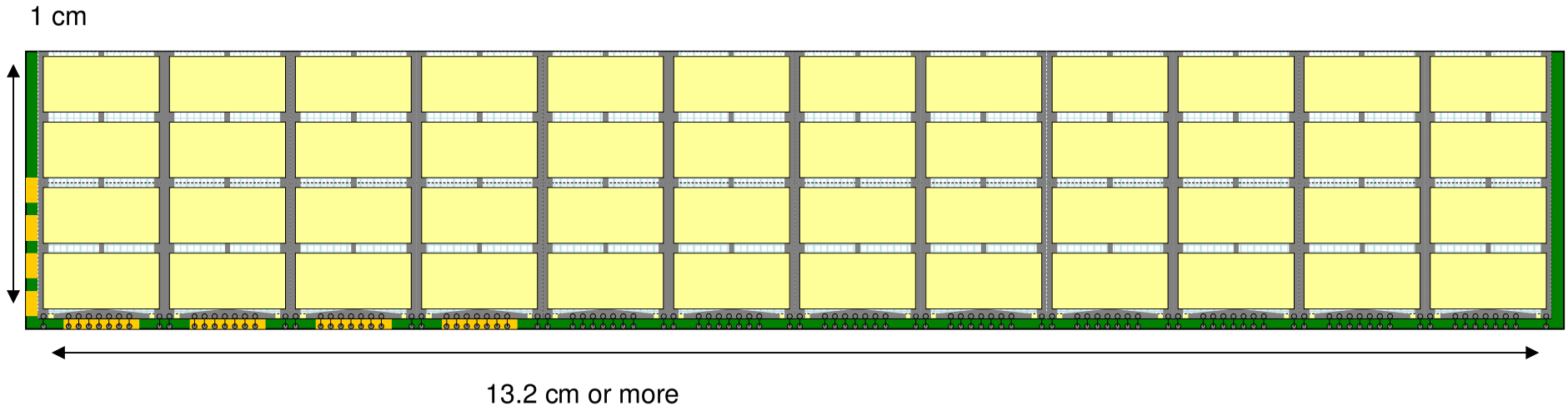
48 readout chips are needed for the full module

CCPD long module



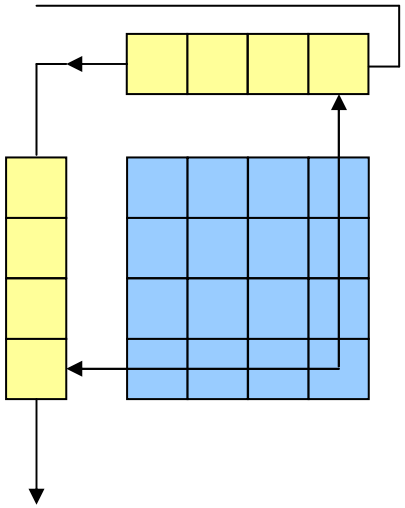
The module is glued onto kapton PCB
Module and kapton PCB are placed on a low-mass module carrier made e.g. of carbon material

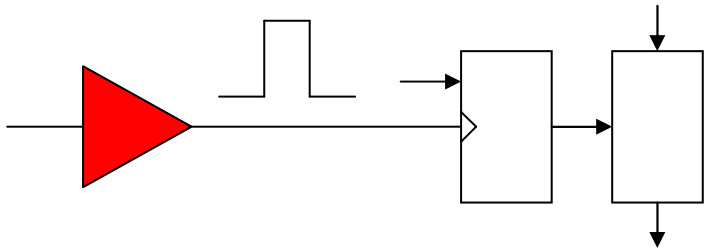
CCPD long module



Thickness: 100 μm (thinned sensor and readout chips)
Easily achieved performances by scaling up of the present design:
Pixel size: 40 x 80 μm (or smaller)
Number of pixels: 256 x 768
Time resolution: 300 ns
Power consumption: 3 W/module (15 μW/pixel)
Radiation tolerance: at least 10^{15} n_{eq} and 60 Mrad
Realistic readout time in the case of un-triggered readout: 1 μs

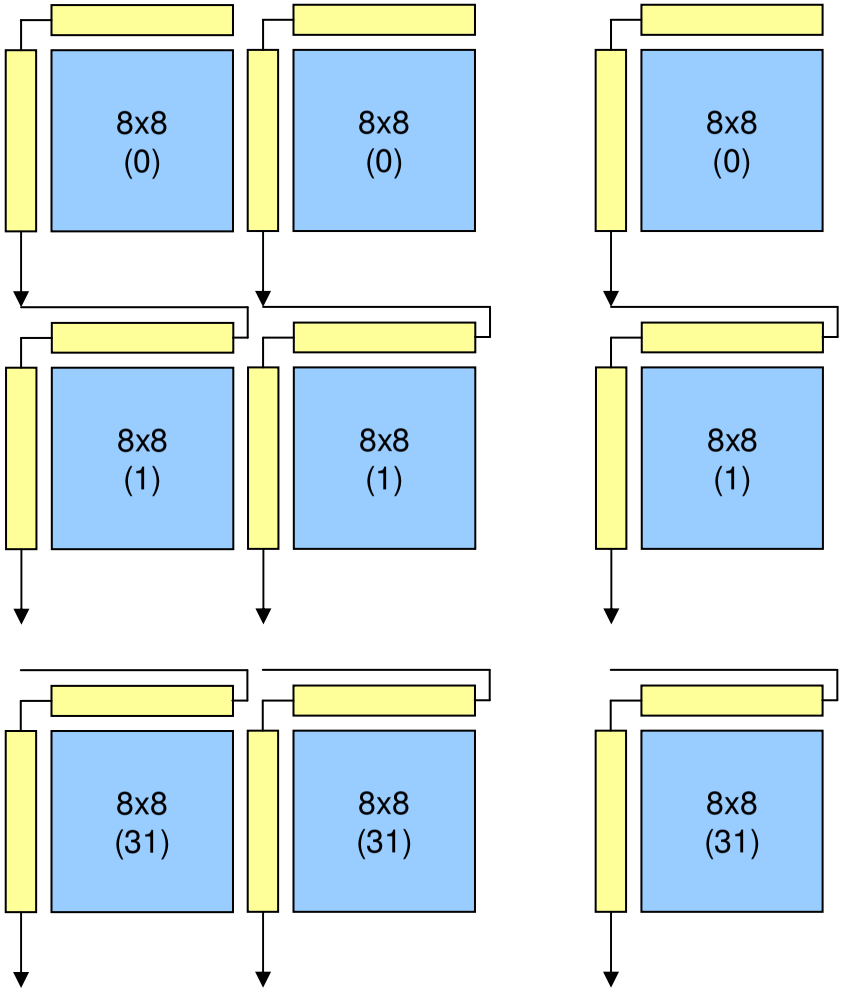
CCPD long module





The pixels are arranged in 4x4 pixel groups
Each group can be logically understood as a micro strip detector
Simple data reduction
Such a scheme could even work for SLHC

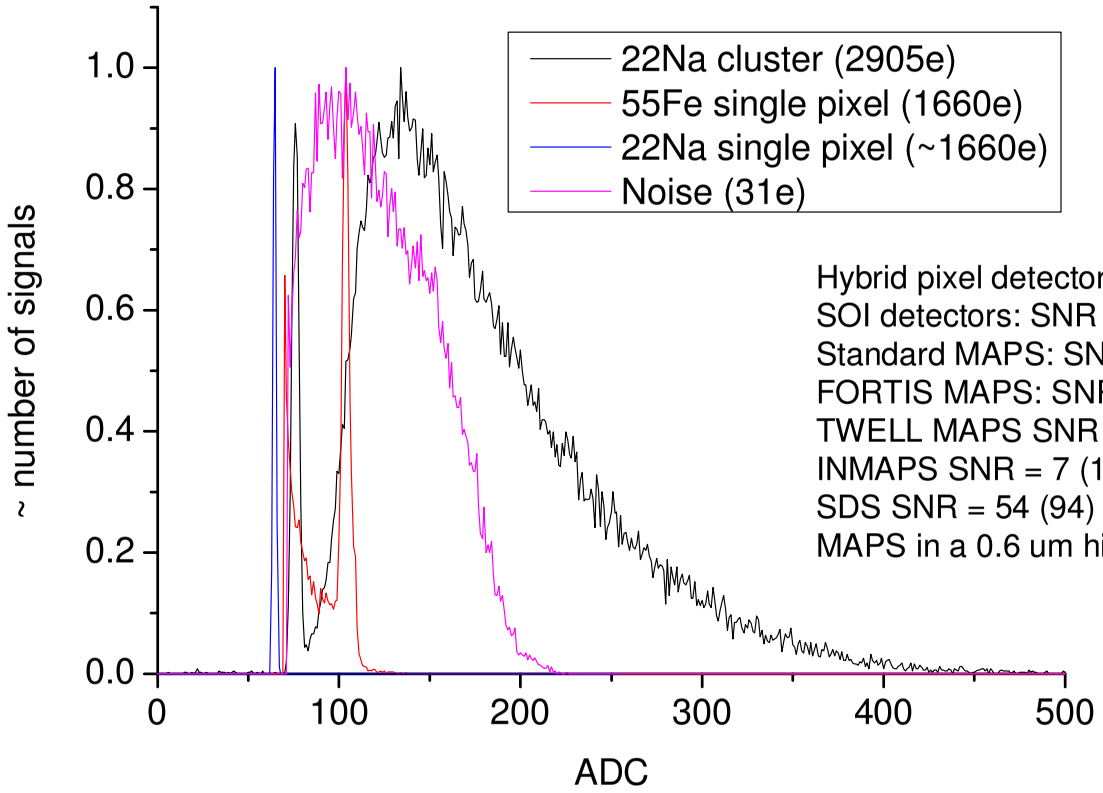
CCPD long module



32 outputs at 500MBit = 1.024us

Some experimental results

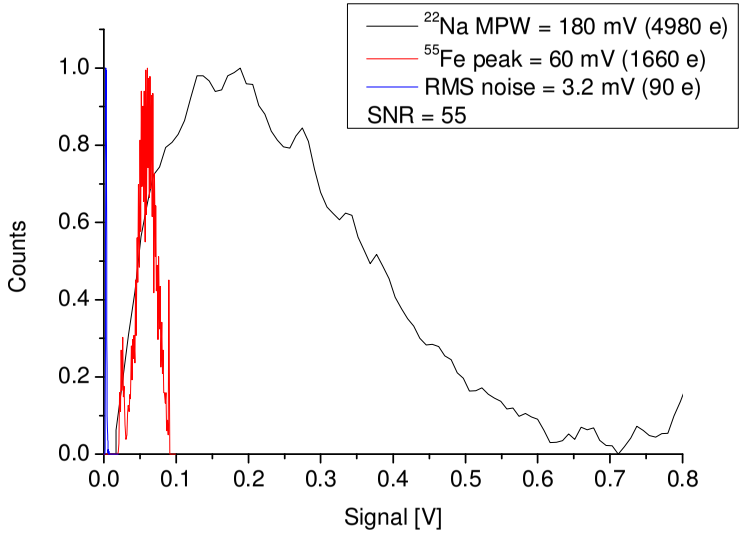
SNR single pixel (cluster) = 54 (94)

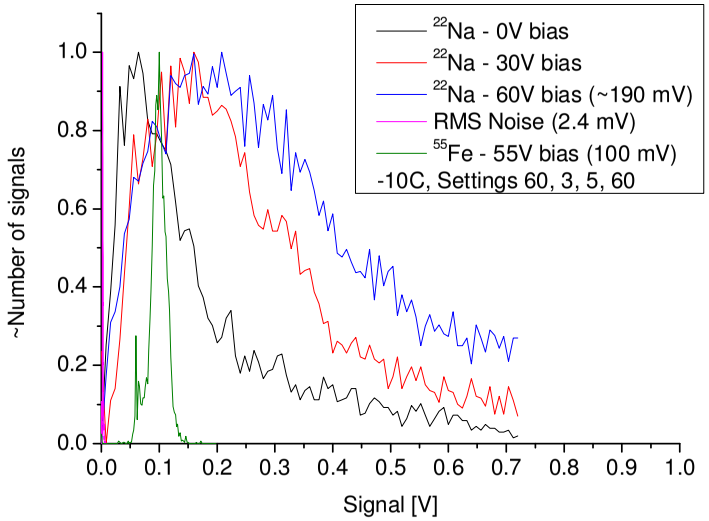


Hybrid pixel detectors: SNR = (?) 120
SOI detectors: SNR = 15 (?)
Standard MAPS: SNR = 18 (62)
FORTIS MAPS: SNR = ? (52)
TWELL MAPS SNR = 24 (?)
INMAPS SNR = 7 (16)
SDS SNR = 54 (94)
MAPS in a 0.6 um high-voltage CMOS (new) SNR = 58 (89)

The spectrum has been measured with ^{22}Na beta source at room temperature
New version of HVM chip
Most probable cluster signal: 2905e
Most probable single pixel signal ~1660 e
Noise: 31e
SNR single pixel = 54
SNR cluster signal to single pixel noise = 94

SNR = 55 (79) +10C (-10C) after irradiation with protons (10^{15} n_{eq})





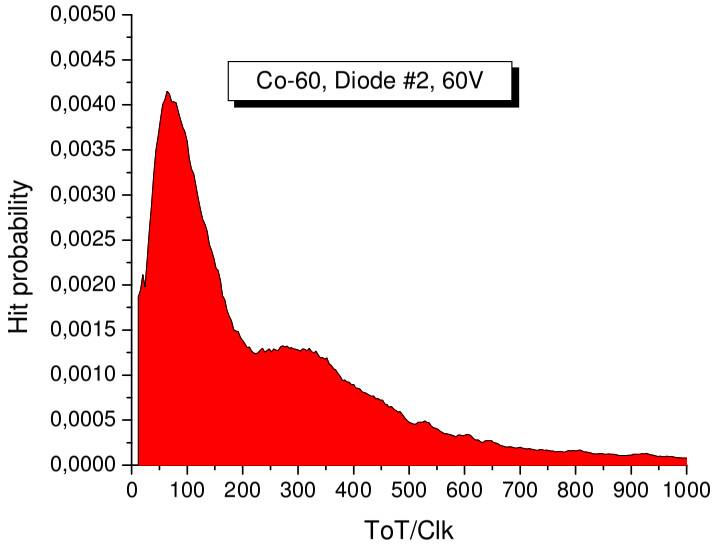
The spectrum has been measured with ^{22}Na beta source at 10C
Sensor pixel of the SDS with capacitive readout has been irradiated with protons to 10^{15} n_{eq}
SNR single pixel = 55

The spectra have been measured with ^{22}Na beta source at -10C
Sensor pixel of the SDS with capacitive readout has been irradiated with protons to 10^{15} n_{eq}
SNR single pixel = 79

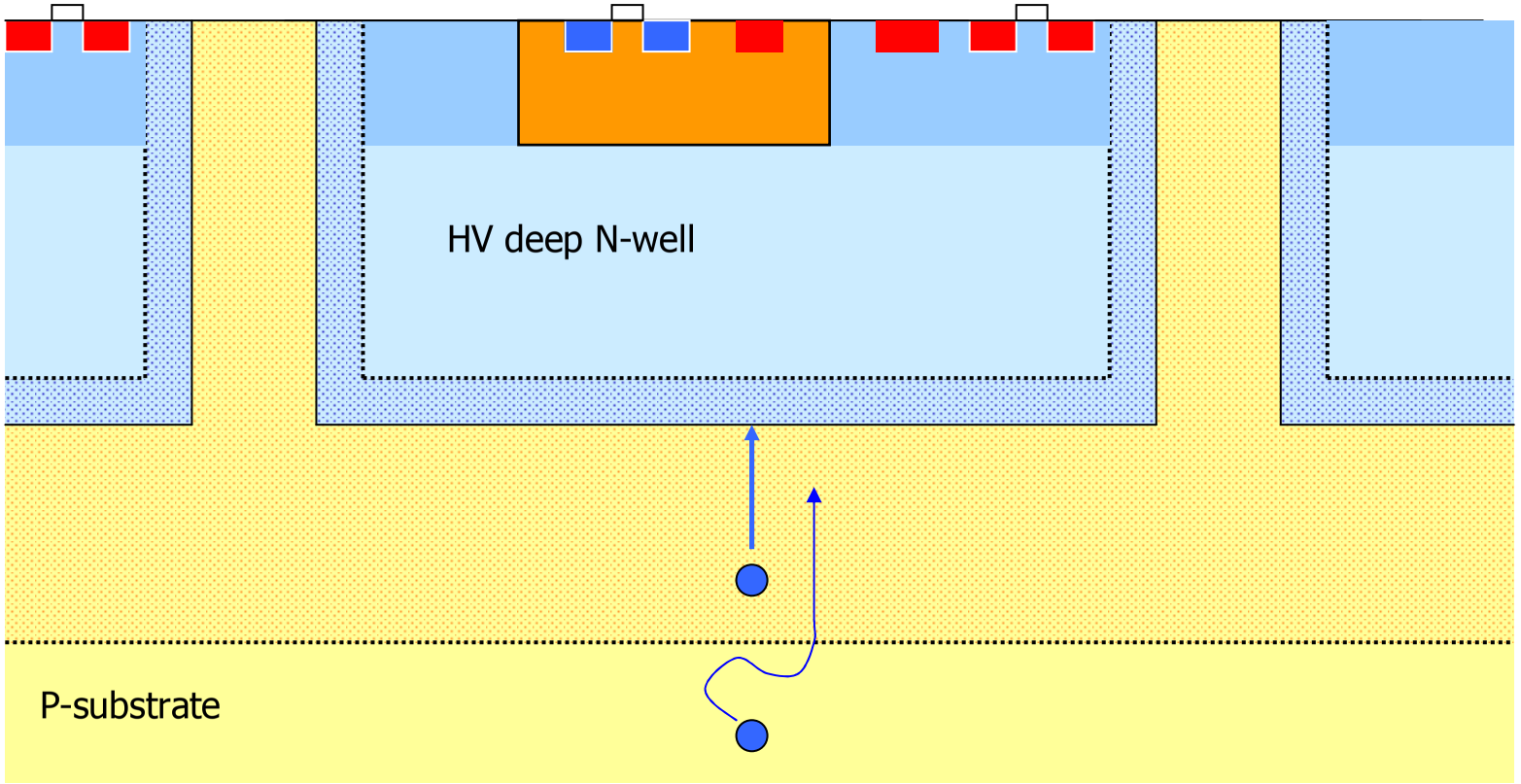
As comparison: ATLAS pixel detector SNR = 73 after irradiation

Bias voltage influence

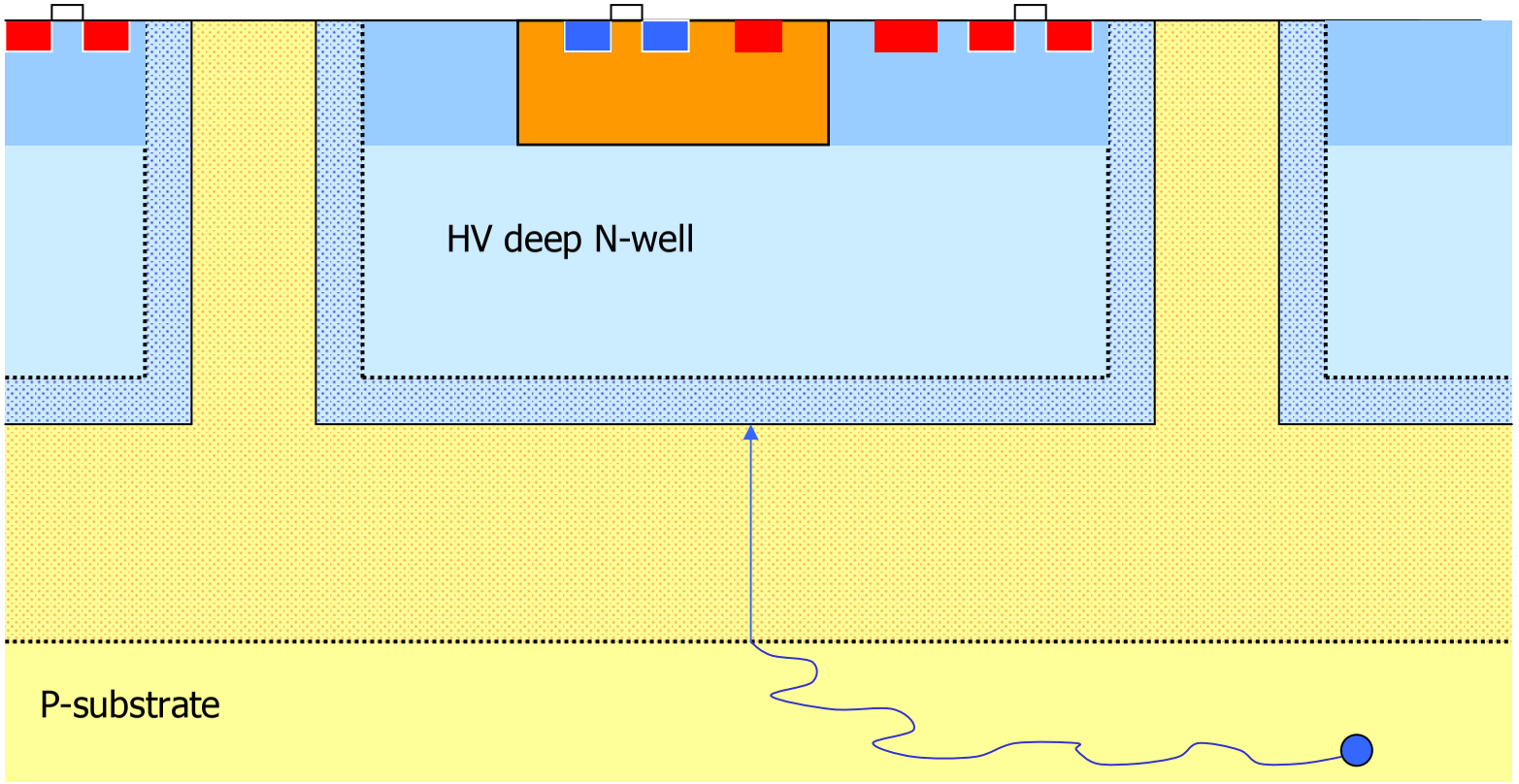
High energy peak moves to lower energies when the bias voltage decreases



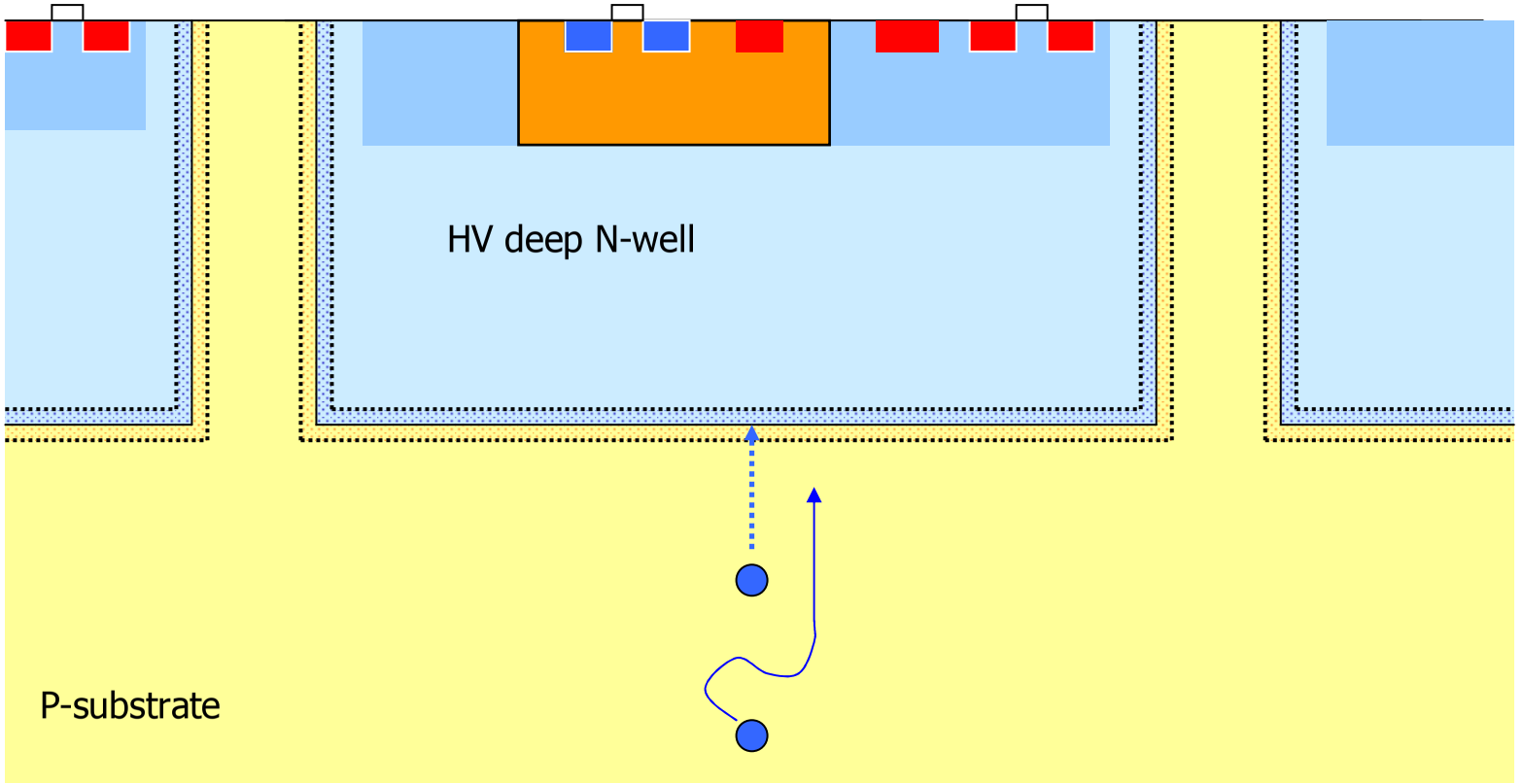
Direct signal



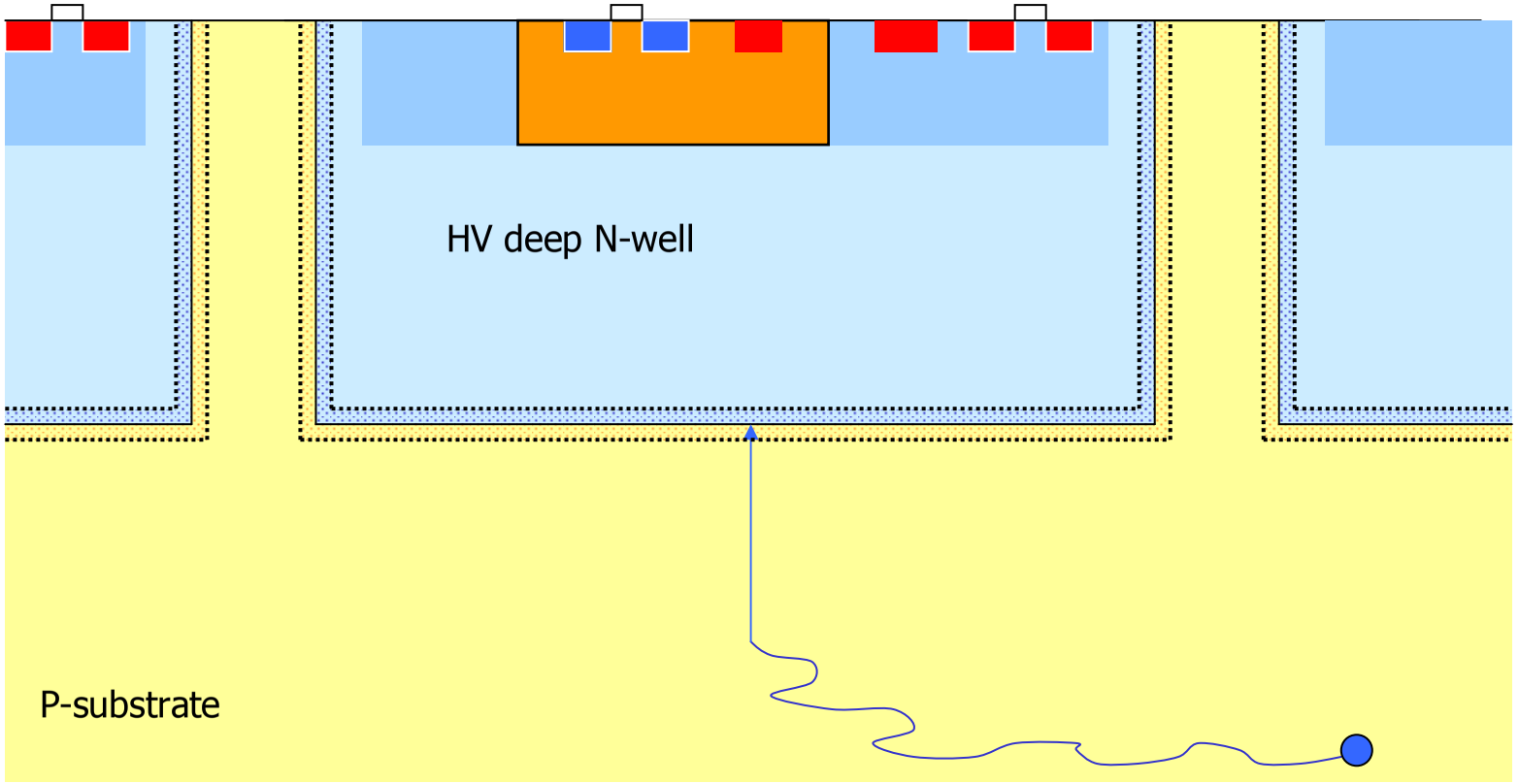
Signal from substrate



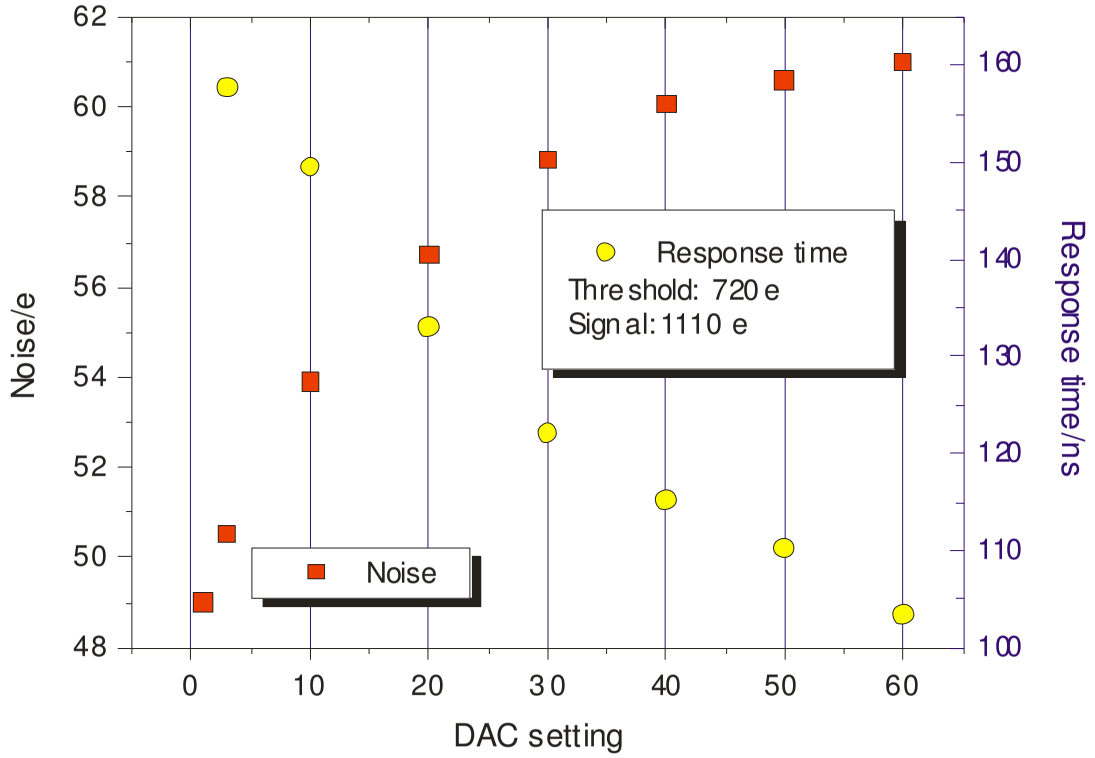
Direct signal



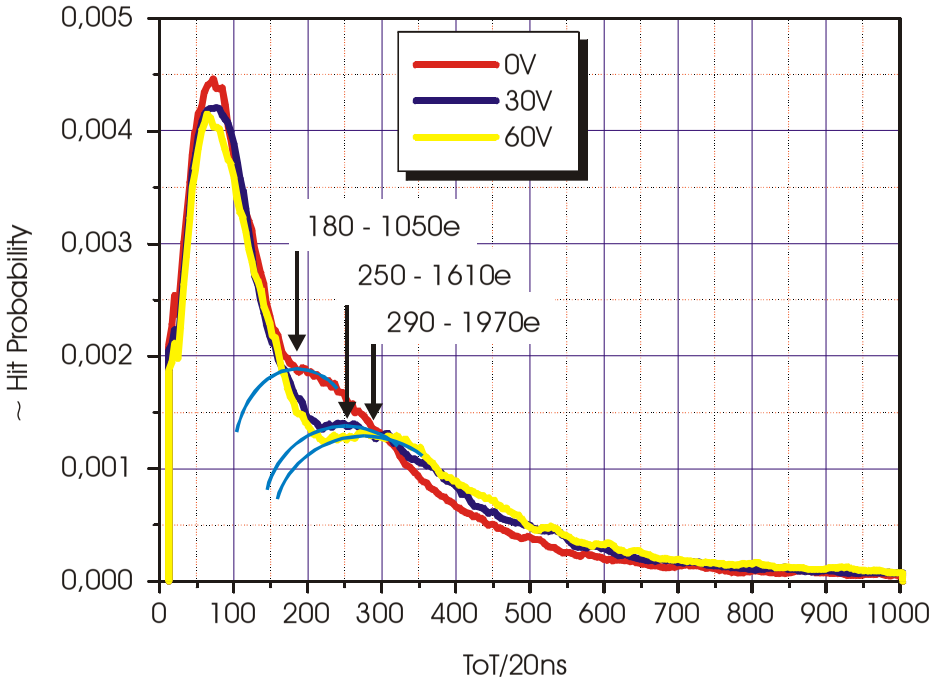
Signal from substrate



SDS with sparse readout – noise and shaping time

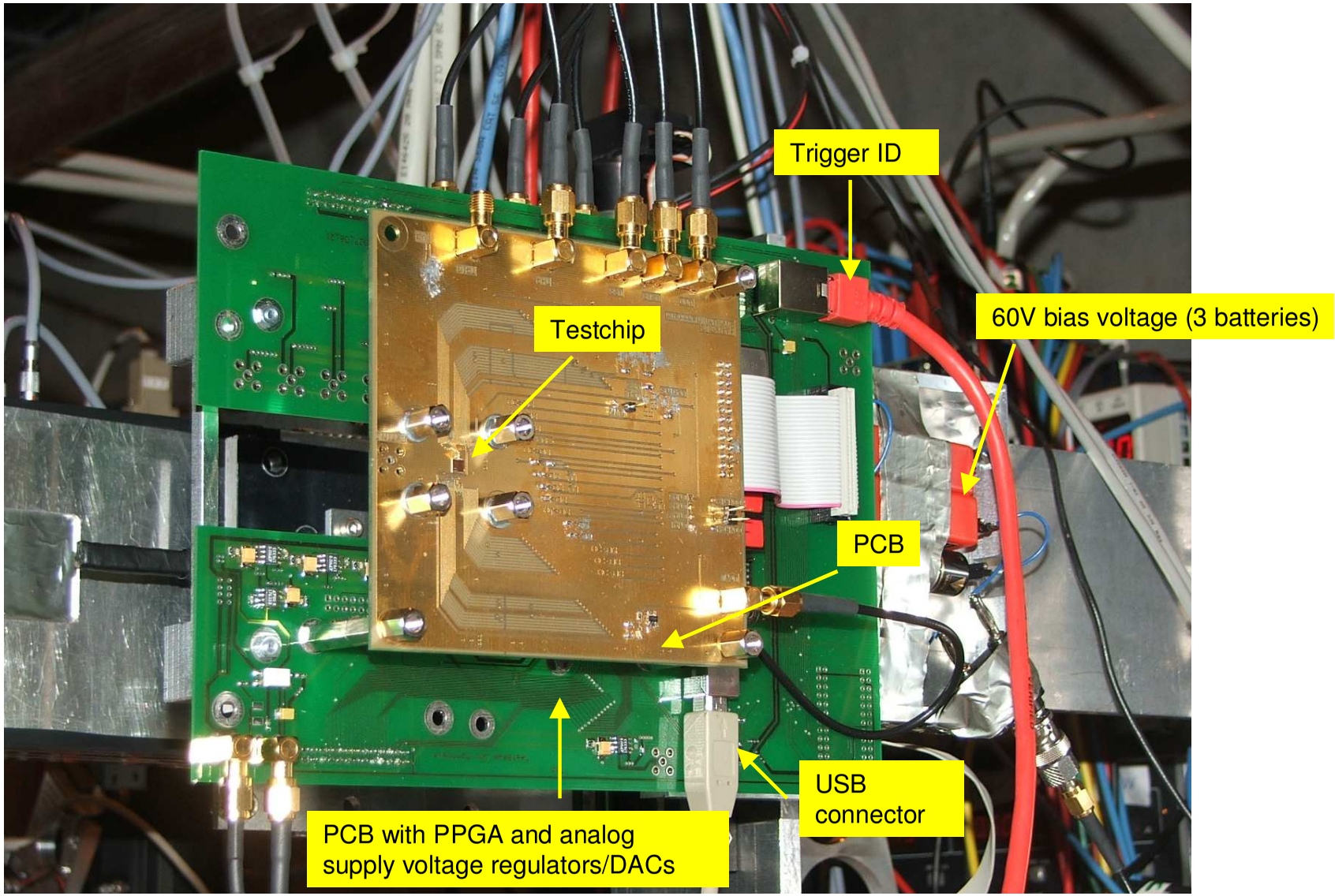


Bias voltage dependence



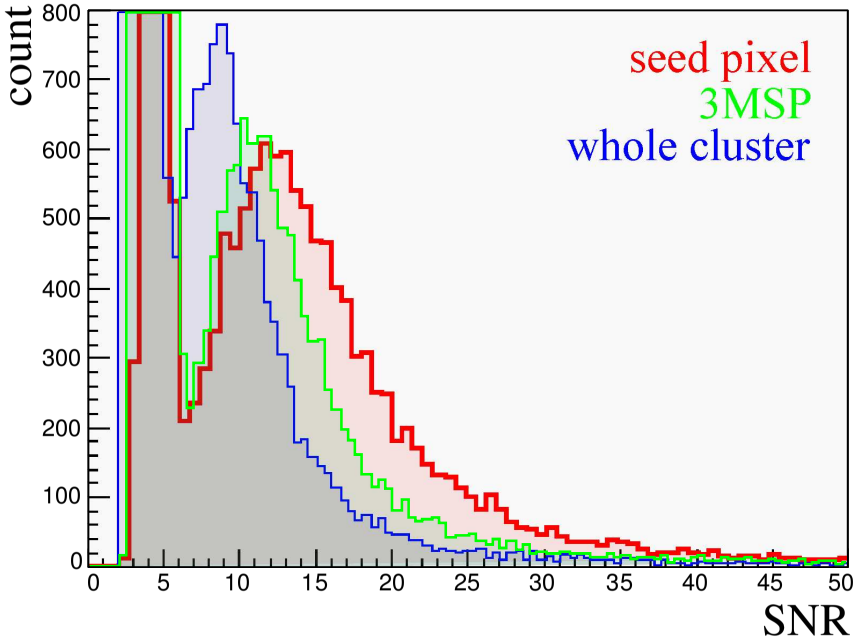
With bias: 1970 e
Without bias: 1050 e
-> Depleted zone: 920 e
-> Expected MIP from d.z. : 800 e

Test beam at CERN (SpS)

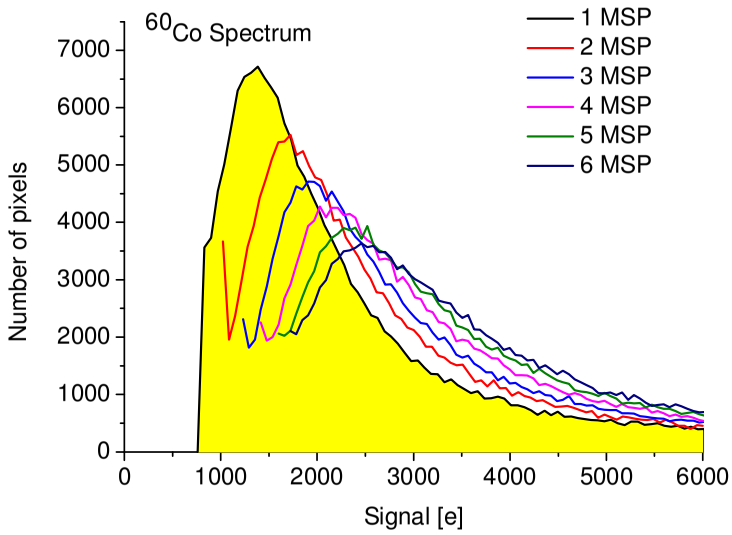


Results – MIP signal

MIP spectrum (CERN SpS - 120GeV protons)



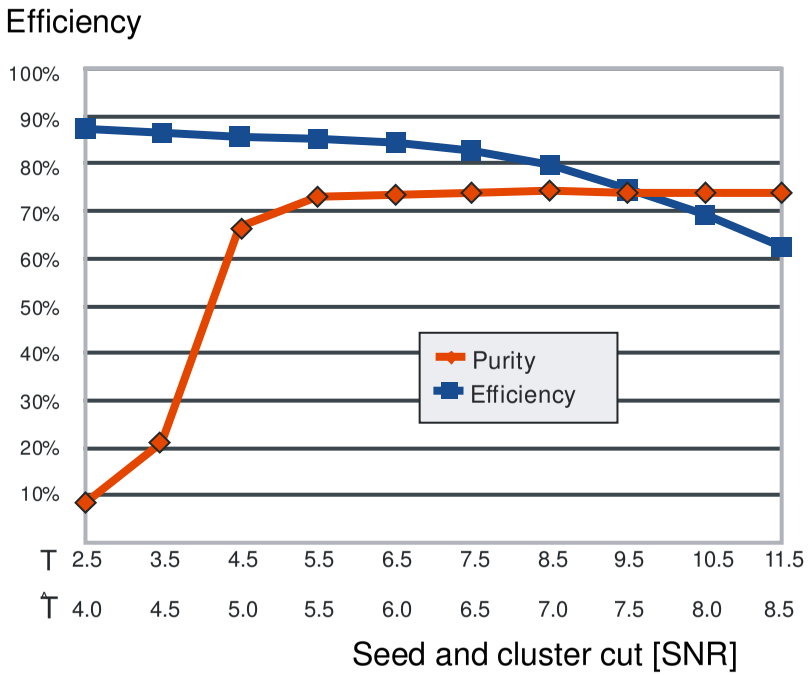
MIP spectrum (^{60} Co)

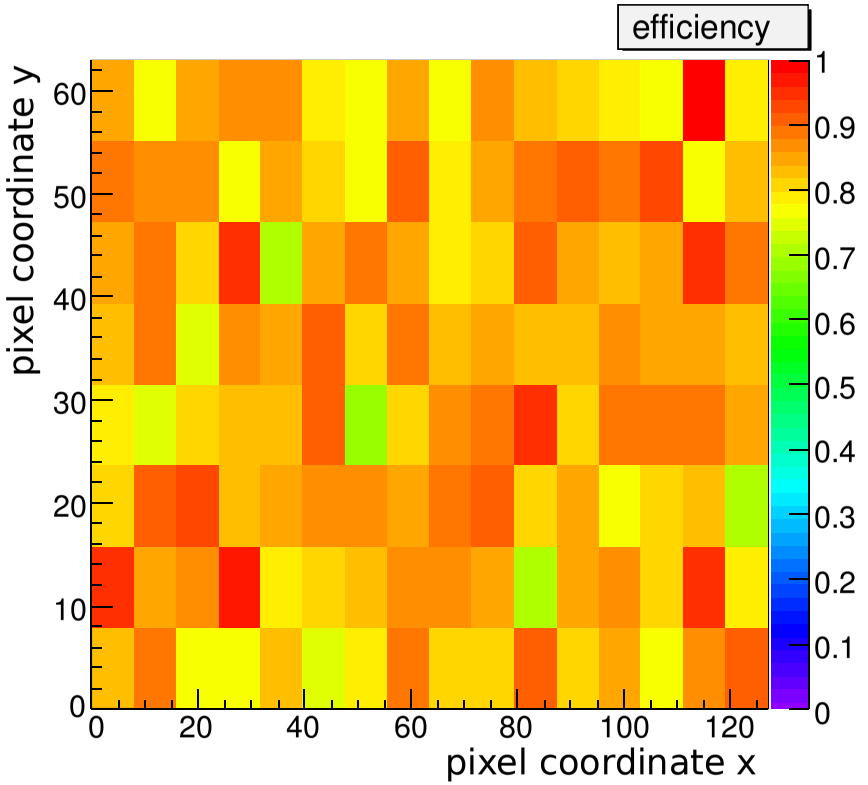


MIP spectrum (CERN SpS - 120GeV protons)
The signal is from **1200 e** (single pixel) to **2200 e** (6-pixel cluster)
The measured S/N ratio varies from 12.3 (single pixel) to 9.8 (6-pixel cluster)

Efficiency

Efficiency is homogenous over the matrix area and saturates at **86% for low seed/cluster thresholds**

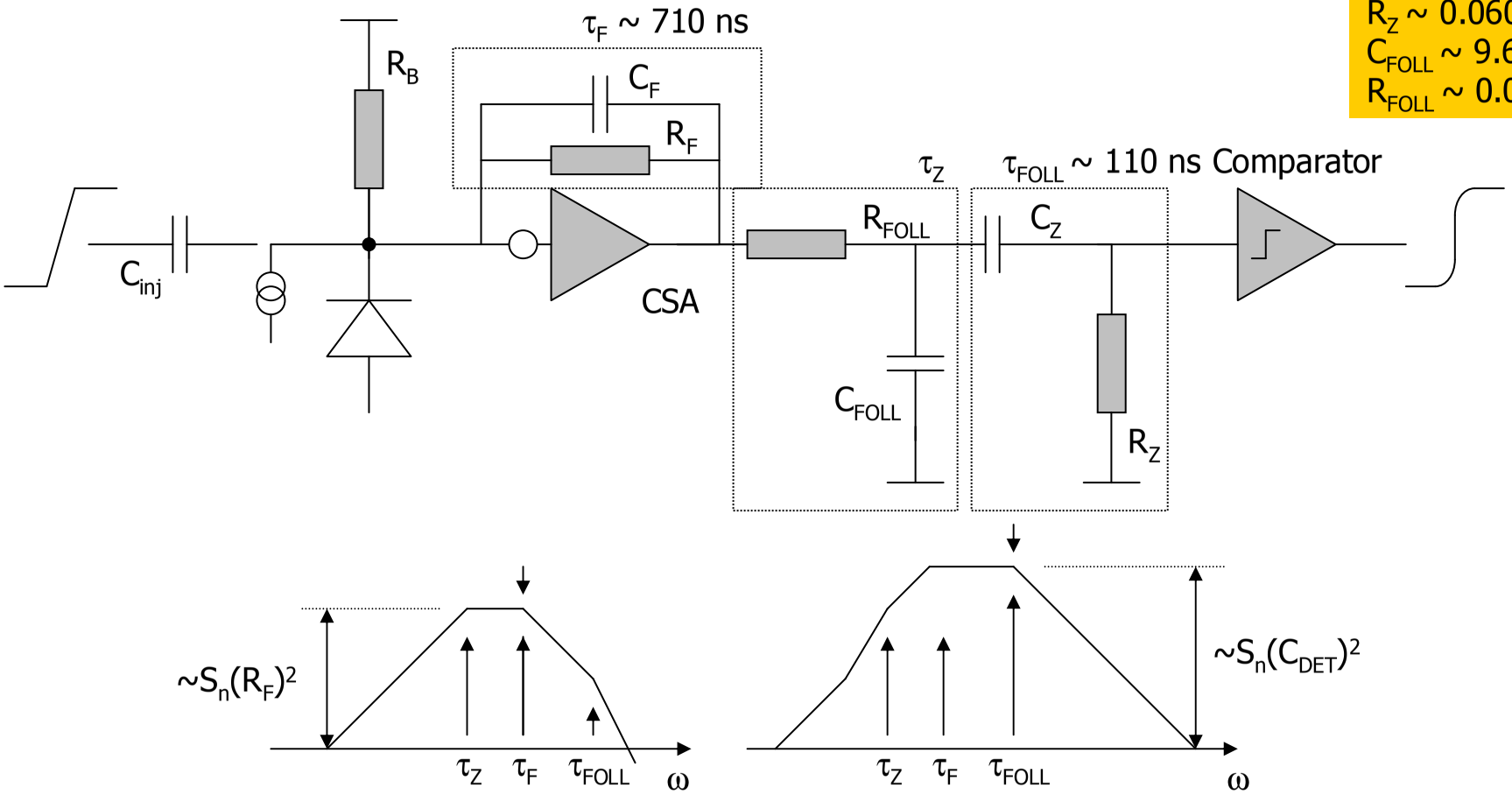




Thank you

Noise (Theory)

C_F ~ 0.9 fF
R_F ~ 0.79 GΩ
C_Z ~ 31.7 fF
R_Z ~ 0.060 GΩ
C_{FOLL} ~ 9.6 fF
R_{FOLL} ~ 0.011 GΩ



Input current noise (spectral power density)

Input transistor noise (SPD)