Radiation Damage to Electronics

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Contents

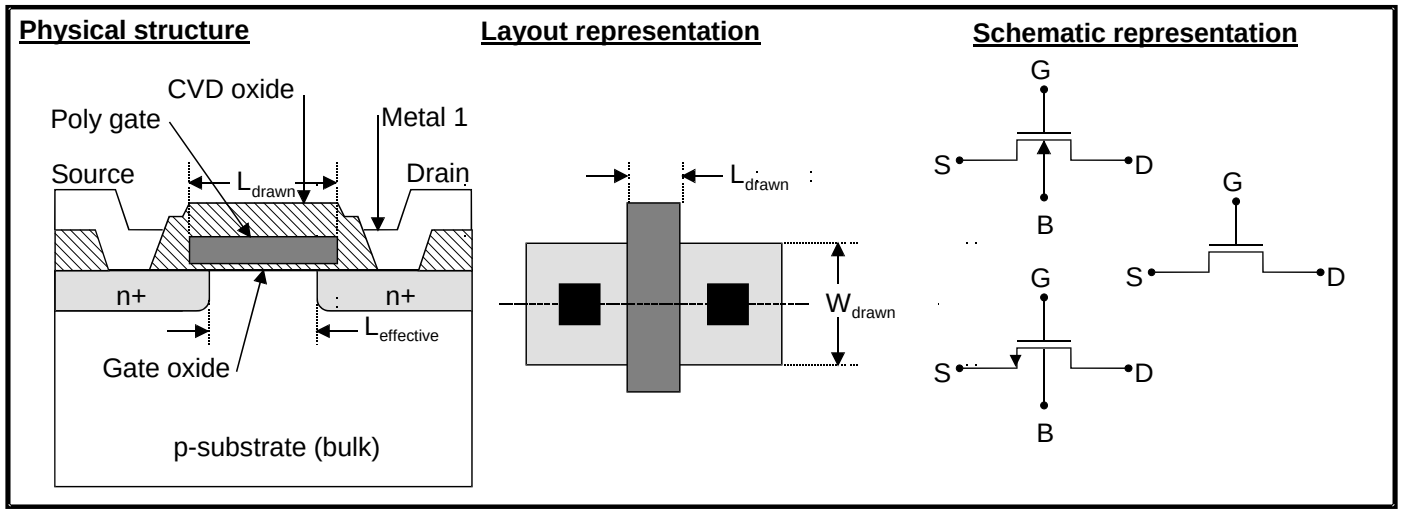
- Electronics: technology and devices
- Terminology
- Overview: types of radiation damage
  - Ionizing and non-ionizing irradiation effects
  - Long term vs. short term effects
- Radiation Hardness vs. Tolerance

- Mentioning methods to improve the electronics

Electronics: Technology

- Technologies: MOS and bipolar
- mainly CMOS: cheap and easily available
- MOS = Metal Oxide Semiconductor
- MOSFET = MOS Field Effect Transistor
- pMOS / nMOS: the two basic transistor types used in MOS technology
- CMOS = Complementary MOS (using both pMOS and nMOS)

Electronics: nMOS Transistor



NMOS physical structure:

- **p-substrate**
- **n+ source/drain**
- **gate oxide (SiO_2)**
- **polysilicon gate**
- **CVD oxide**
- **metal 1**
- **L_{eff}<L_{drawn} (lateral doping effects)**

NMOS layout representation:

Implicit layers:

- oxide layers
- substrate (bulk)

Drawn layers:

- n+ regions
- polysilicon gate
- oxide contact cuts
- metal layers

Slide: V. Lindenstruth, ME1

Electronics: Devices

- Commercial ICs
- ASICs
  - incl. special-purpose ICs like regulators
- PLDs, FPGAs
- Memories: SRAM / DRAM, Flash, EPROM

Electronics Irradiation Terminology ?

- Total Ionizing Dose
- (minimum) LET
- annealing
- SEE, SEU, SEL
- displacement damage, lattice structure
- NIEL
- gate oxide, lateral oxide, field oxide
- parasitic leakage (current)
- Si/SiO interface
- threshold voltage, transconductance

Types of Radiation Damage

- **Differentiation between Ionizing and Non-Ionizing Radiation**

- **Ionizing: damage through charge deposition**
- **Non-Ionizing: ‘physical’ damage**

- **Long-Term accumulated effects vs. single-event effects**

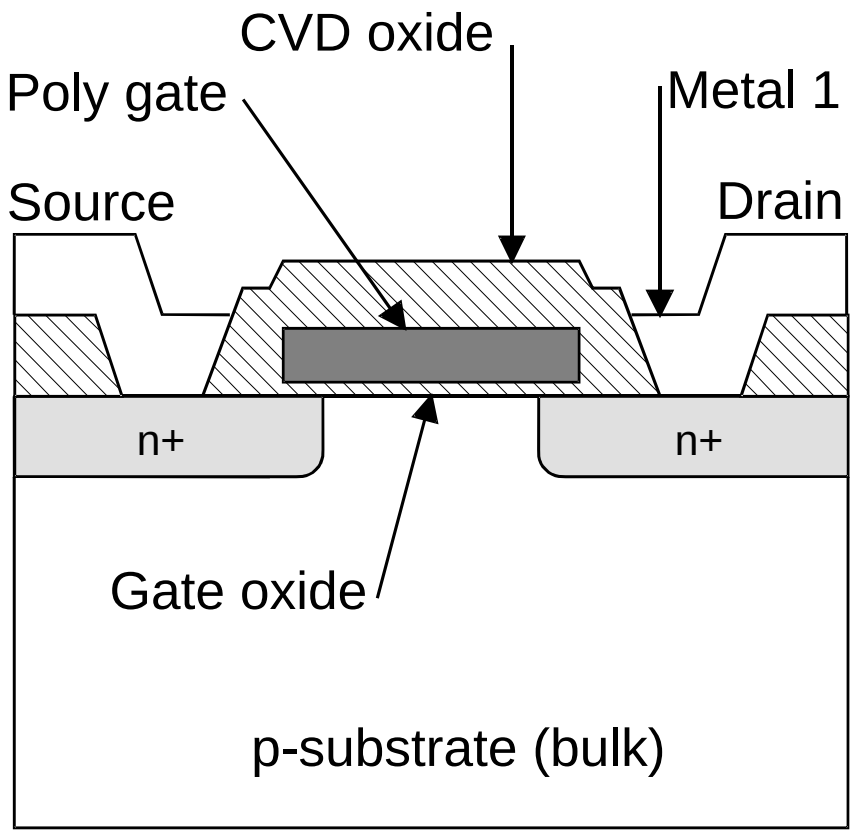
Long-Term Ionizing Radiation Damage

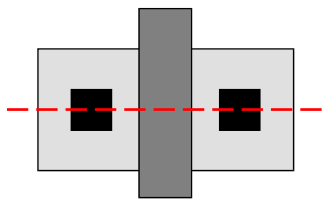
- **Ionization / Charge Deposition**
  - **directly: electrons, charged hadrons**
  - **indirectly: gammas, neutrons (energy deposition)**

- **Creation of electron-hole pairs**
- **No electrical field: recombination**
- **With electrical field: electrons quickly removed, trapping of positive charges**
- **Trapped charges change the electrical properties**

Long-Term Ionizing Radiation Damage

- **Critical areas?**

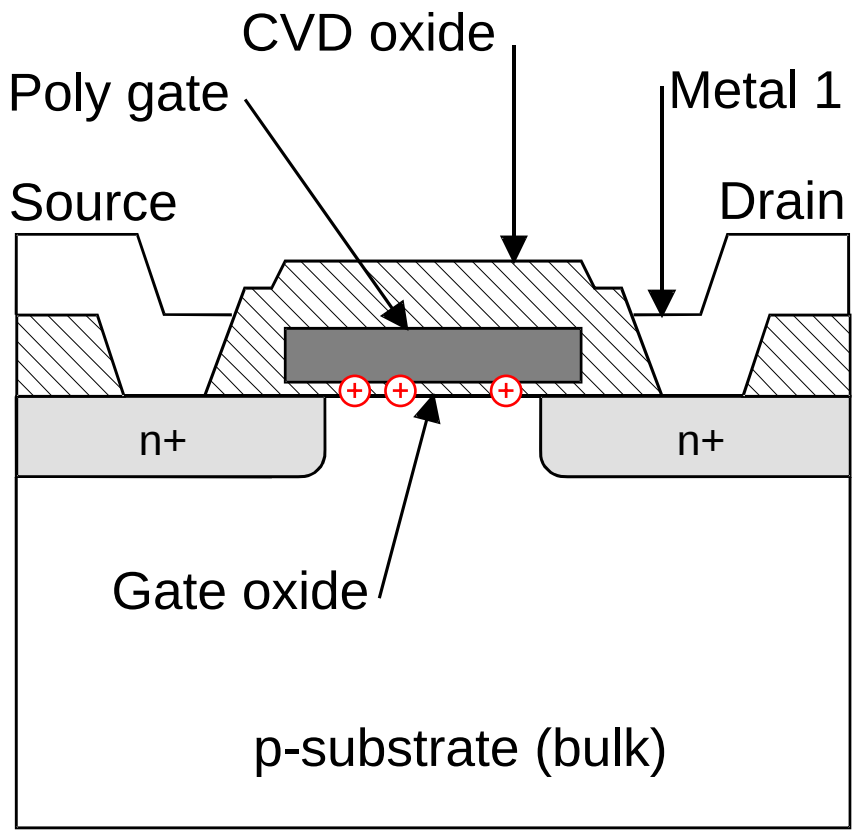


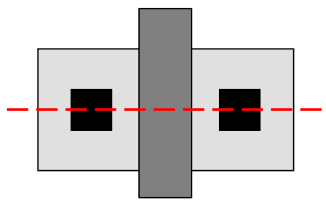


Images: V. Lindenstruth, ME1

Long-Term Ionizing Radiation Damage

- **Critical areas?**





Long-Term Ionizing Radiation Damage

- **Accumulation of trapped charges over time**
- **Gate Oxide: slow movement of holes towards negative electrode, ‘deep trapping sites’**
- **Leads to shift in the gate bias voltage (threshold voltage V_{th}), changing the switching characteristics of the transistor**

- **Expressed as a function of the *Total Ionizing Dose* (TID)**

Long-Term Ionizing Radiation Damage

- **More Critical Areas: Lateral Oxide (Field Oxide)**

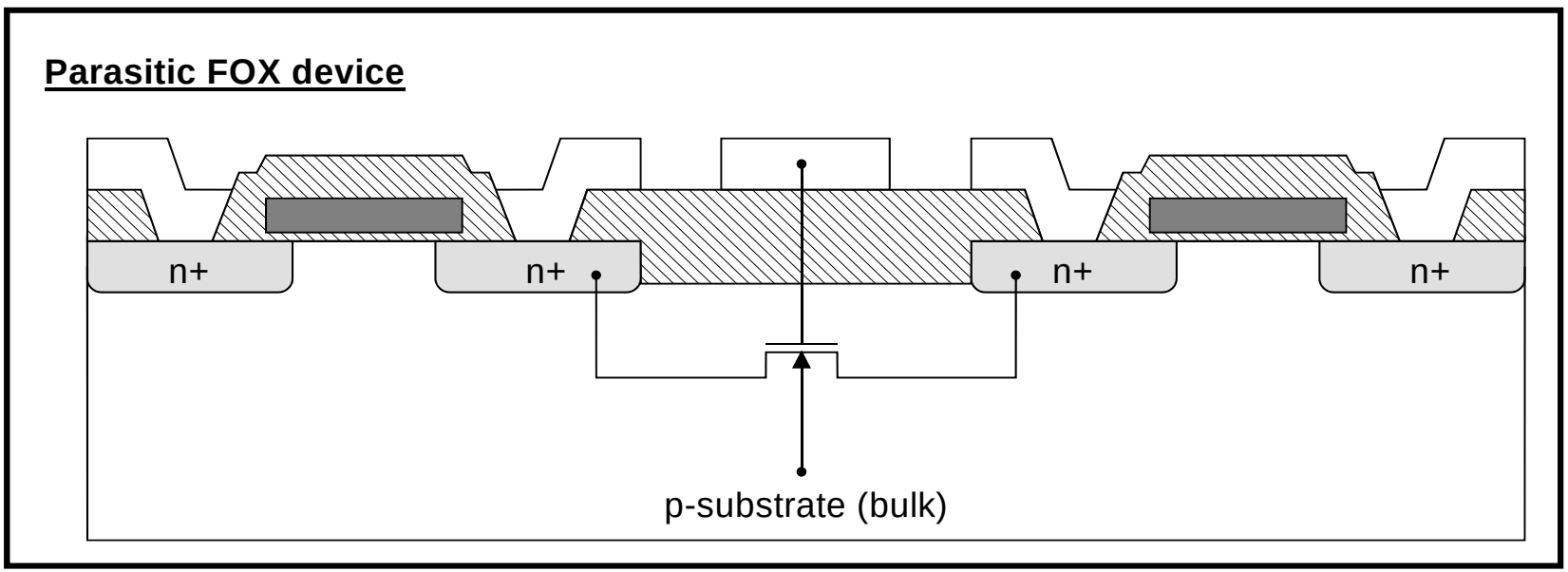


Image: V. Lindenstruth, ME1

Long-Term Ionizing Radiation Damage

- **More Critical Areas: Lateral Oxide (Field Oxide)**

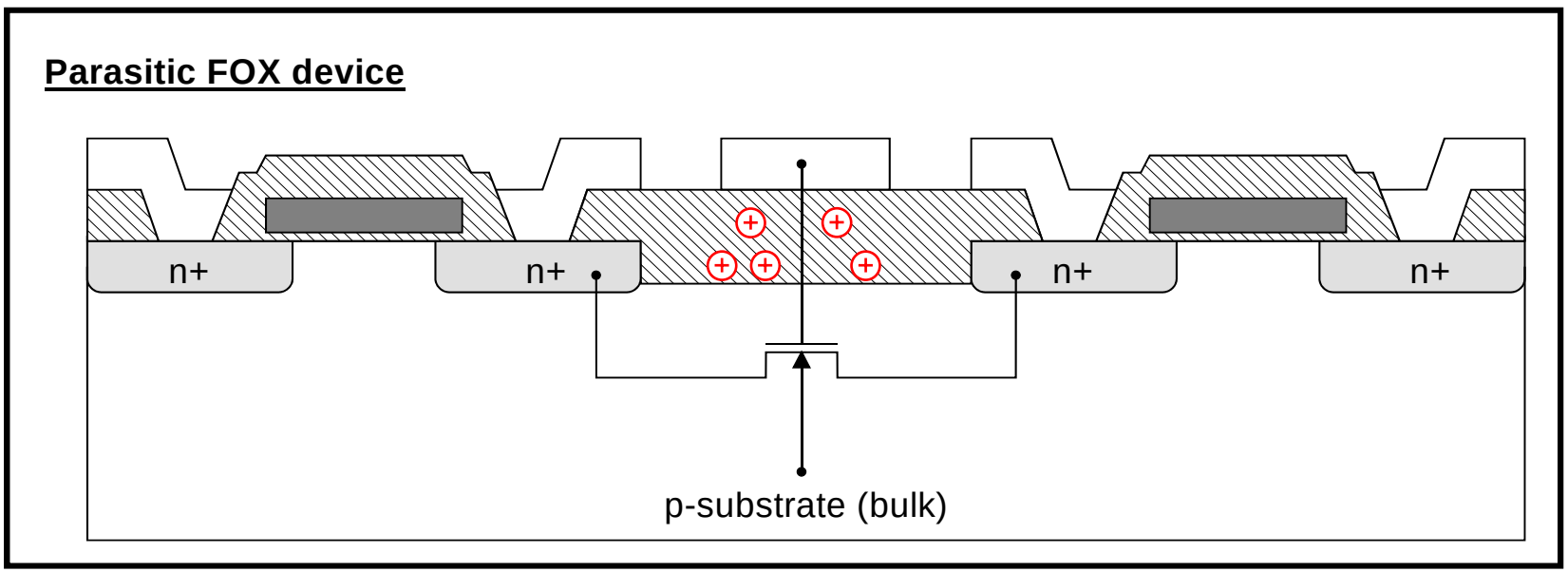


Image: V. Lindenstruth, ME1

Long-Term Ionizing Radiation Damage

- **Trapped holes in Lateral Oxide (in nMOS structures): parasitic channels**
  - **increased leakage current**
- **Annealing: trapped charges can be removed from the oxides by elevated temperatures**
- **Changes in geometry / processing can reduce the effects of defects in Lateral Oxide**

Interfaces States

- **Defects in crystal lattice at the Si/SiO_2 interface**
  - **Trap charges from the channel**
  - **Another cause for shift in threshold voltage**
  - **Reduce carrier mobility in channel**
- **Cannot be removed easily**

Non-Ionizing Radiation Effects

- **Ionizing effects require minimum energy transfer of ~3.6 eV**
  - **Minimum energy for the generation of an electron-hole pair in silicon**
- **Particles which transfer more energy can cause structural damage in silicon by removing atoms from the lattice structure, starting at ~20 eV (displacement damage)**

Single Event Effects

- **Ionizing particle crossing the transistor area**

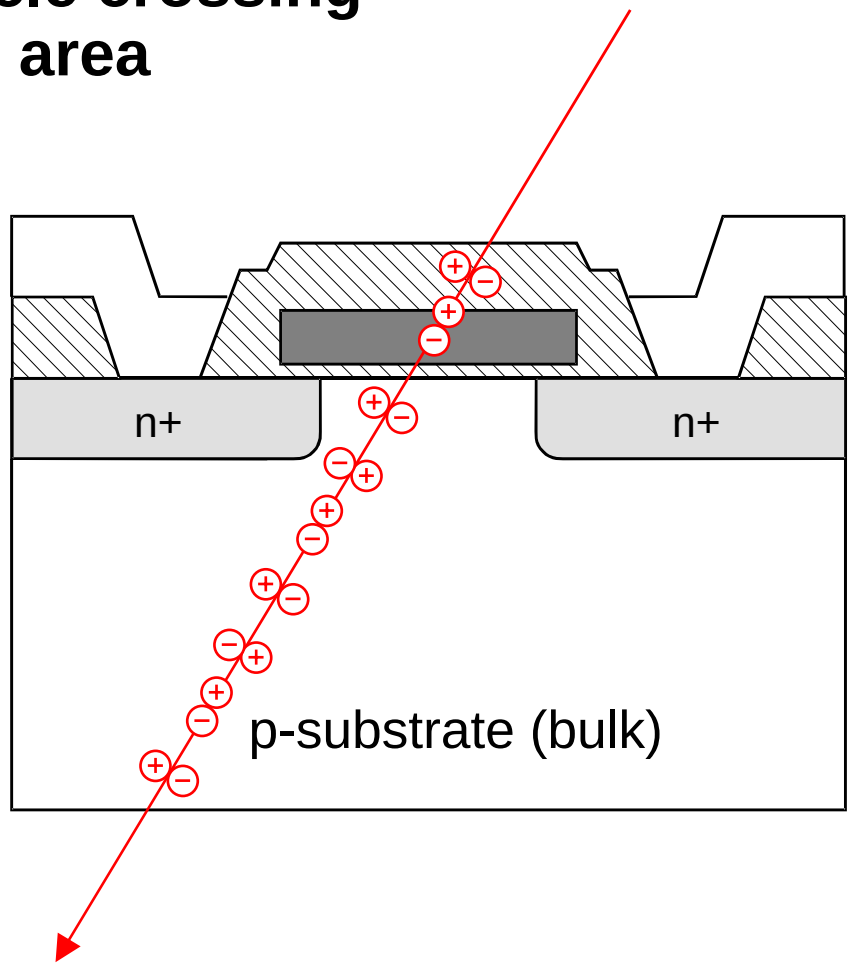


Image: V. Lindenstruth, ME1

Single Event Effects

- **Effects directly caused by individual particles crossing sensitive areas of the device**
  - **Transient: asynchronous signals, can become static**
  - **Static: changes in content of memory cells**
  - **Permanent: destructive events**

Single Event Effects

- **Timeline**
  - **Ionizing particle crosses the device**
  - **Looses energy by ionization (creating electron-hole pairs)**
  - **in bulk material: recombination, no effect**
  - **in active regions: separation → current spike**
    - » **fast component (ps) : sources within depleted region**
    - » **slow component (ns): from slightly outside active region**
  - **Many pairs → combine for total effect**

Single Event Effects

- **Linear Energy Transfer (LET): measure for the total energy deposited in the transistor**
- **Critical LET: minimum energy required to change the state of the device (for example flip-flop)**
- **Heavy ions can transfer enough energy**
- **Lighter particles (p^+, α, etc.) can initiate nuclear reactions with heavy recoil products**

Single Event Effects by Severity

- **Highest: Single Event Burnout, Gate Rupture etc.**
  - **Very high energy required**
  - **Observed in power applications**

- **High: Single Event Latch-up (SEL, or Latch-up)**
  - **Caused by positive feedback loops in parasitic structures (i.e. parasitic bipolar structures in CMOS)**
  - **Parasitic currents, leading to (almost) short circuit between power and ground → destructive**
  - **Can be prevented (different MOS technology, sometimes by careful current limitation)**

Single Event Effects by Severity

- **Medium: Single Event Upset (SEU) in flip-flops etc.**
  - **Contents of memories affected, can be overwritten**
  - **Usually tolerable**
  - **Subject to application of Error Correcting Codes (ECC), redundancy (TMR), self correcting algorithms etc.**
- **Low: asynchronous transients on signals**
  - **In digital parts: only 'visible' if latched**
  - **In analog parts: effect varies**
  - **Subject to application of redundancy etc. as above**

Single Event Upsets (SEUs)

- **SEUs in full custom ASICs: application of error correcting methods is easy during design**
- **SEUs in COTS ICs: usually only fixable by external redundancy or ECC**
- **SEUs in SRAM FPGAs: same as COTS ICs; on-chip ECC or redundancy provides only limited improvement**

Radiation Hardness vs. Tolerance

- **Radiation Hardness:**
  - **Resistance to radiation effects; for example via**
    - » **Shielding [the bulky things]**
    - » **Specially adapted design methods and technology**

- **Radiation Tolerance:**
  - **Ability to tolerate radiation effects; usually achieved by employing Error Correcting Codes or redundancy**

The End

Thanks for your attention.