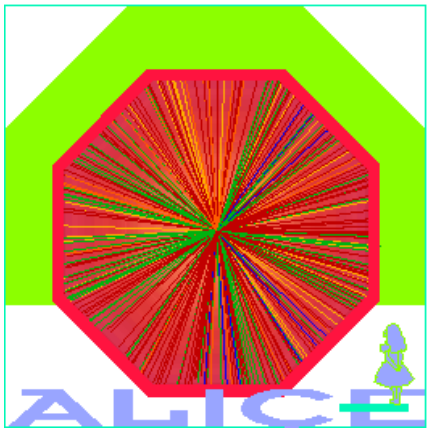


The ALICE High-Level-Trigger

Overview

The ALICE High-Level-Trigger:

- dataflow in the ALICE experiment
- trigger systems : L0, L1, L2
- TPC – largest datasource
- High-Level-Trigger: Tasks & Implementation

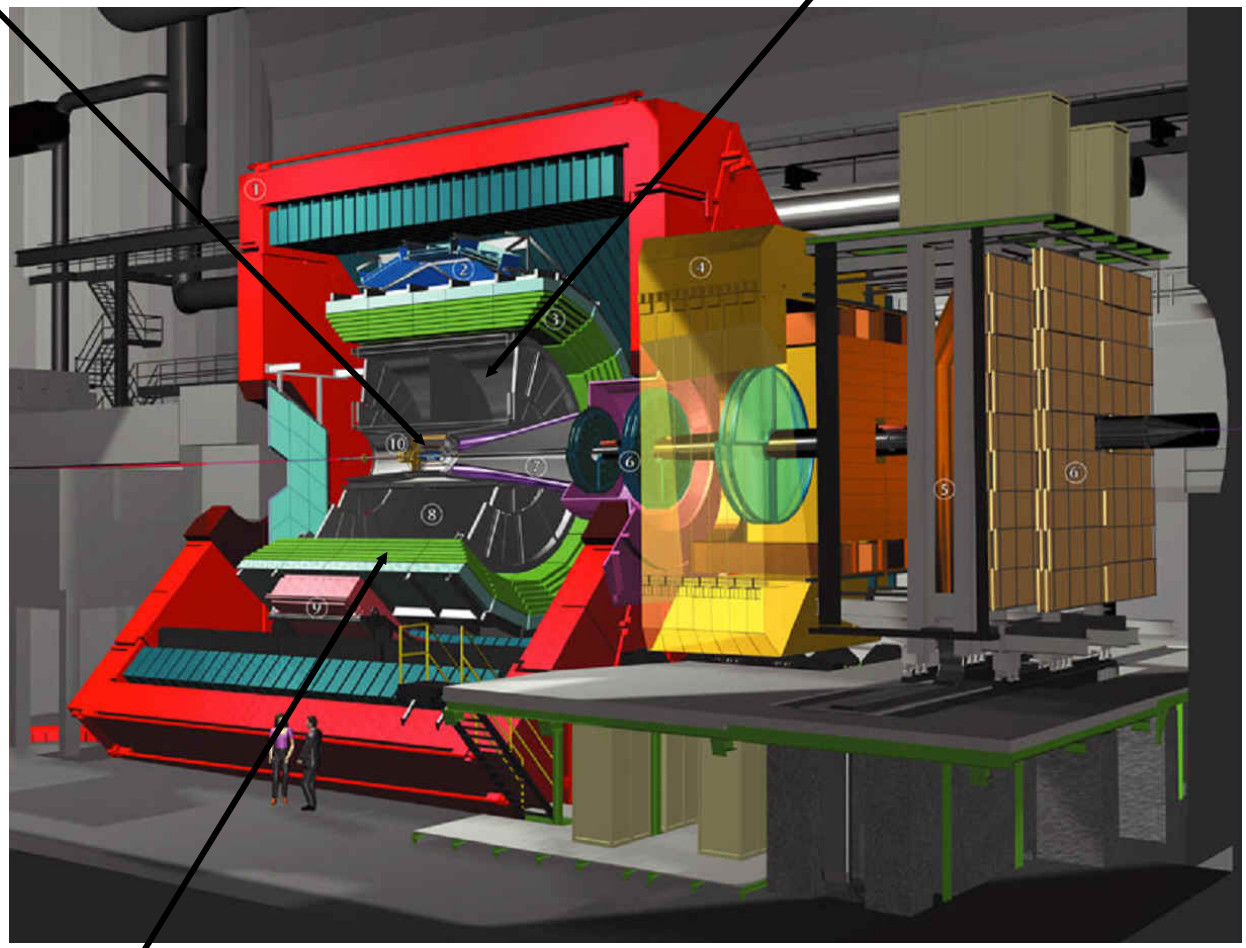
The HLT ReadOut-Receiver-Card (H-RORC):

- Tasks & Requirements
- Implementation

The ALICE detector

ITS : Inner Tracking System

TPC : Time Projection Chamber



TRD : Transition Radiation Detector

Trigger

- L0 - 1.2µs : event occured
- L1 – 6.5µs : start sampling in the Front-End-Electronics
- L2 – 88µs : readout data from the Front-End-Electronics data buffer

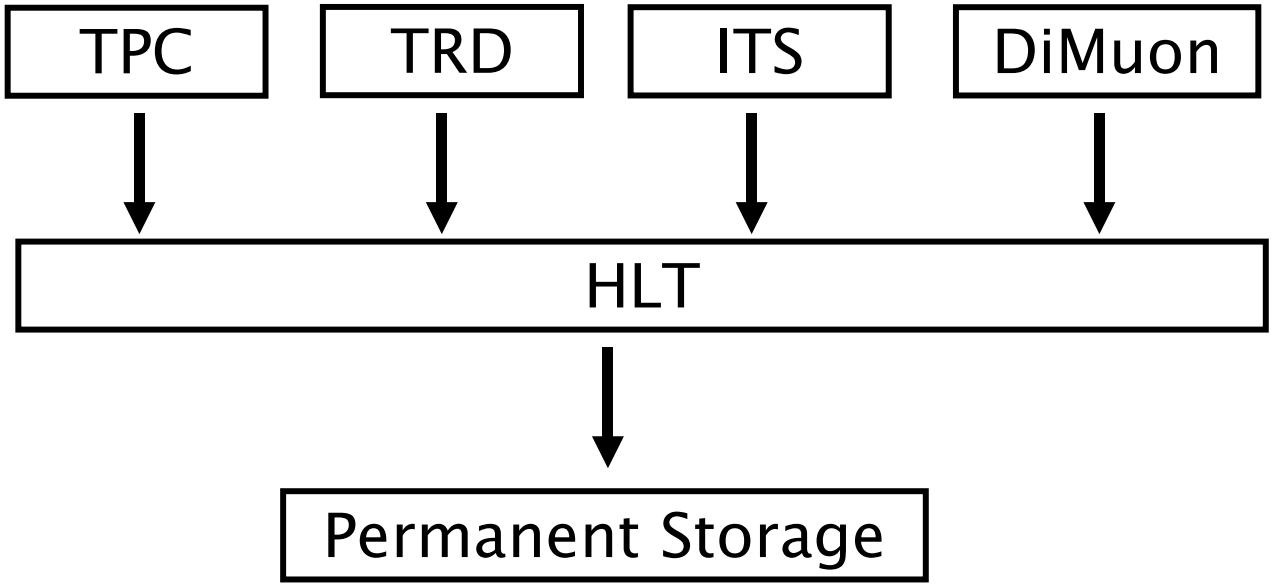
L0, L1, L2 look for „valid“ events and trigger the readout!

High-Level-Trigger : HLT

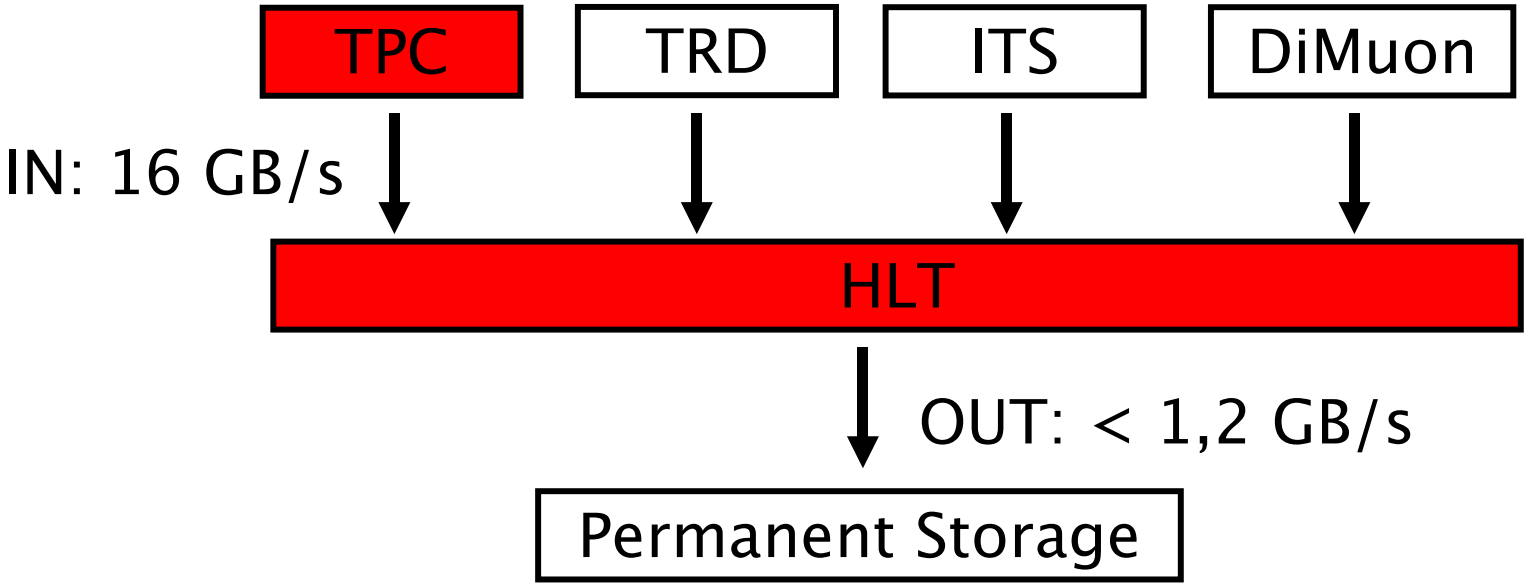
Needs for a High-Level-Trigger:

- the sub-detectors produce more data than a permanent tape storage system can handle
- Online analysis allows to trigger for rare events i.e. jets
- Events can be „tagged“ to prepare them for later offline analysis

HLT - Dataflow



HLT - Dataflow

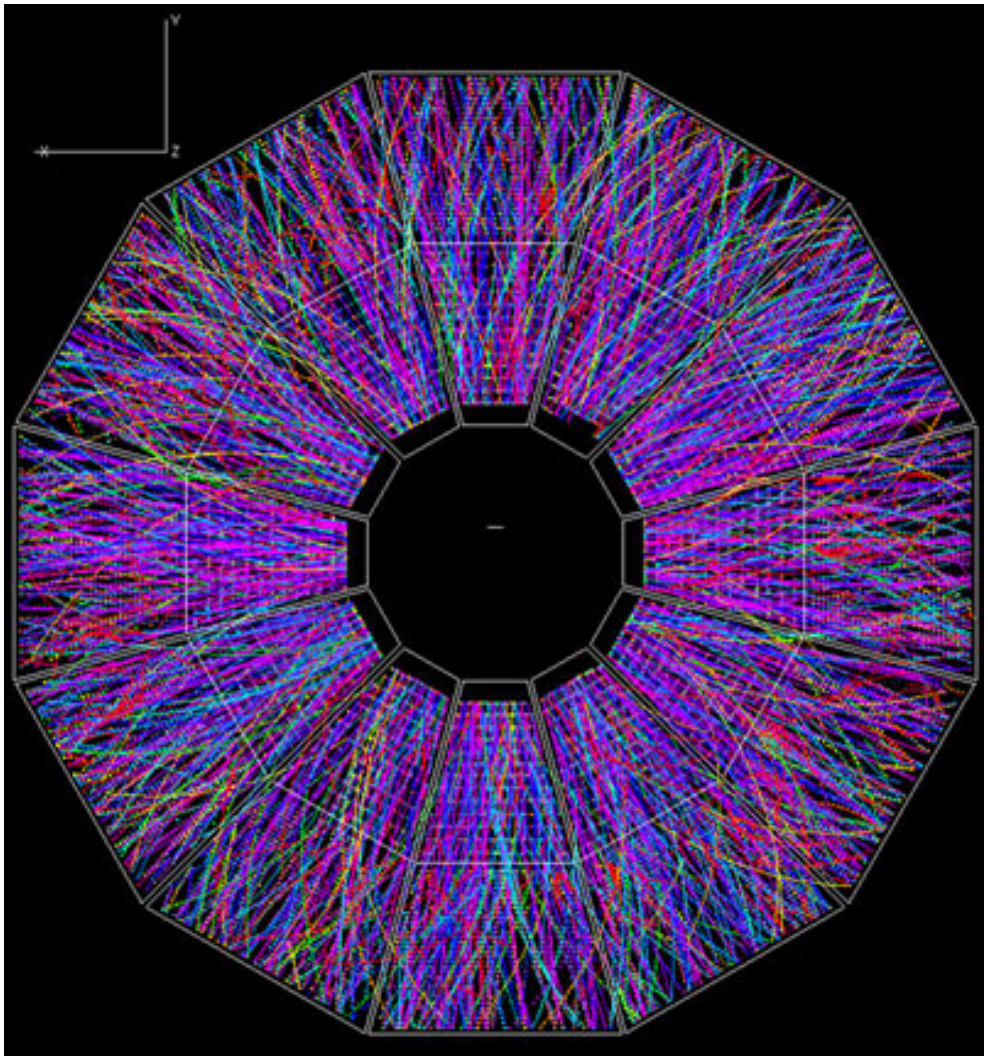


Picture of the ALICE TPC

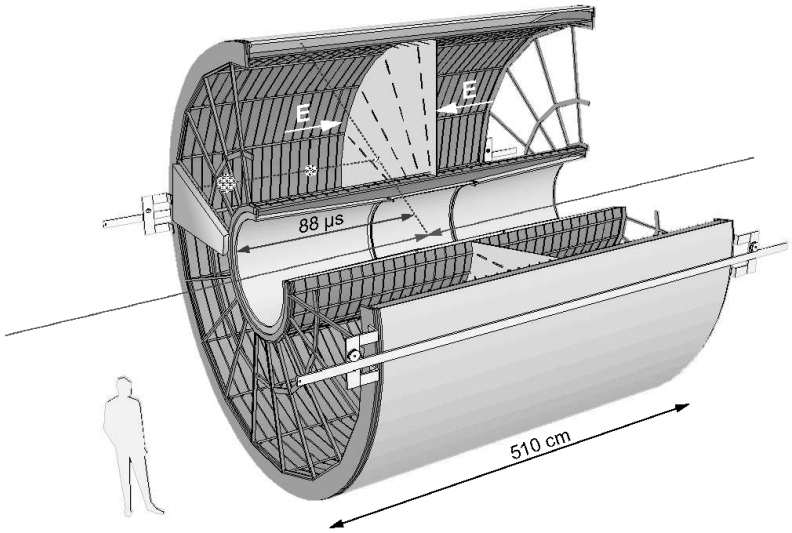
Sector

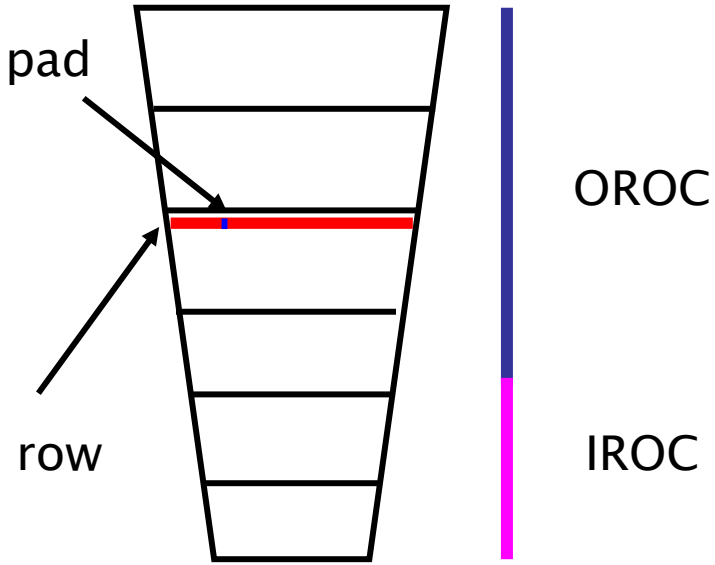
P.Glaessel – will be replaced by ITS later

Event in the STAR TPC



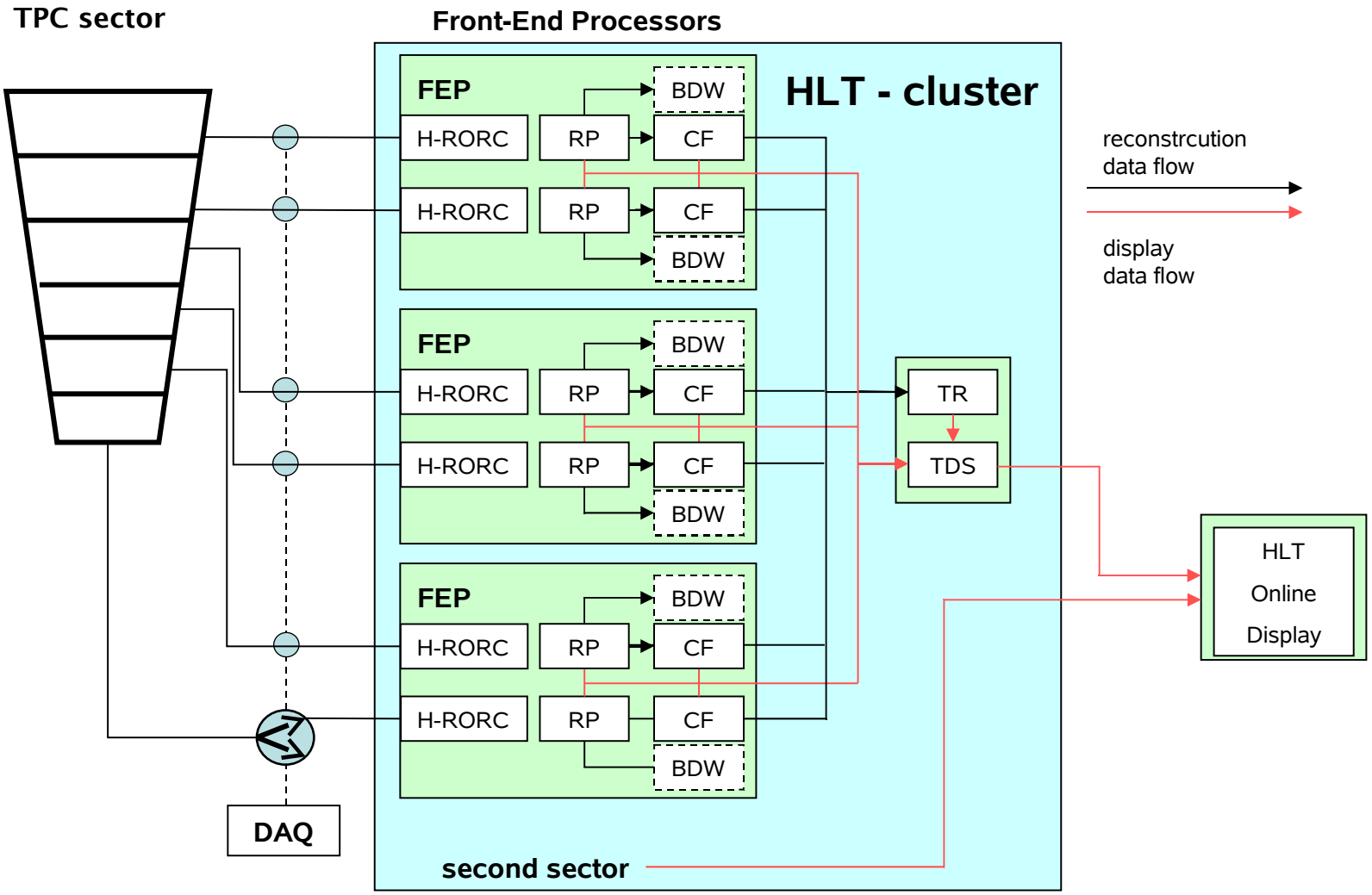
TPC Read-Out Electronics





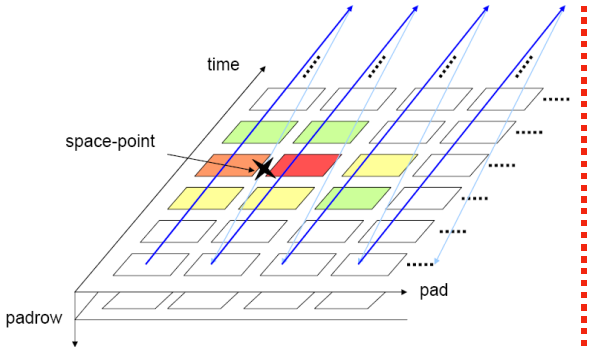
- 2 x 18 sectors (Side A & C)
- 6 readout partitions (patch) per sector : 216 patches
- ~ 26 rows per patch
- ~ 90 pads per row
- = 557,568 pads

HLT Infrastructure for one TPC sector



Tracking in the HLT

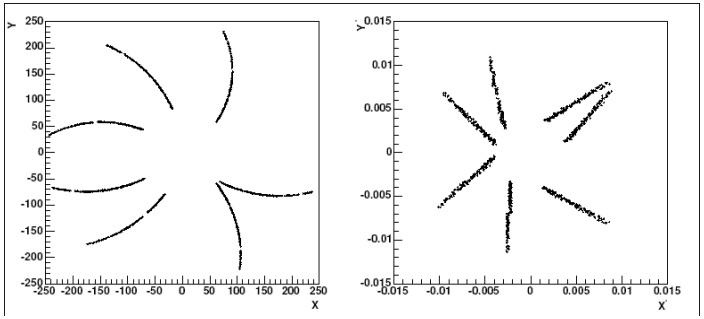
Raw Data(Ordering, Zero Suppression)



Cluster Finding (in readout partition)

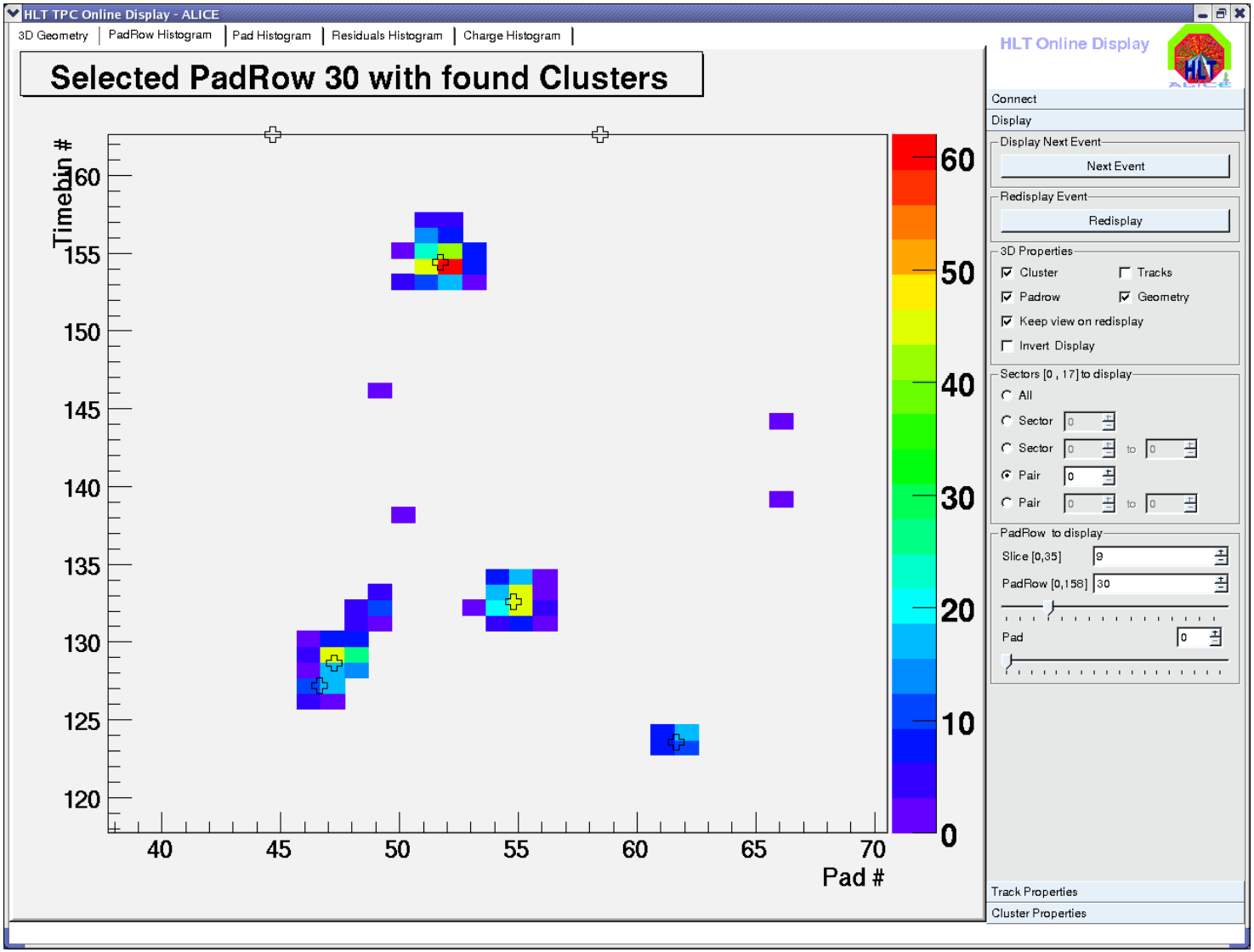
Can be done in the FPGA

– Data amount
+ Computing amount

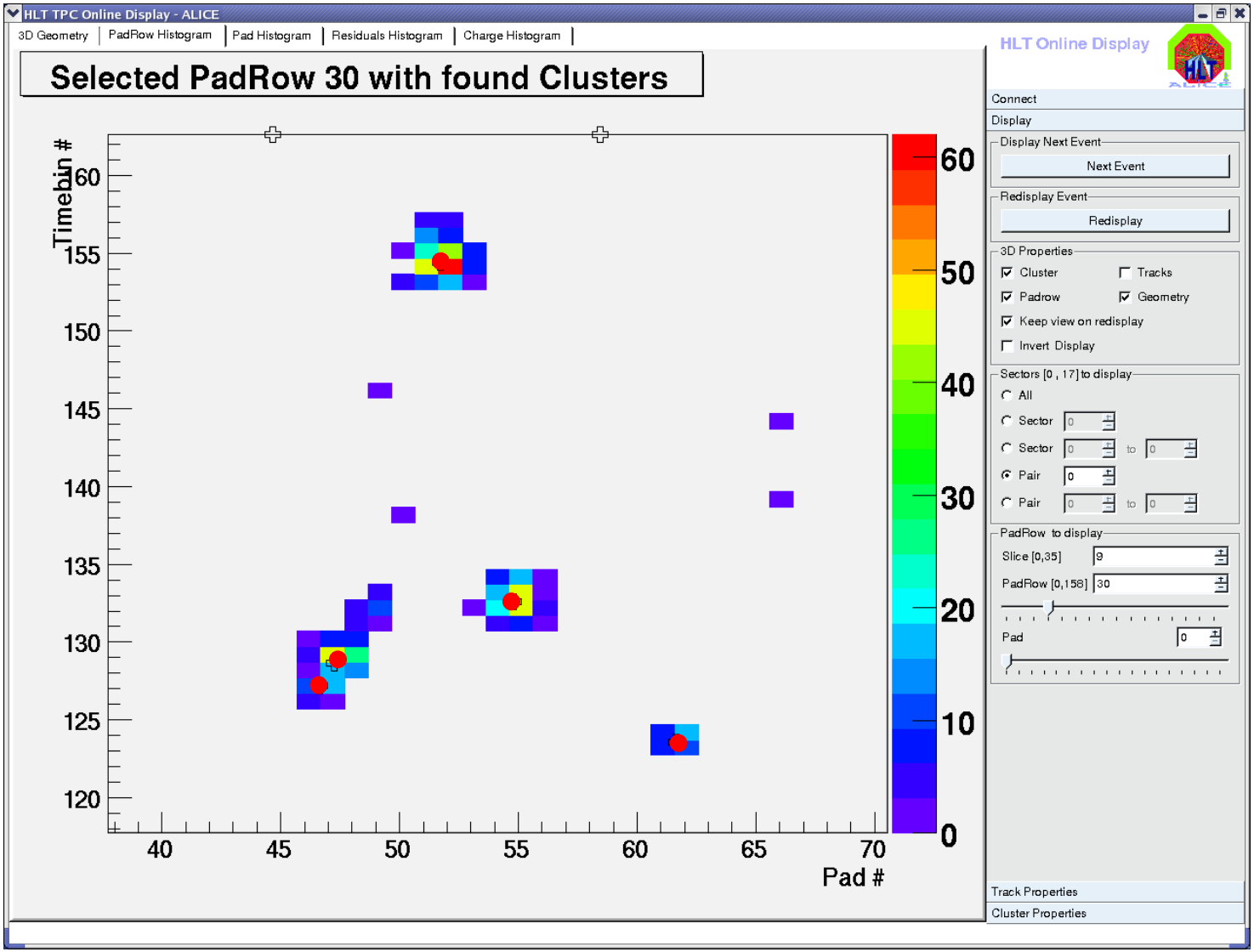


Tracking
(Conformal-Mapping / Track Follower)

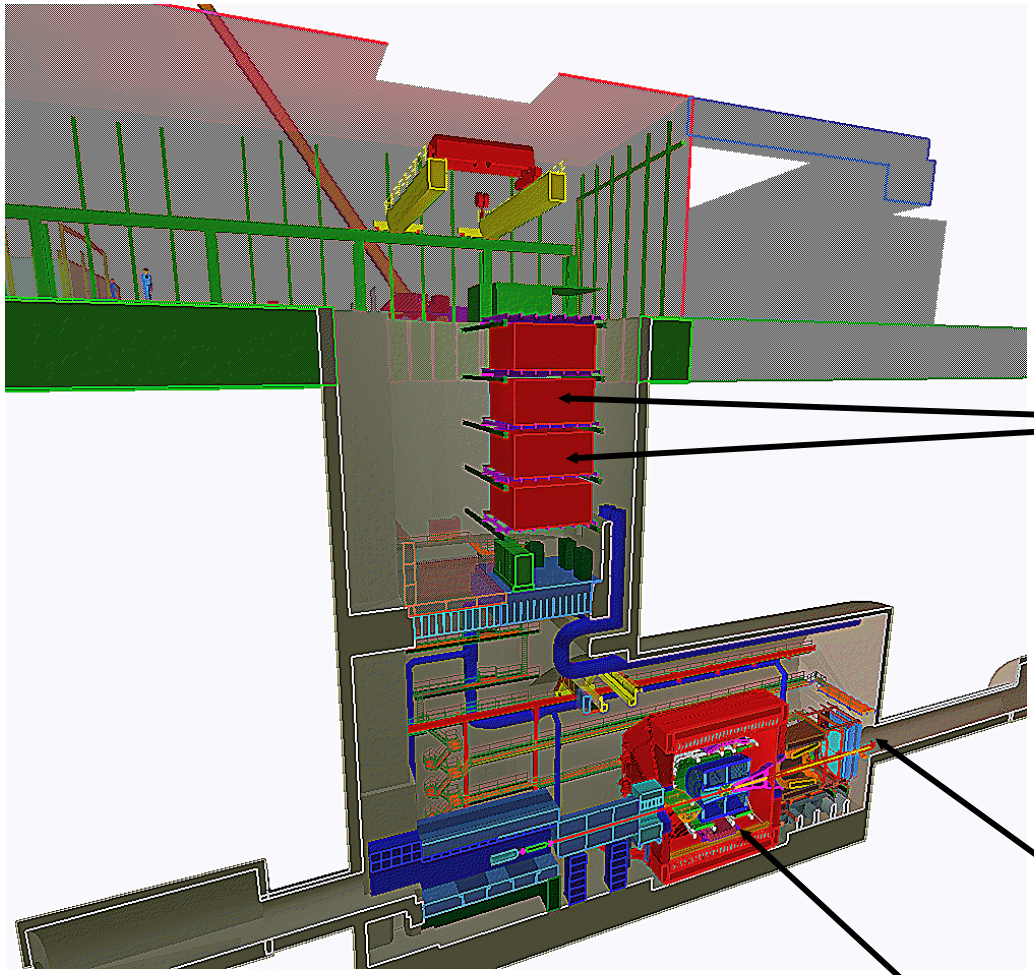
Clusterfinding 1



Clusterfinding 2



HLT in the pit – Counting Room 2 &3



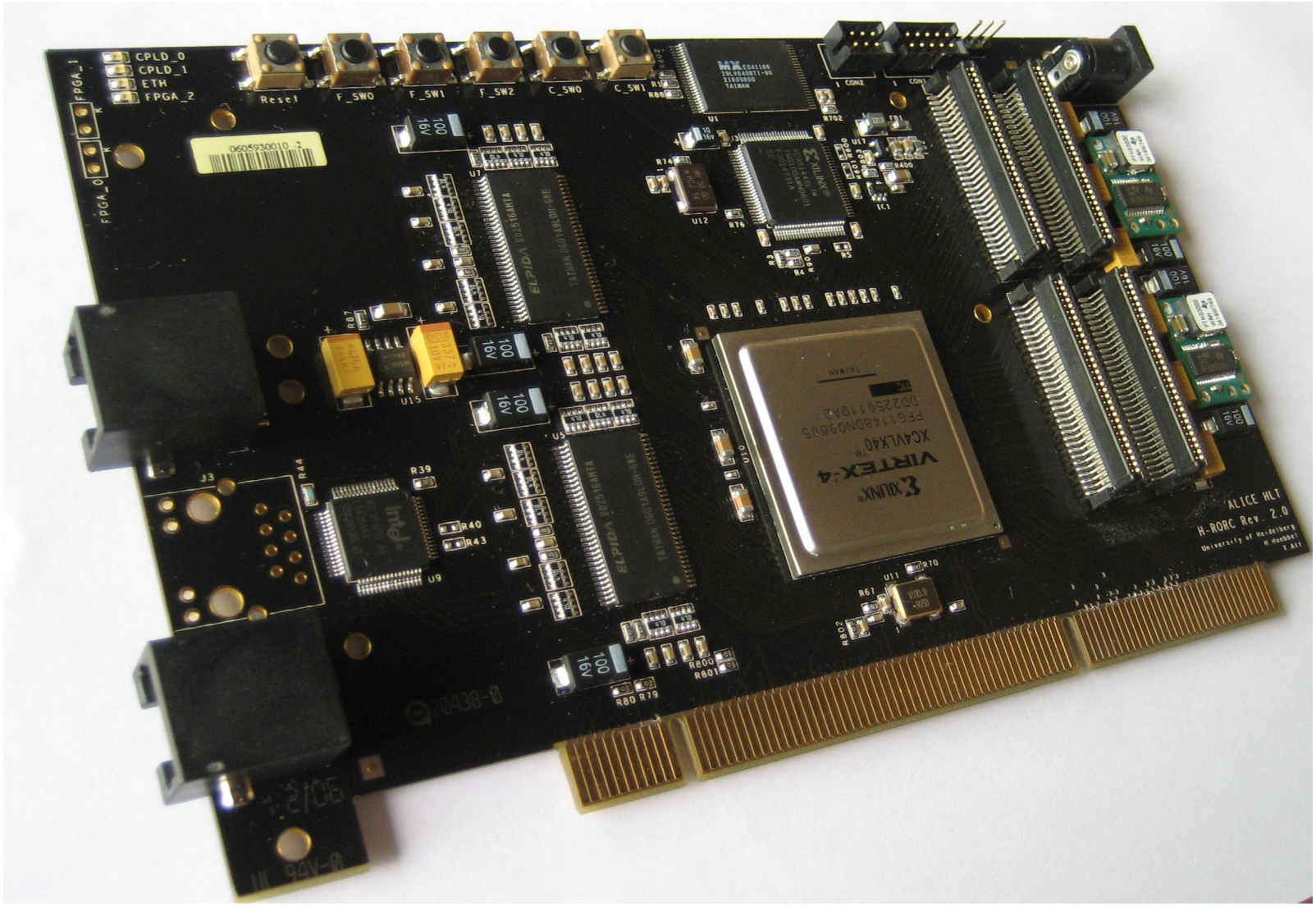
The HLT Cluster

HLT Prototype at KIP

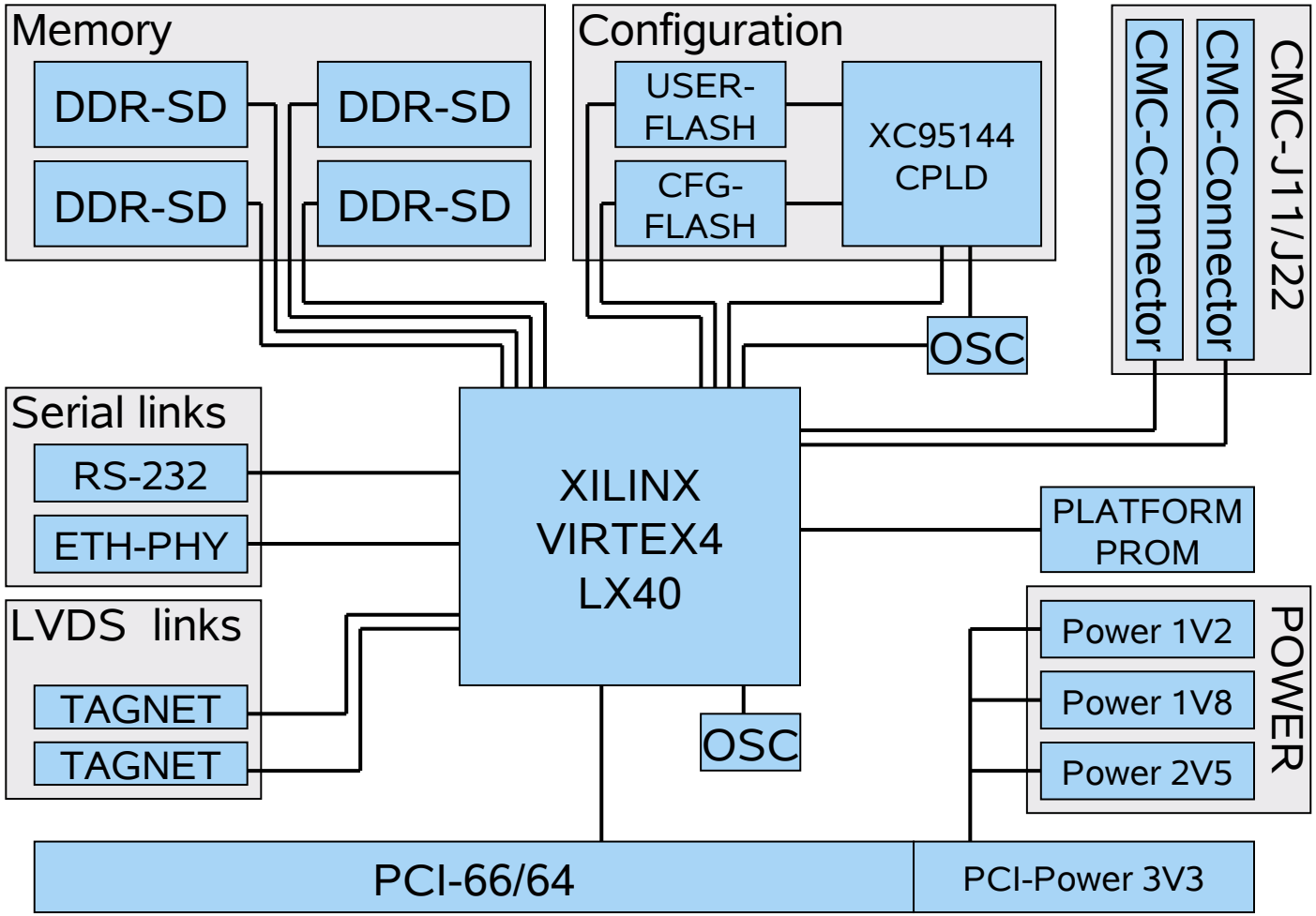
First Stage :

- Installation will take place from 28.2 to 7.3.
- 80 server with 2 x DualCore Opteron
- Each server will be equipped with 2 RORCs
- Each server will be equipped with a remote control system : CHARM
- 216 incoming DDLs for the TPC
- 10 outgoing DDLs to the DAQ

The H-RORC


CPLD_0
CPLD_1
ETH
FPGA_2
Reset
F_SW0
F_SW1
F_SW2
C_SW0
C_SW1
XILINX
VIRTEX-4
XC4VLX40
ALICE HLT
H-RORC Rev. 2.0

H-RORC Block diagramm



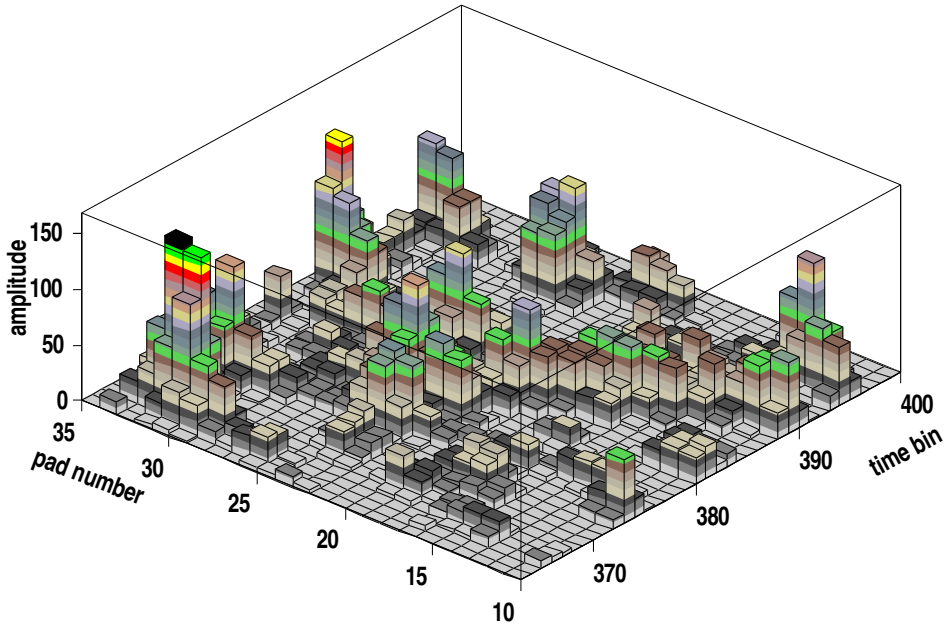
H-RORC Overview

- H-RORC : *HLT Read-Out Receiver Card*

- Tasks:
  - Receiving of the raw detector data
  - Injecting the data into the main memory of the hosts of the HLT framework
  - Online processing of the data in hardware
  - Sending processed data out of the HLT
  - Serve as a developing platform for new designs

- Requirements :
  - Flexible and modulare architecure
  - Possibility to upgrade to larger FPGAs
  - Safe update of the firmware

Clusterfinding in the FPGA 1



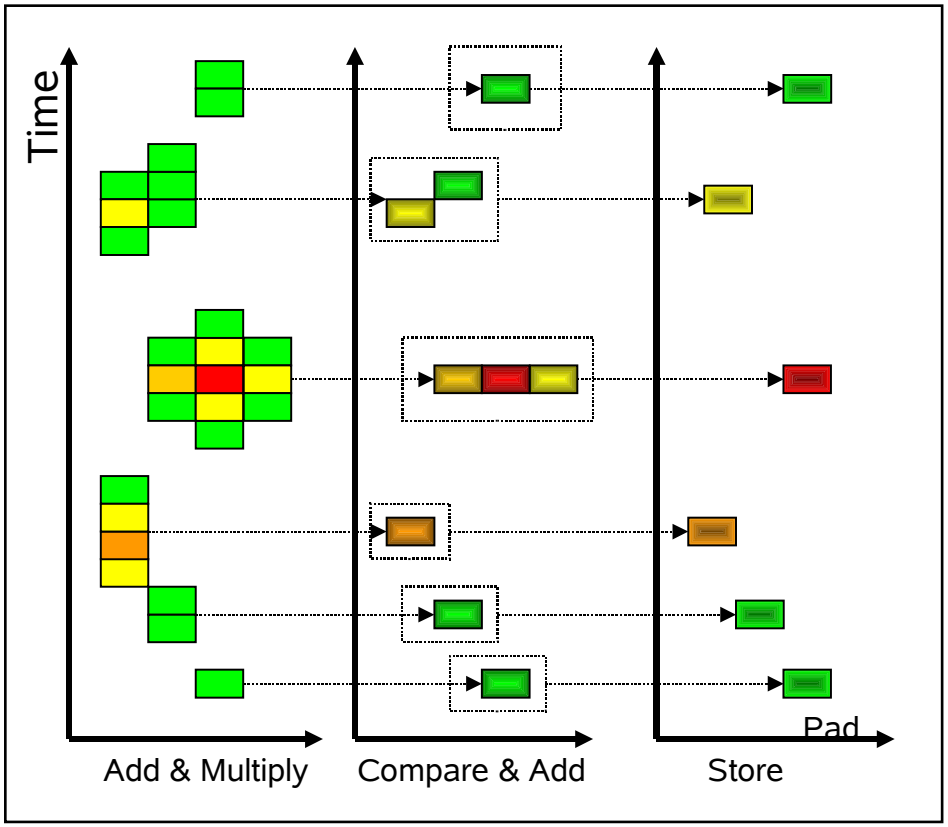
- Each datapoint is represented by 4-dimensional vector

  (row, pad, time, charge)
- Processing can by done for each row independently:

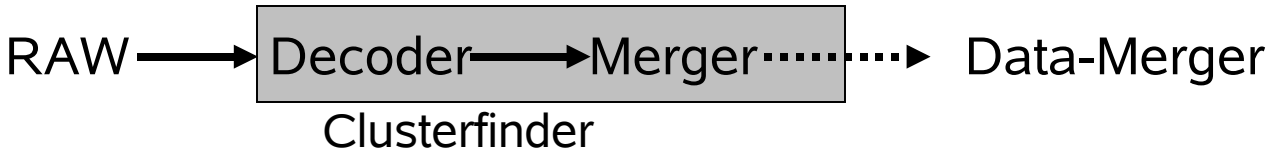
  Clusterfinding is a parallel process
- Clusterfinder operates on

  (pad, time, charge)
- Main operations: add, multiply, compare, store
- Main operations can be done in parallel

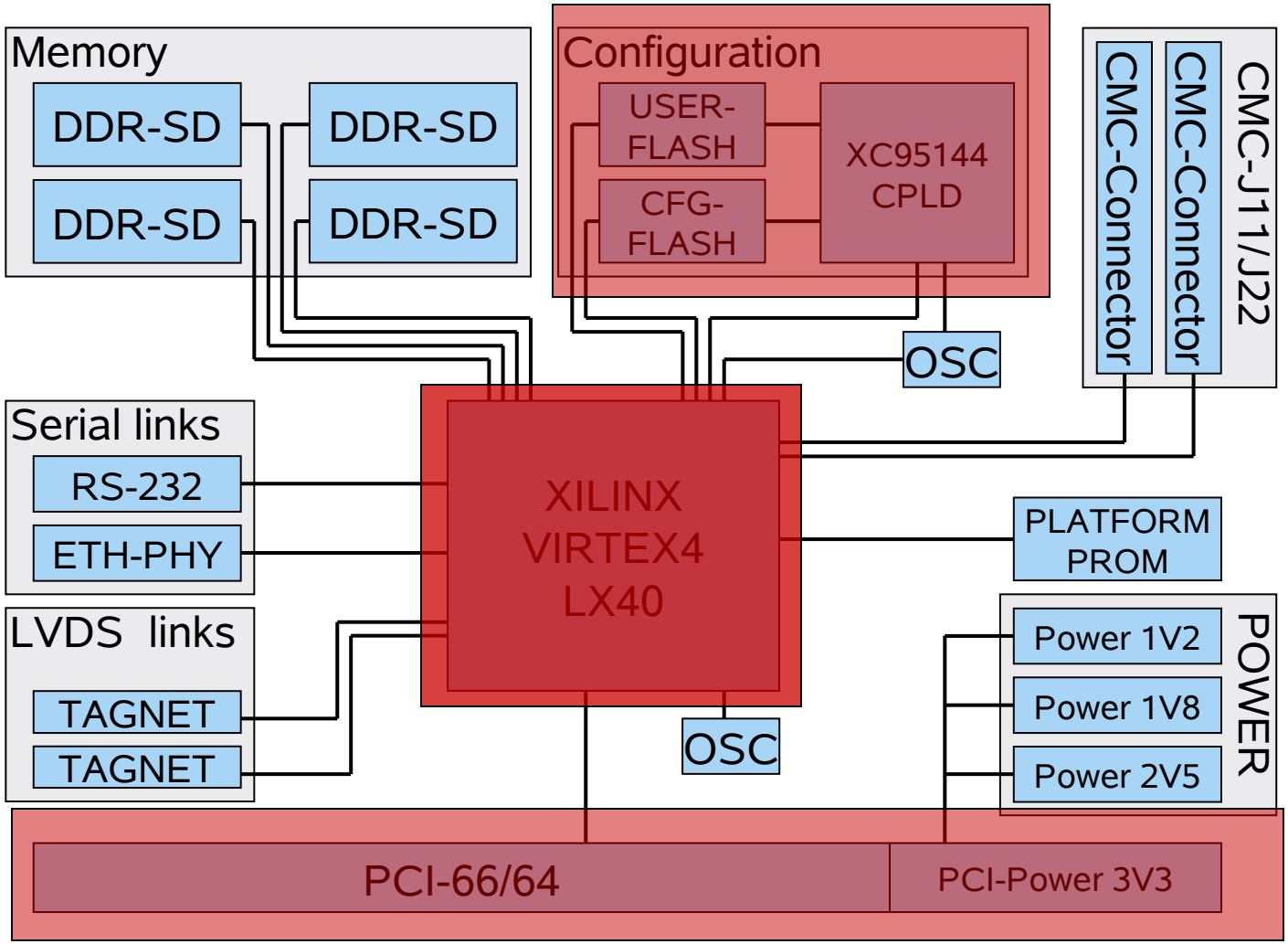
Clusterfinding in the FPGA 2



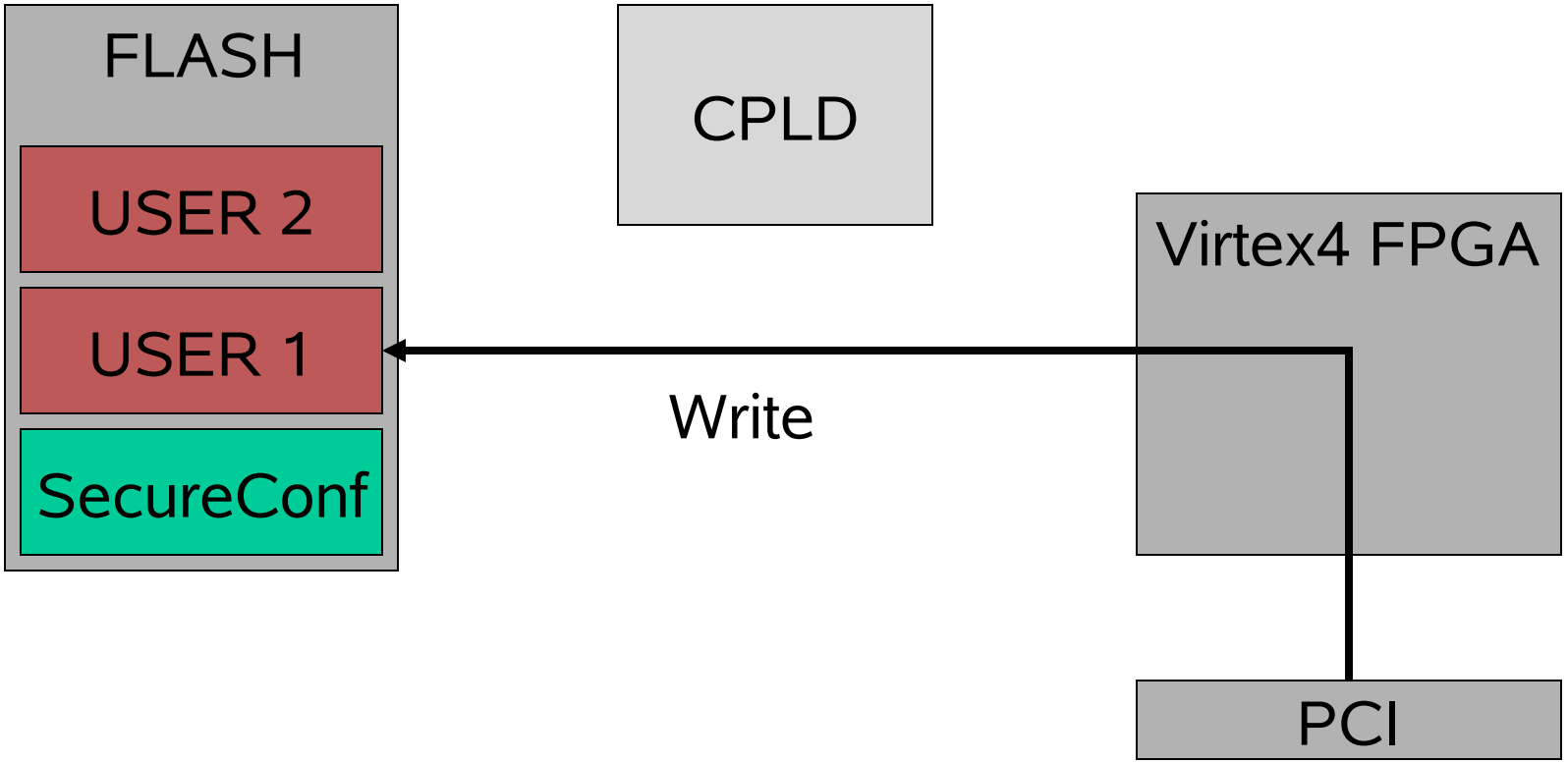
- 1.stage: CF-DECODER
  CF calculate the weighted time, the sequential charge and the total charge.
- 2.stage: CF-MERGER
  The values are compared and merged if they correspond
- 3.stage: DATA-MERGER
  The clusters are written to a memory



Secure Configuration

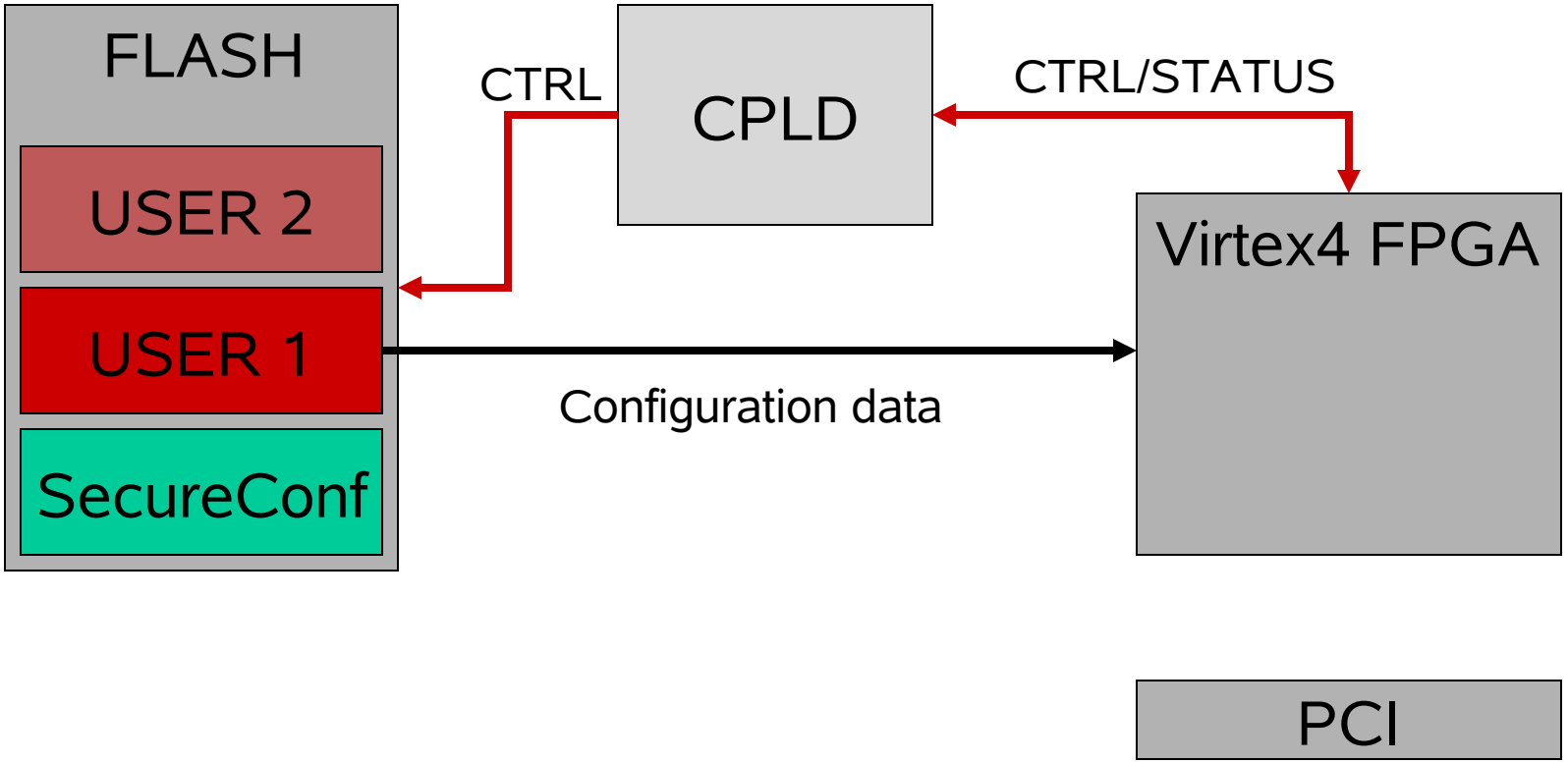


Secure Configuration 2



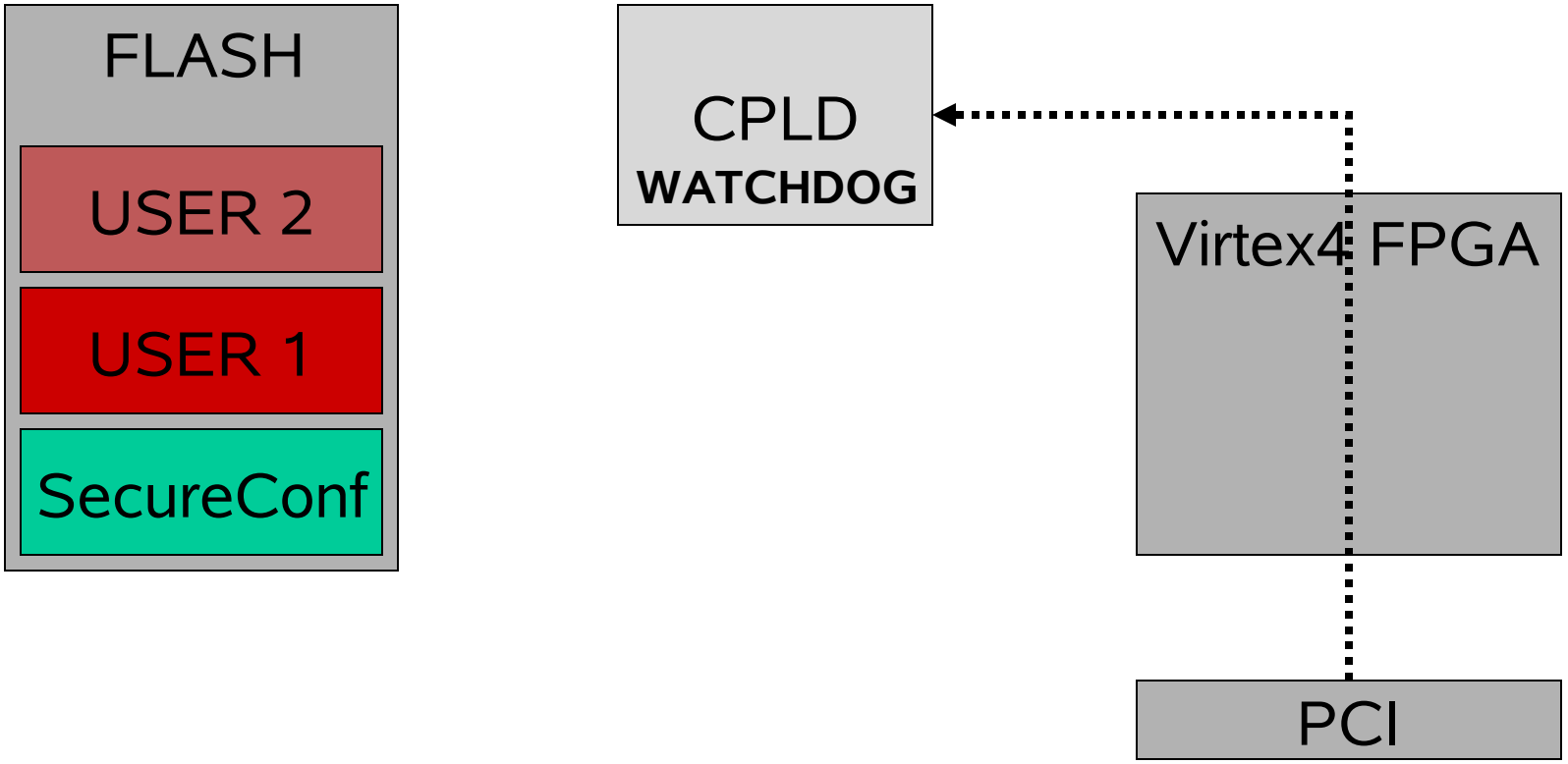
A user configuration can be written to the FLASH via PCI. Depending on the size of the FLASH several user configurations can be stored.

Secure Configuration 3



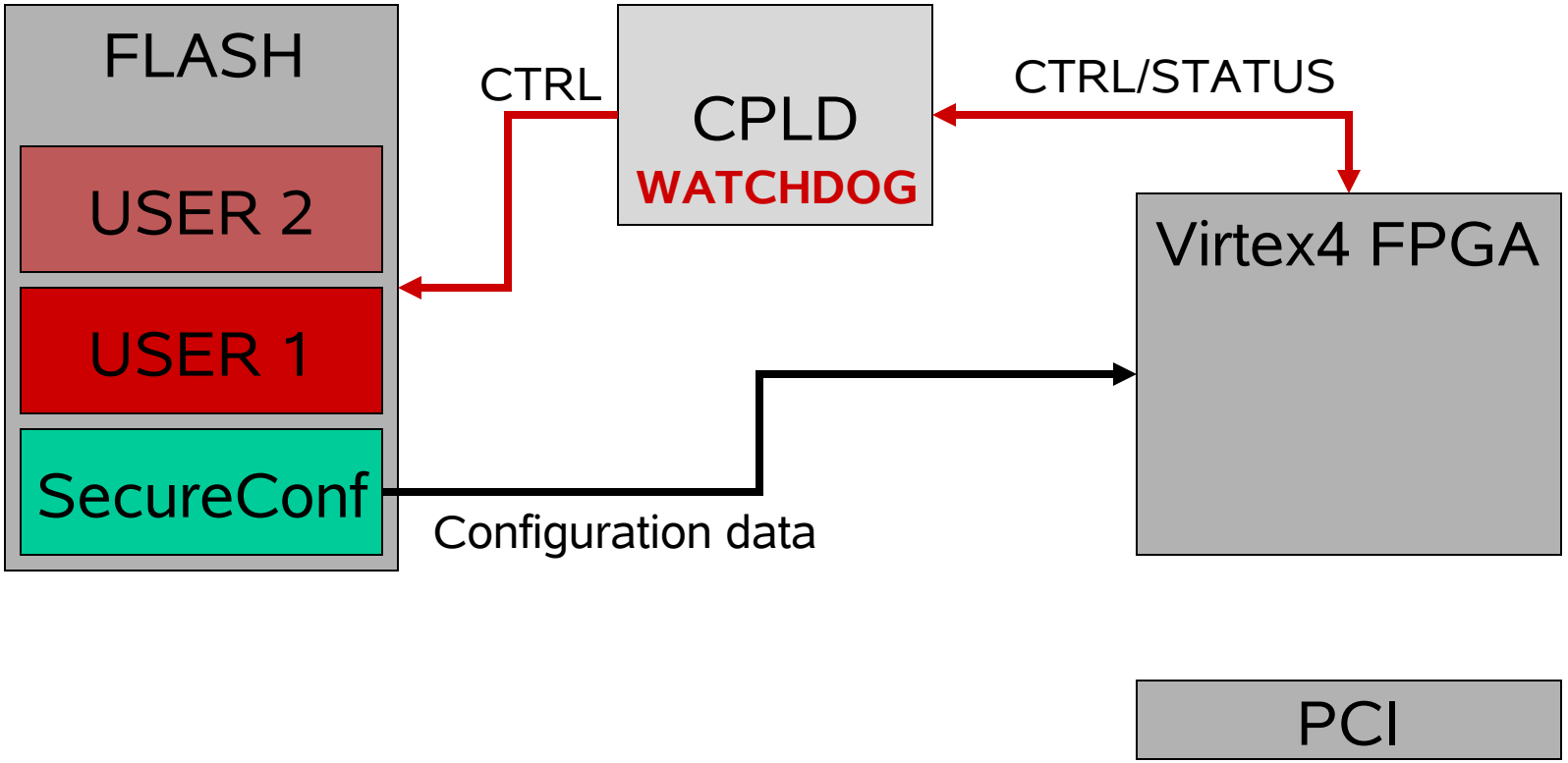
The CPLD checks the FLASH for a valid user configuration and the FPGA is then configured with this configuration

Secure Configuration 4



After configuration a watchdog is enabled inside the CPLD. It needs to be disabled by a defined sequence send via PCI. If anything goes wrong and the watchdog isn`t disabled, it will time out and the FPGA will be reconfigured with the SecureConf.

Secure Configuration 5



The watchdog has timed out and the FPGA is reconfigured with the SecureConf. The SecureConf contains a design which will always give access to the FLASH via PCI.