The ALICE TRD Trigger System

Overview and Current Status

Outline

- Introduction to TRD Trigger for ALICE
- TRD Online Global Tracking
- From Tracklets to Trigger: Algorithm
- Low-latency Trigger Hardware: Track Matching Unit
- Results from Current Test Setup
- Summary and Status

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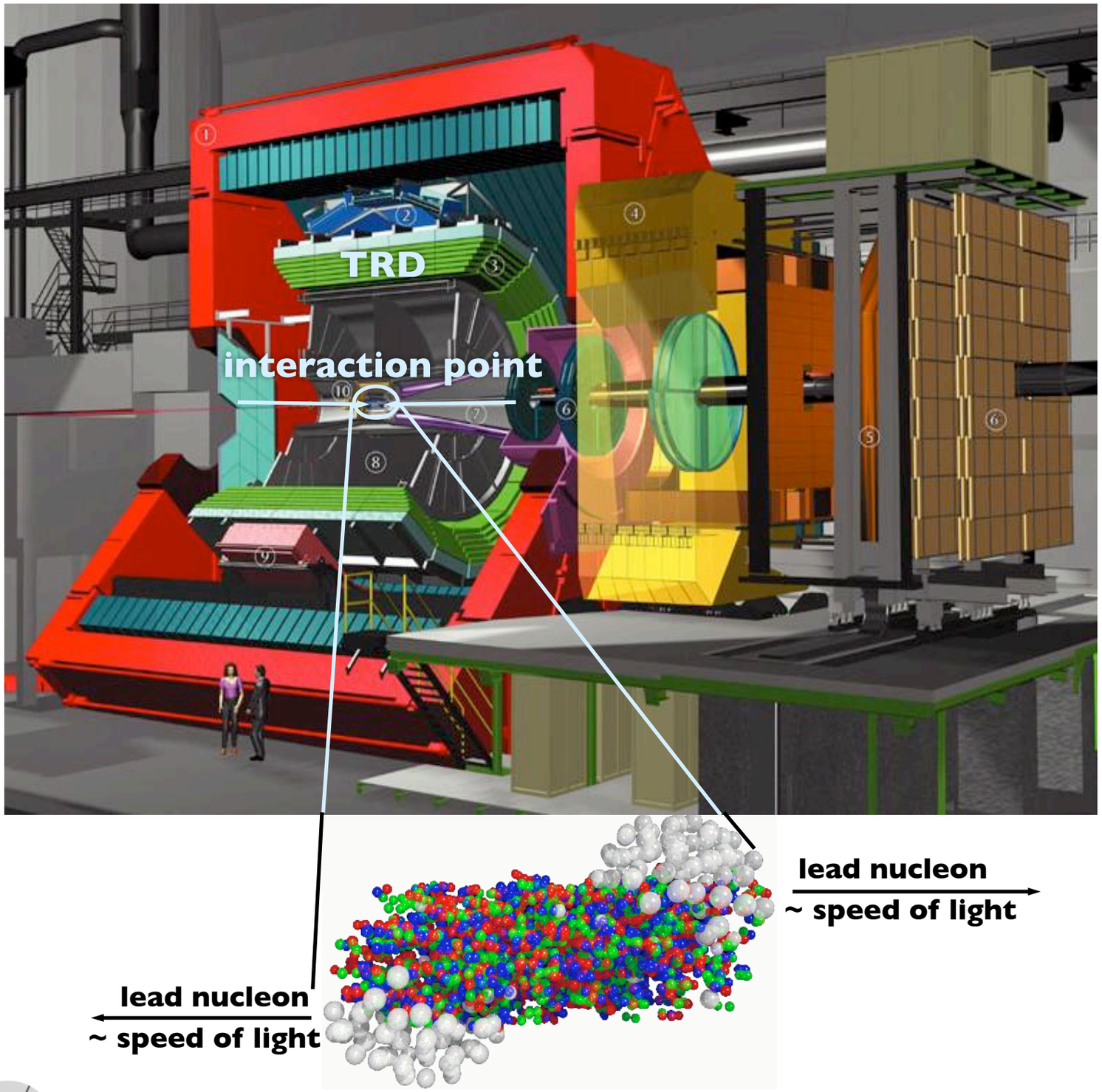
IRTG Meeting
2007-02-26 in Heidelberg

ALICE Experiment Overview



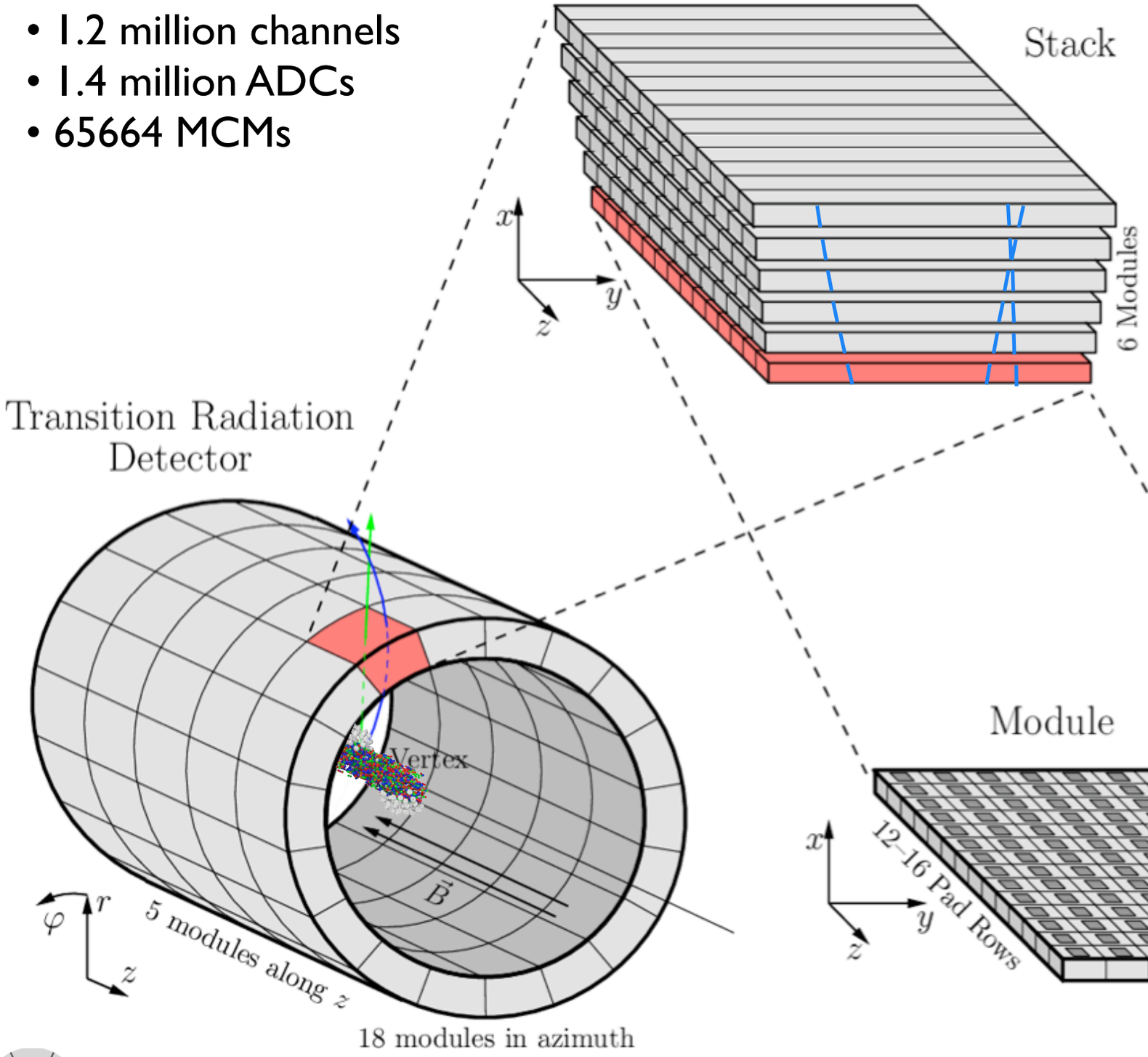
ALICE

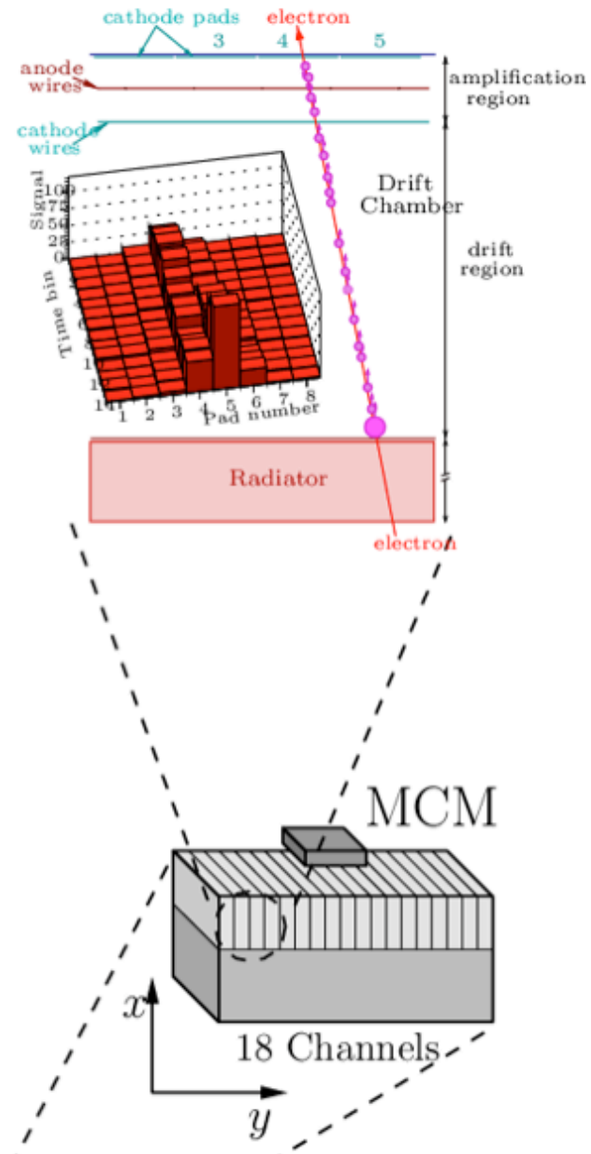
- 1150 TeV Pb-Pb interactions
- 8000 collisions per second
- Detectors for
  - **Trigger** (diff. levels): ITS, TRD
  - High resolution tracking: TPC
  - ...

Goal is to create the Quark-Gluon Plasma, a state of matter existing during the first few microseconds after the big bang

Transition Radiation Detector – TRD

- 1.2 million channels
- 1.4 million ADCs
- 65664 MCMs

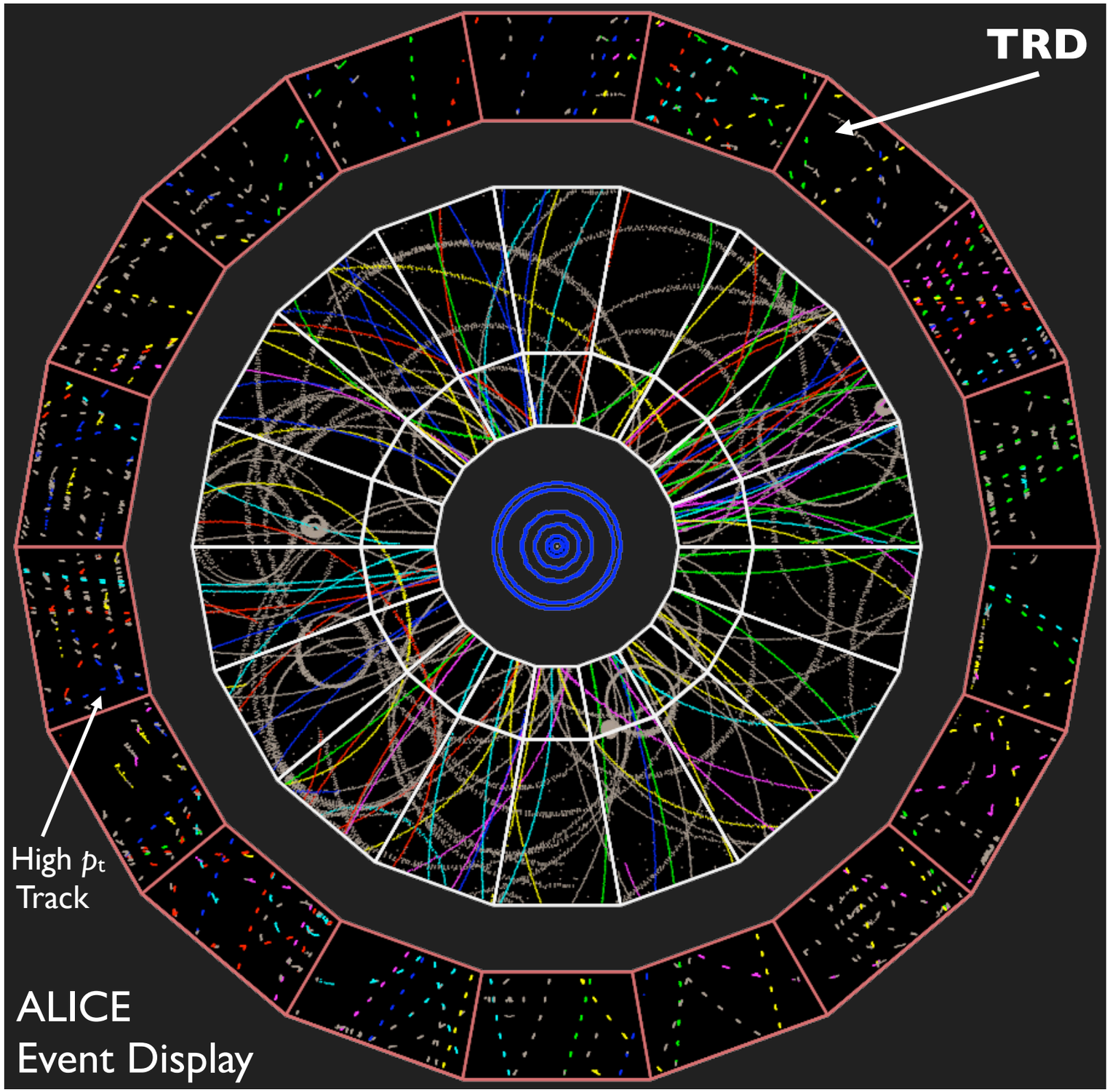




MCMs perform amplification, digitization, linear fit and read-out

TRD Trigger Tasks

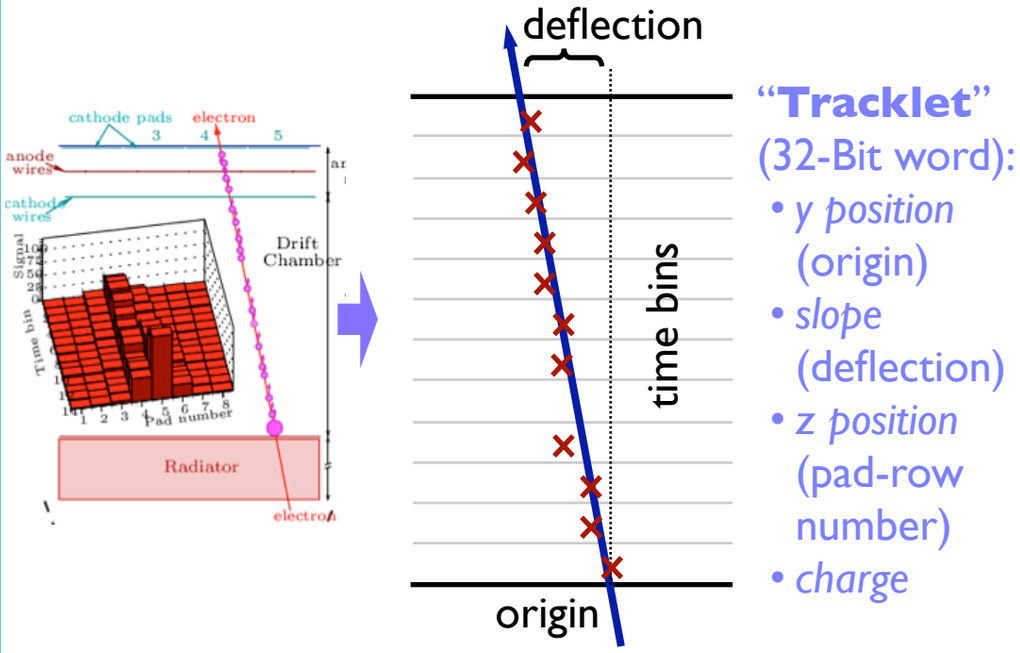
- Complex trigger system
- Objective:
  - Find high p_t electron pairs
- Tasks:
  - Reconstruct tracks
  - Analyze tracks
- Trigger decision required after 6 µs
  - Primary design objective: minimize latency



TRD Trigger Timing

Charge Cluster to Tracklet

- Local tracking units on detector perform linear fits and reject uninteresting data

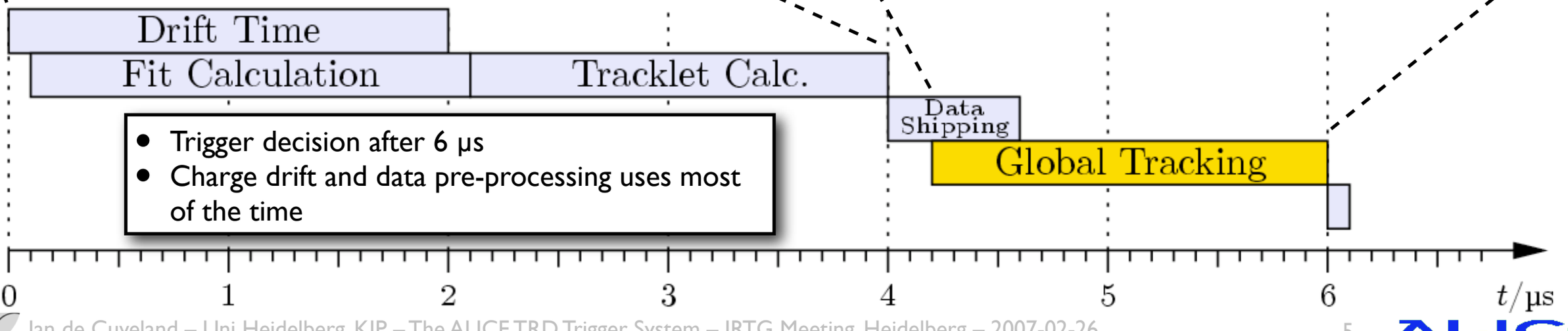


"**Tracklet**" (32-Bit word):

- *y position* (origin)
- *slope* (deflection)
- *z position* (pad-row number)
- *charge*

Global Tracking

- Inside GTU (Global Tracking Unit)
- Objective: find high momentum tracks
- Search for tracklets belonging together
- Combine tracklets from all six layers
- Reconstruct p_t, compare to threshold and generate trigger
- Constraint:
  only approx. 1.5 µs processing time



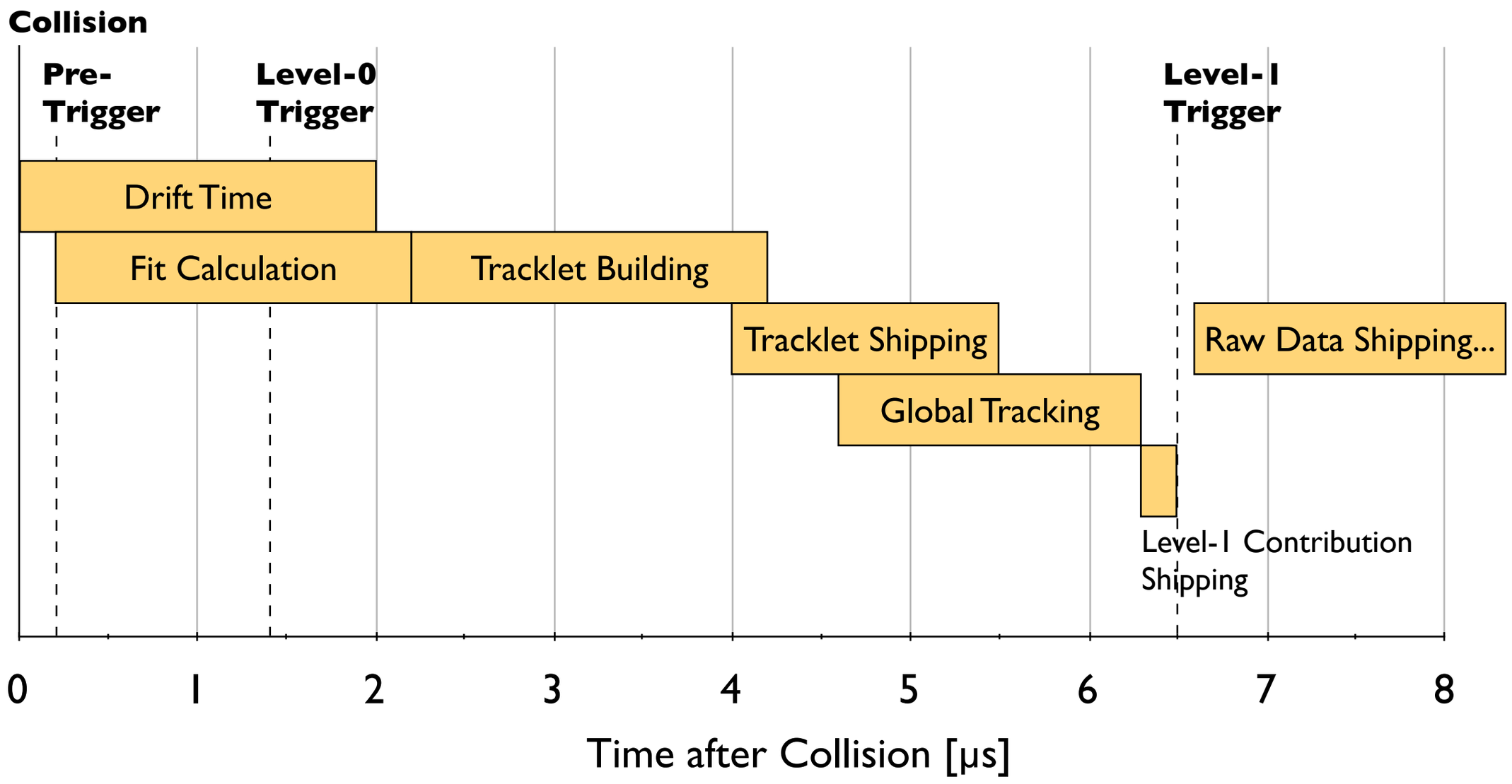
- Trigger decision after 6 µs
- Charge drift and data pre-processing uses most of the time

ALICE Trigger Hierarchy

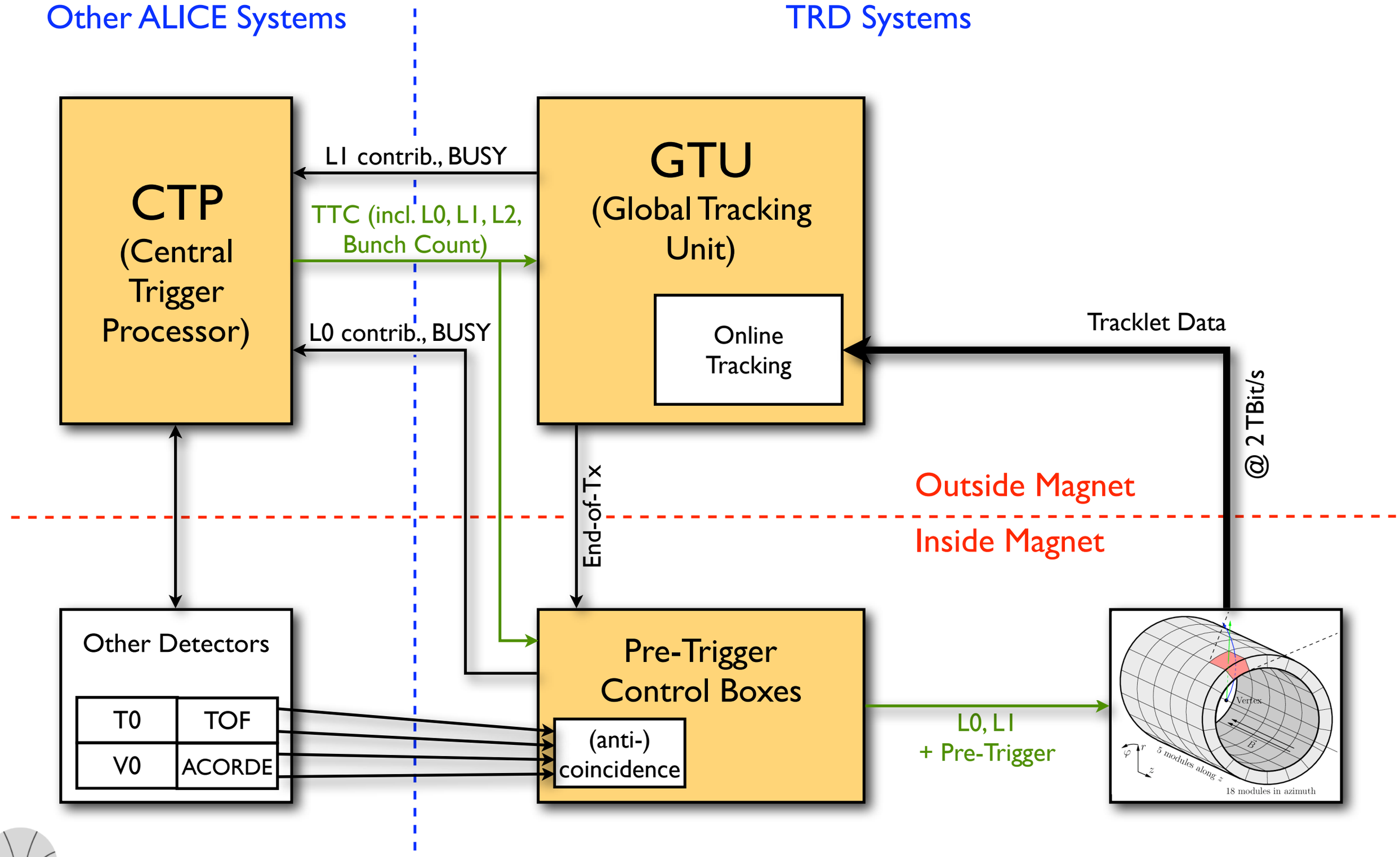
- To account for different detector latencies, there are several levels in the ALICE trigger:

Trigger	Pre-Trigger	Level-0	Level-1	Level-2	High-Level
Time after Interaction	0.2 μs	1.2 μs	6.5 μs	~ 88 μs	> 1 ms
Average Rate (Pb-Pb)	~ 5000 Hz	~ 5000 Hz	~ 400 Hz	~ 200 Hz	~ 100 Hz
Description/Use	TRD Specific Wake-Up	Strobe to Sampling Electronics	Major Rate Reduction	TPC Past-Future Protection	Software Trigger, Data Compression
TRD Contribution	generated for TRD	TRD contributes to L0 via Pre-Trigger	TRD contributes to L1 via GTU	–	–

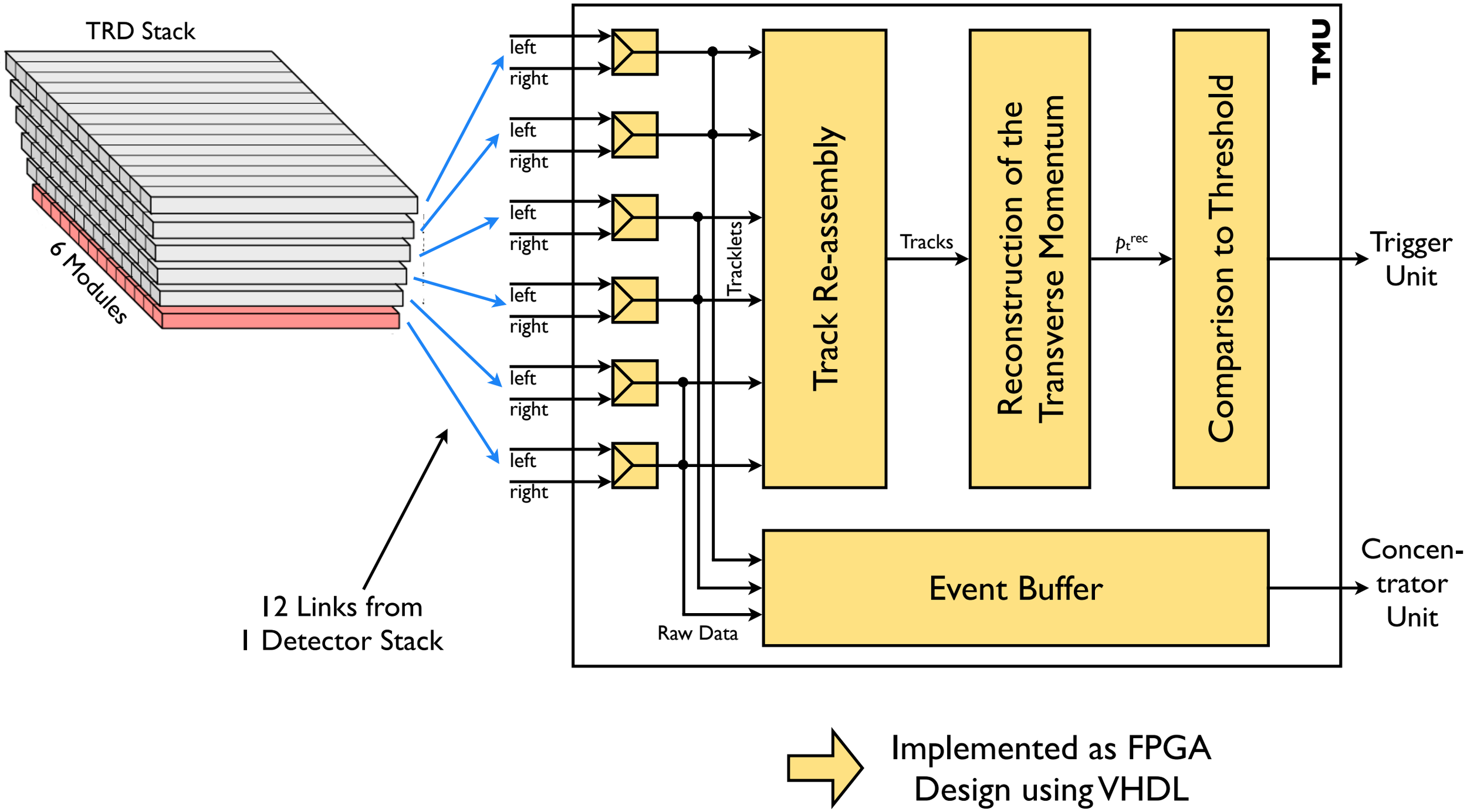
TRD Trigger Timing



TRD Trigger System Overview

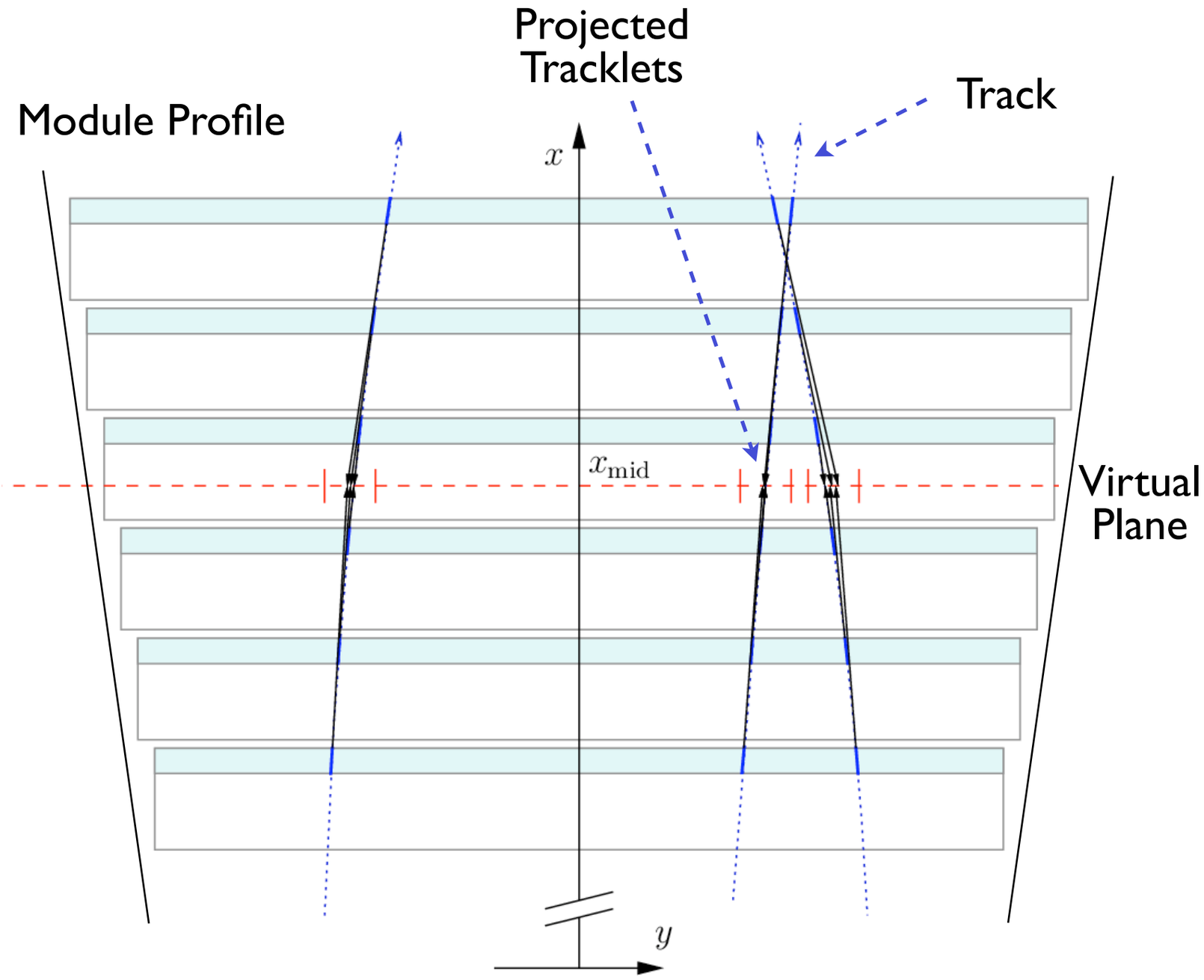


Track Matching Unit (TMU): From Tracklets to Trigger



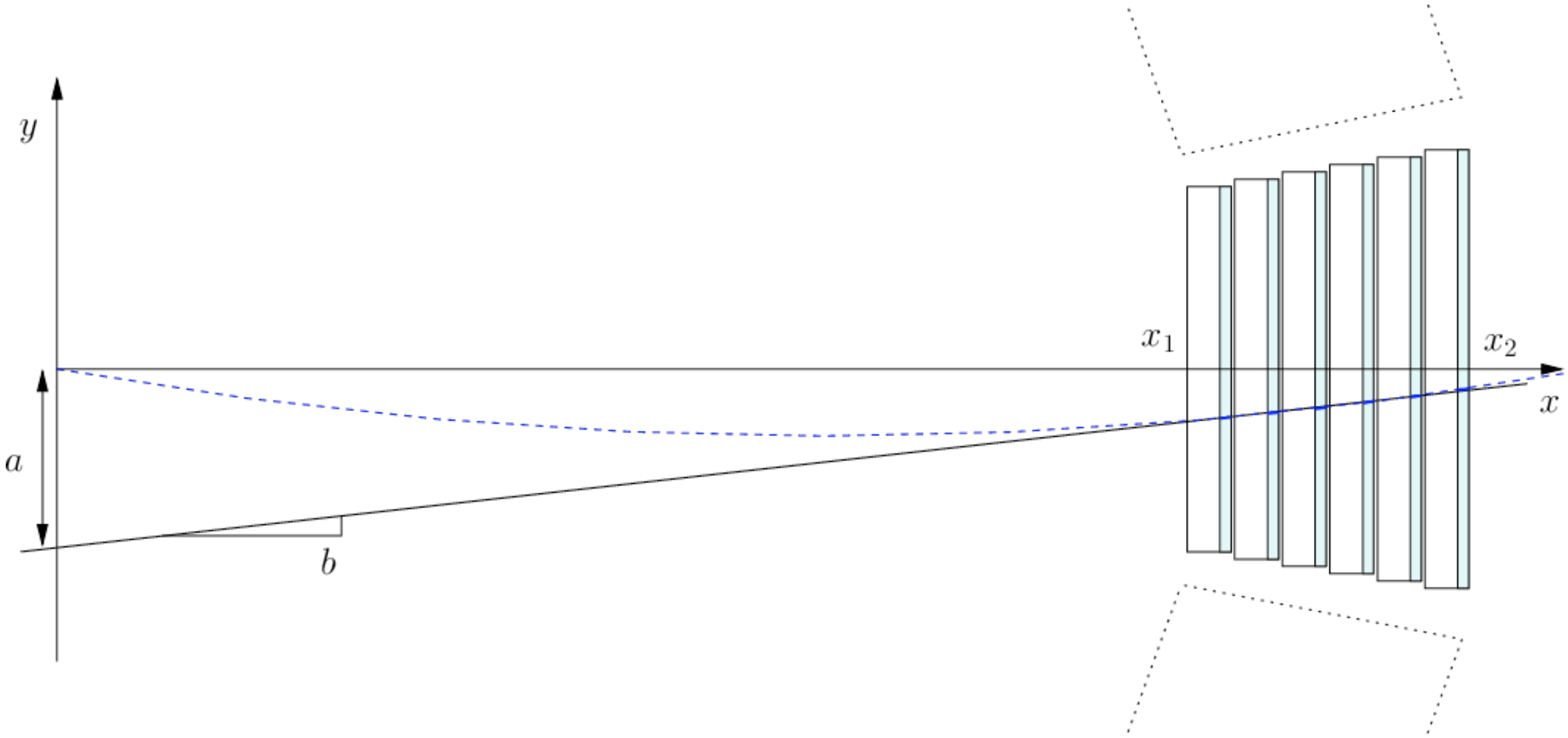
Implemented as FPGA Design using VHDL

Track Re-assembly



- Search for tracklets belonging together (3-dimensional matching task)
- Projection of tracklets to virtual plane
- Sliding window algorithm
- A track is found, if ≥ 4 tracklets from different layers inside same multi-dimensional window

Reconstruction of the Transverse Momentum

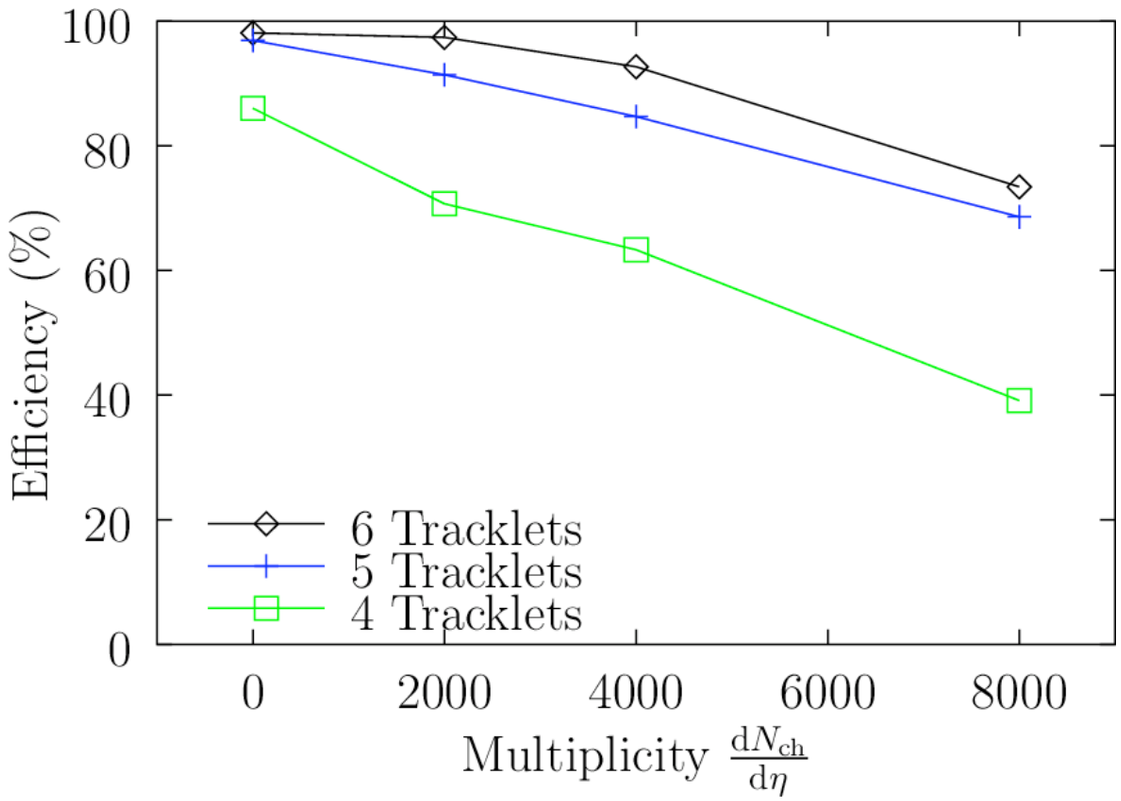


- Calculate linear fit of (unprojected) *y* positions of tracklets
- Estimate transverse momentum from line parameter *a*
- Uses look-up tables, additions and multiplications

Simulation Results

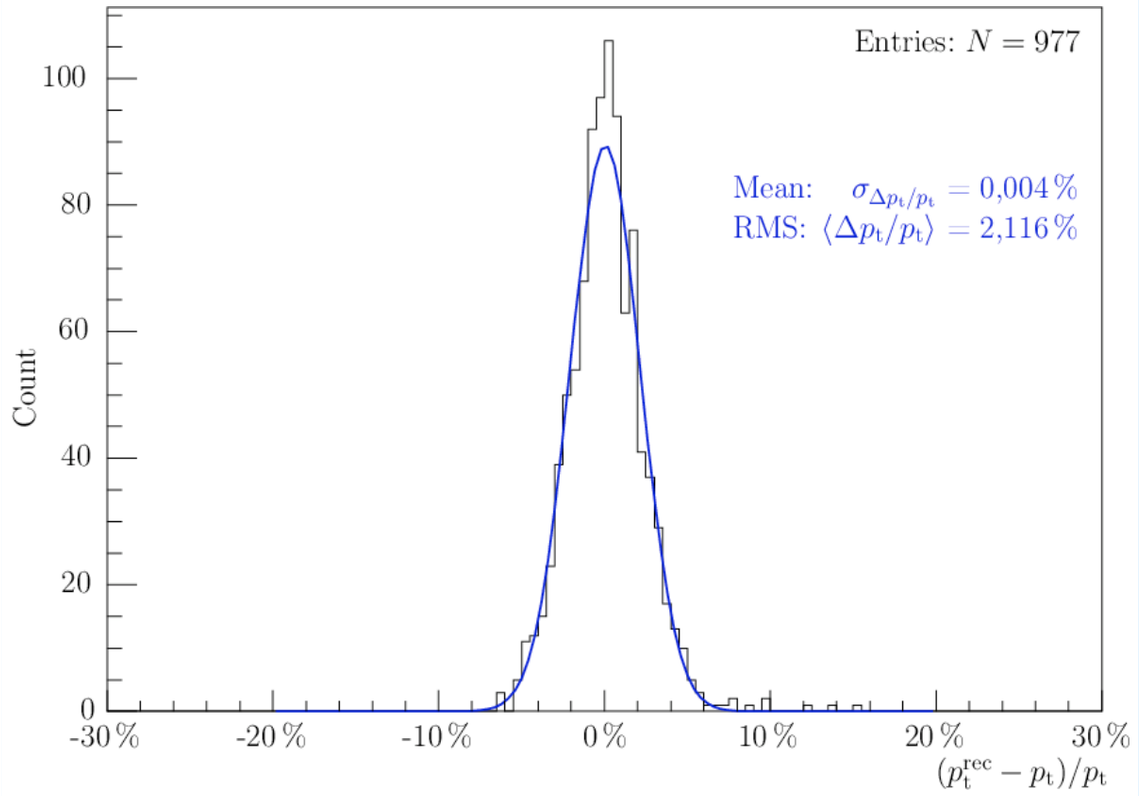
- Simulation with AliRoot data, electrons with p_t > 3 GeV/c

Detection Efficiency



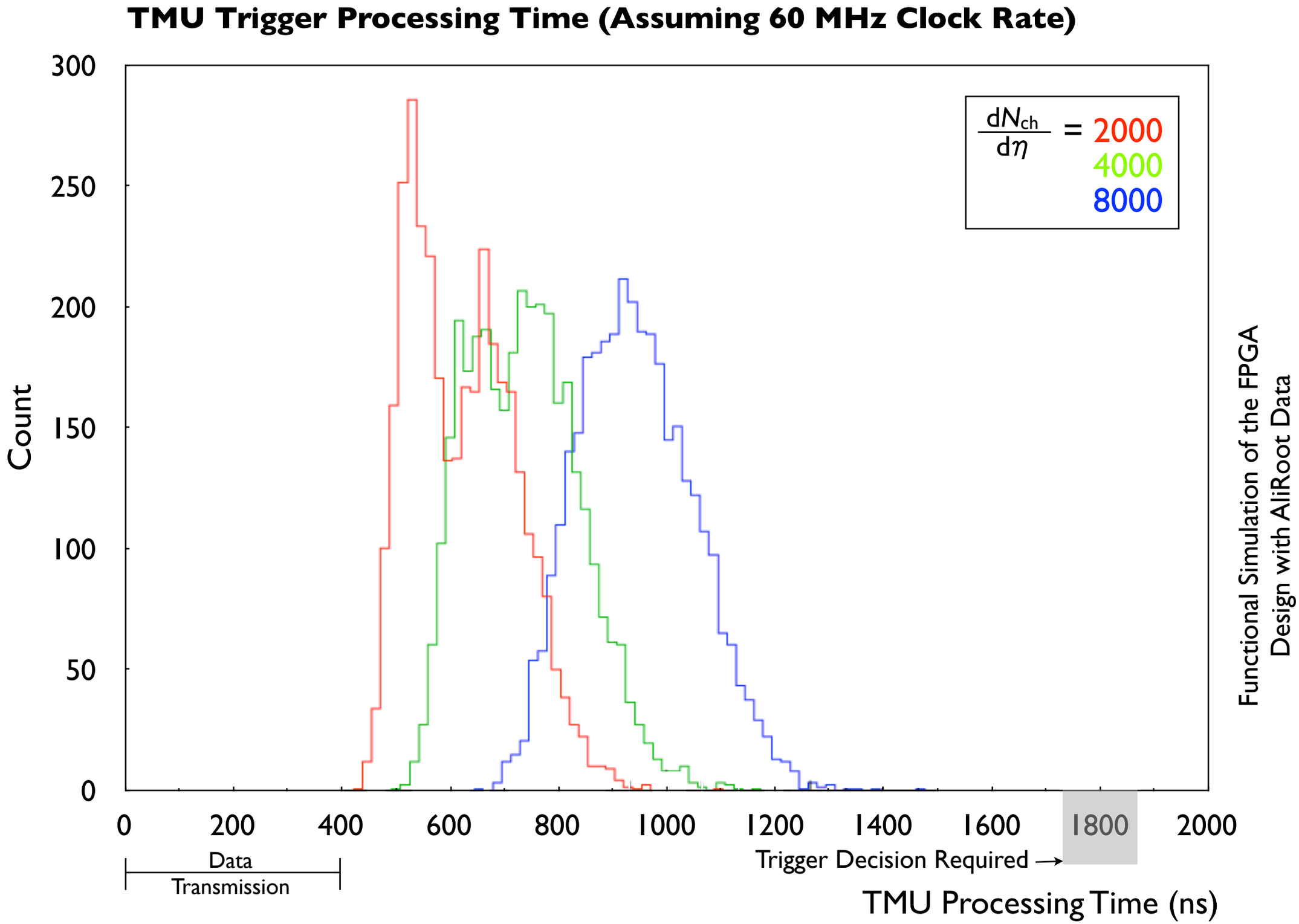
Results depend on multiplicity density $dN_{ch}/d\eta$ and number of tracklets delivered by detector

Reconstruction Precision

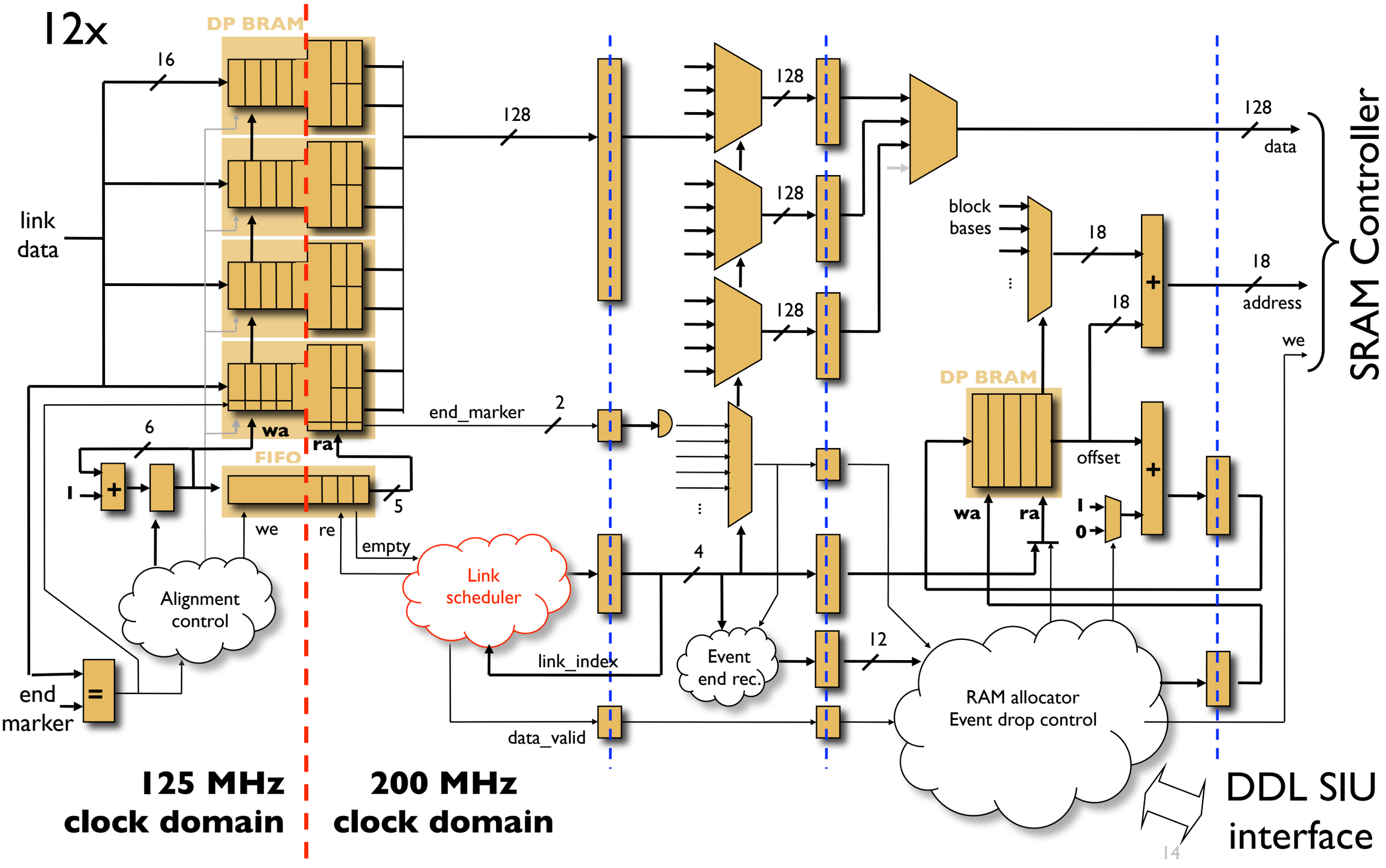


p_t reconstruction precision: 2.1 %

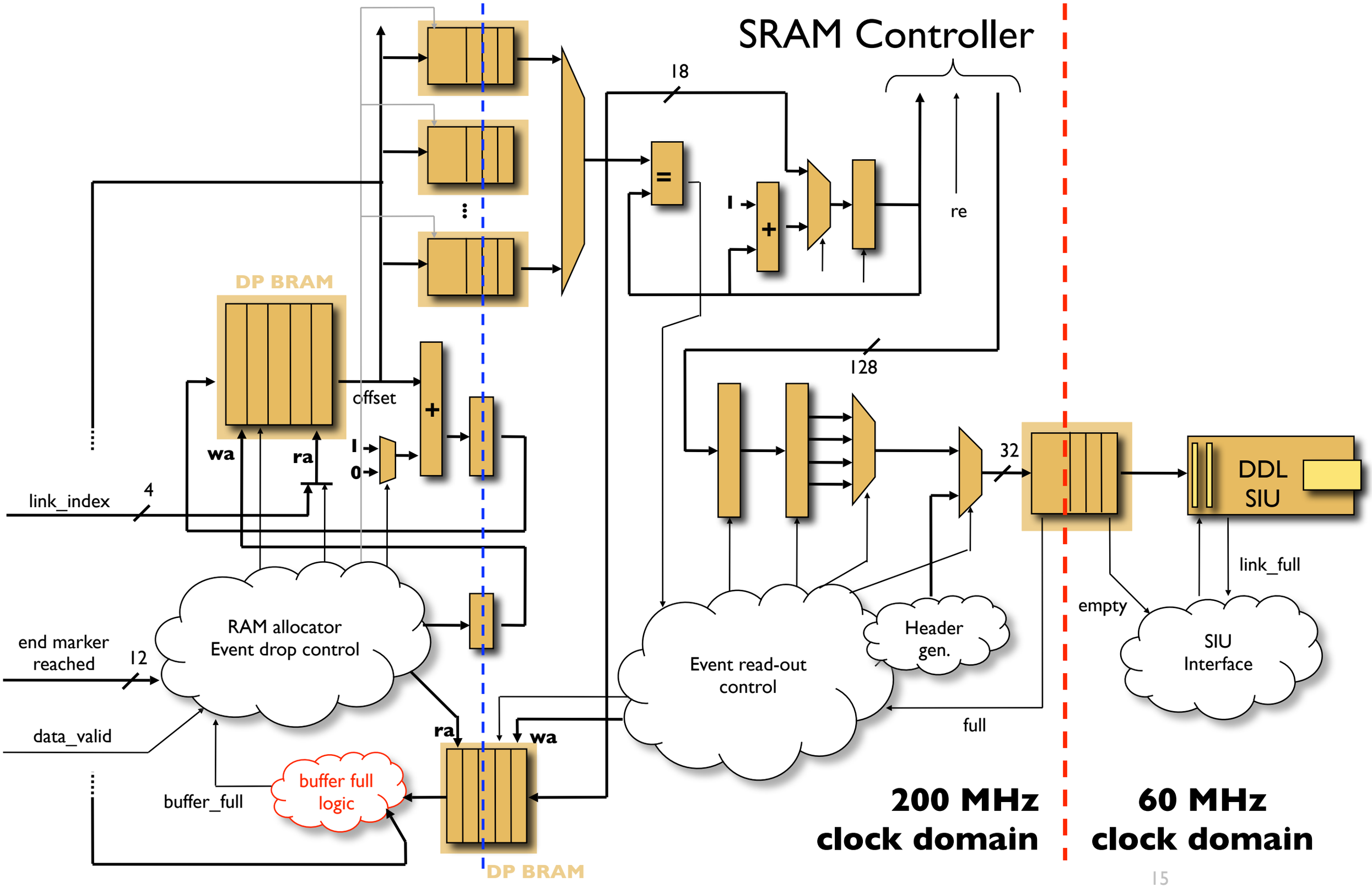
FPGA Design Results



TMU Board – Buffering Design Structure

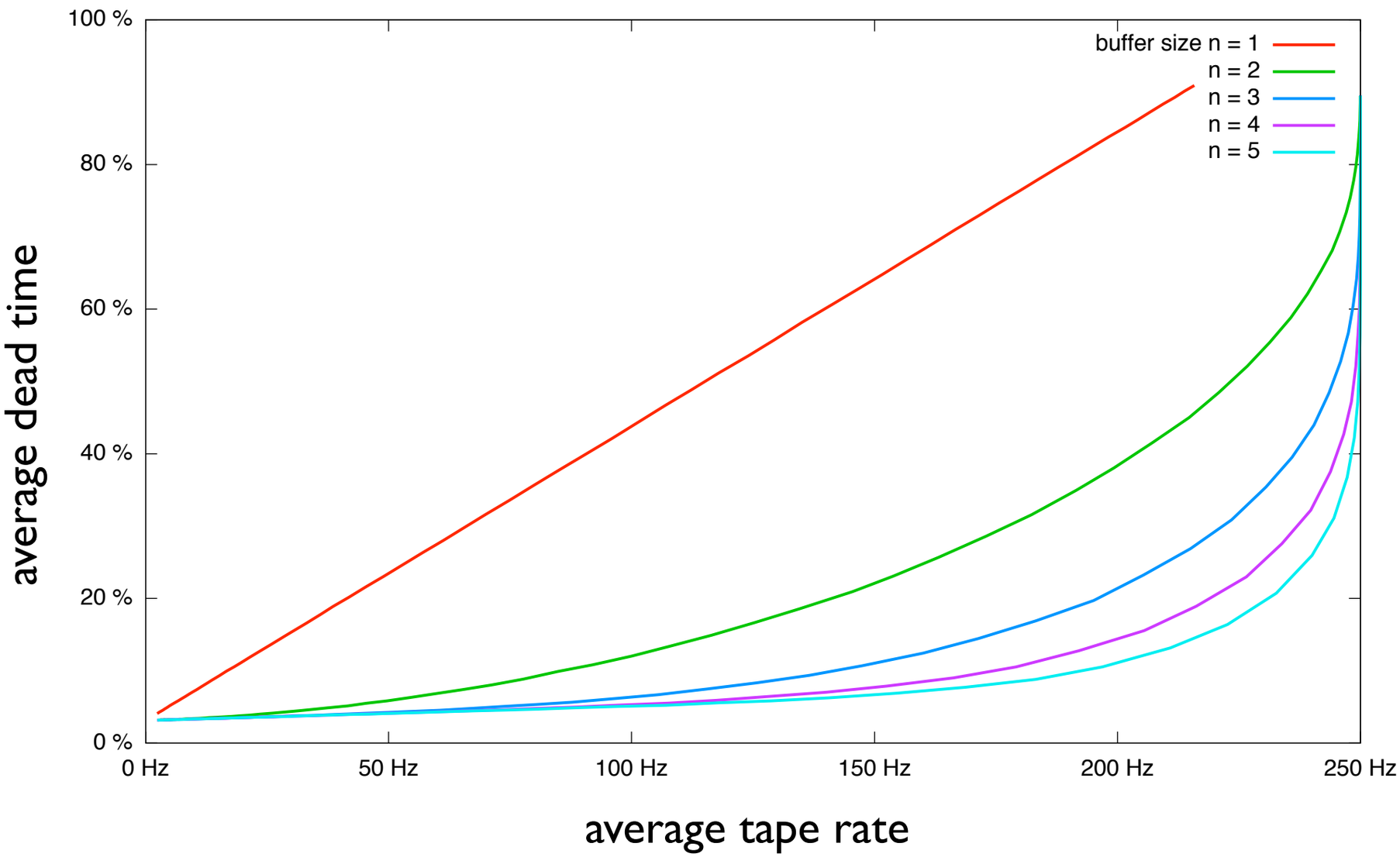


TMU Board – Buffering / SIU Interface



Multi-Event Buffering inside the GTU

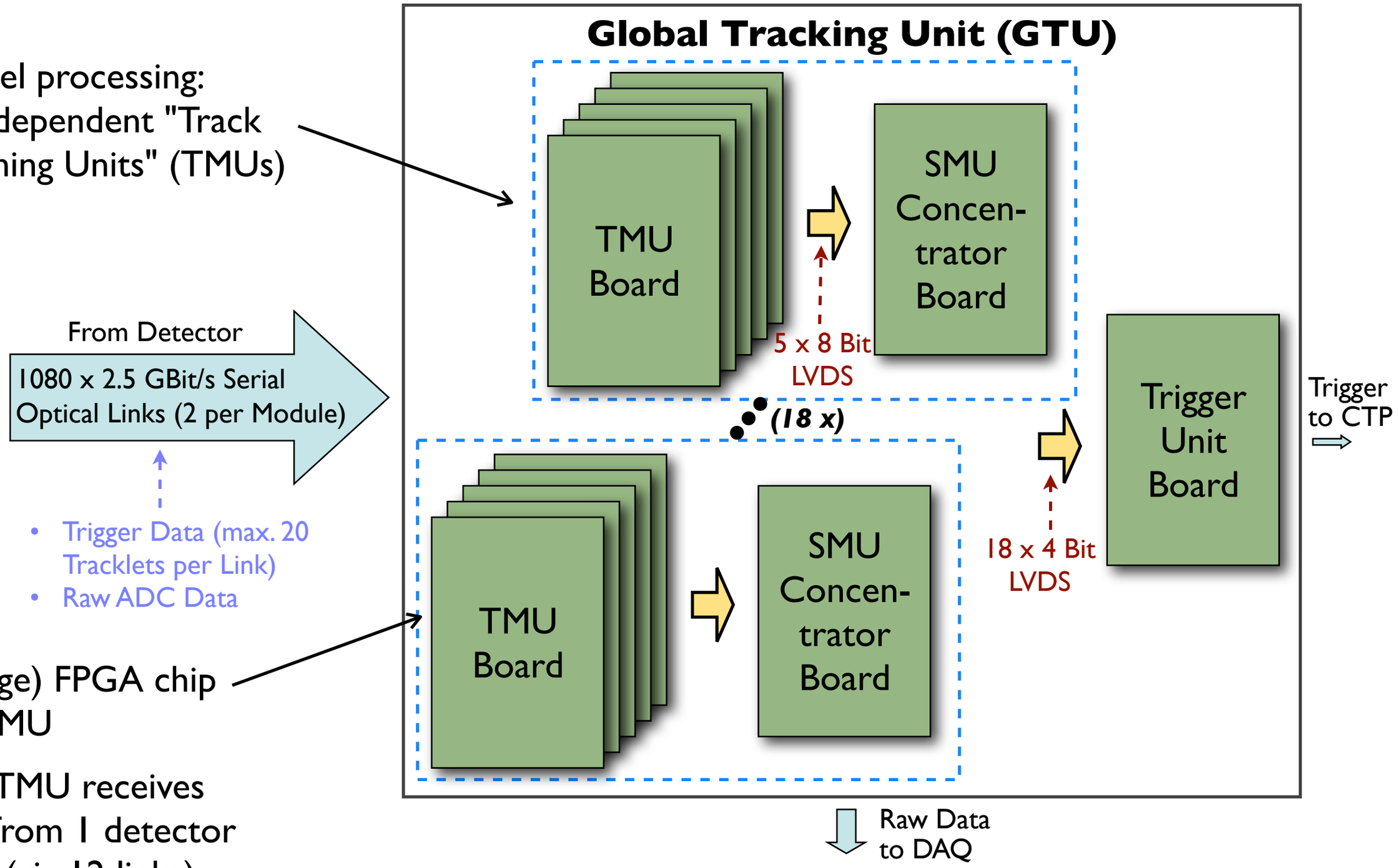
- Multi-Event buffering significantly reduces detector dead time:



(Results from Monte-Carlo Simulation of Trigger Timing)

GTU Architecture

Parallel processing:
90 independent "Track Matching Units" (TMUs)

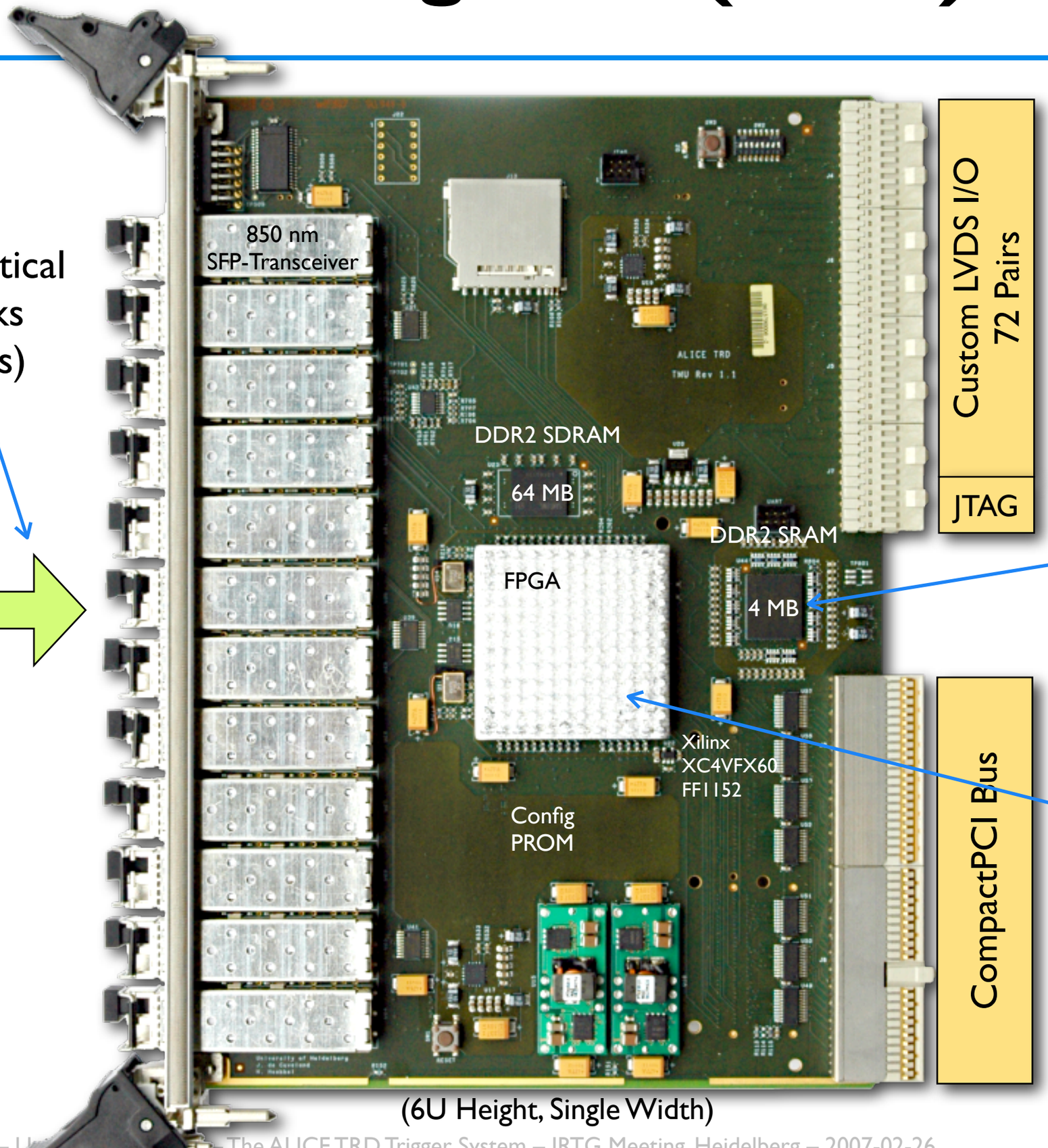


- Trigger Data (max. 20 Tracklets per Link)
- Raw ADC Data

1 (large) FPGA chip per TMU

Each TMU receives data from 1 detector stack (via 12 links)

Track Matching Unit (TMU) Board



12 Fiber Optical Serial Links (2.5 GBit/s)

From 1 Detector Stack

3 Parallel Links (120 MHz DDR, 8 Bit LVDS)

To Right TMU

From Left TMU

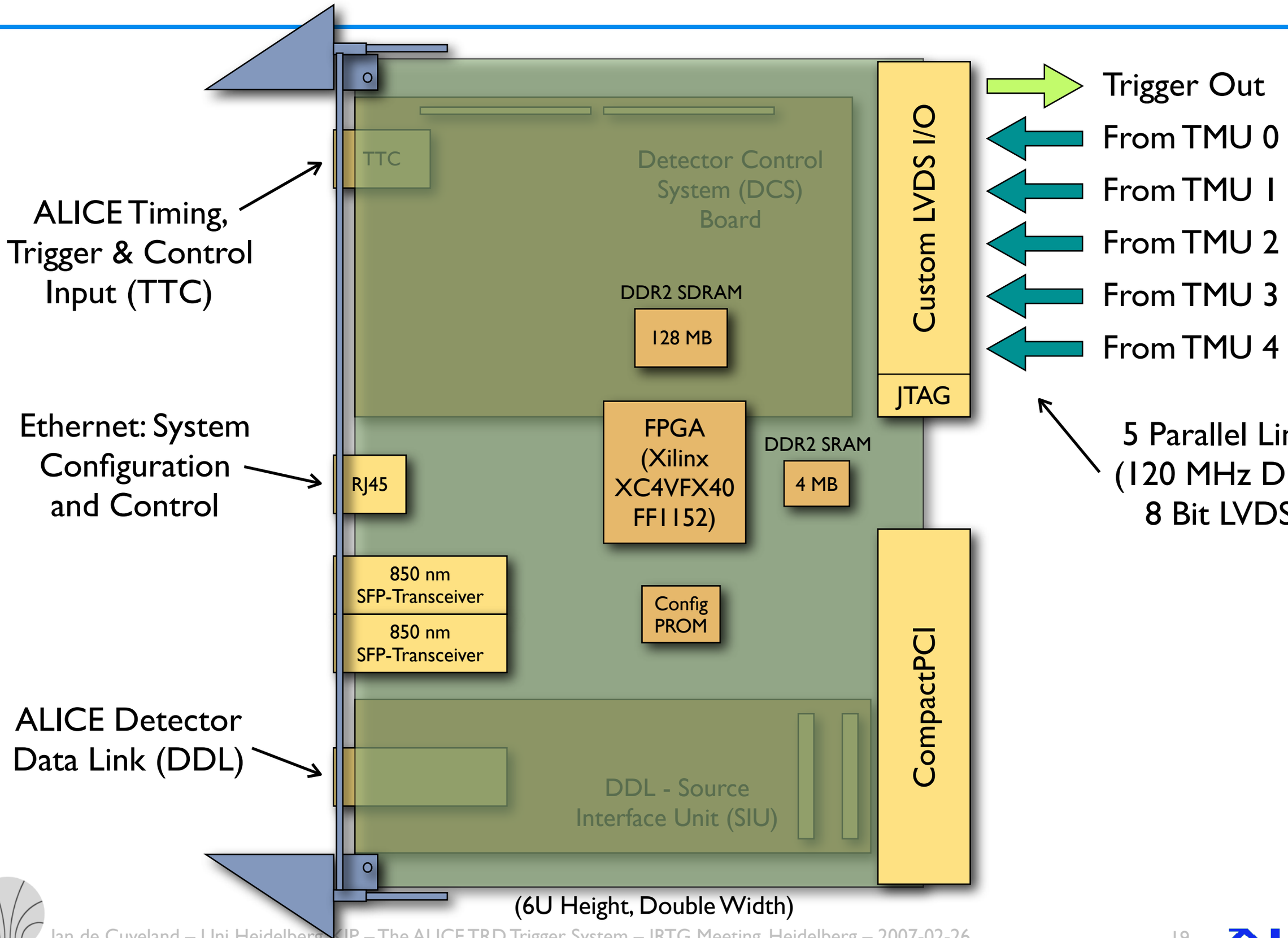
To SMU Board

DDR2 SRAM: High Bandwidth (28.8 GBit/s) Data Buffer

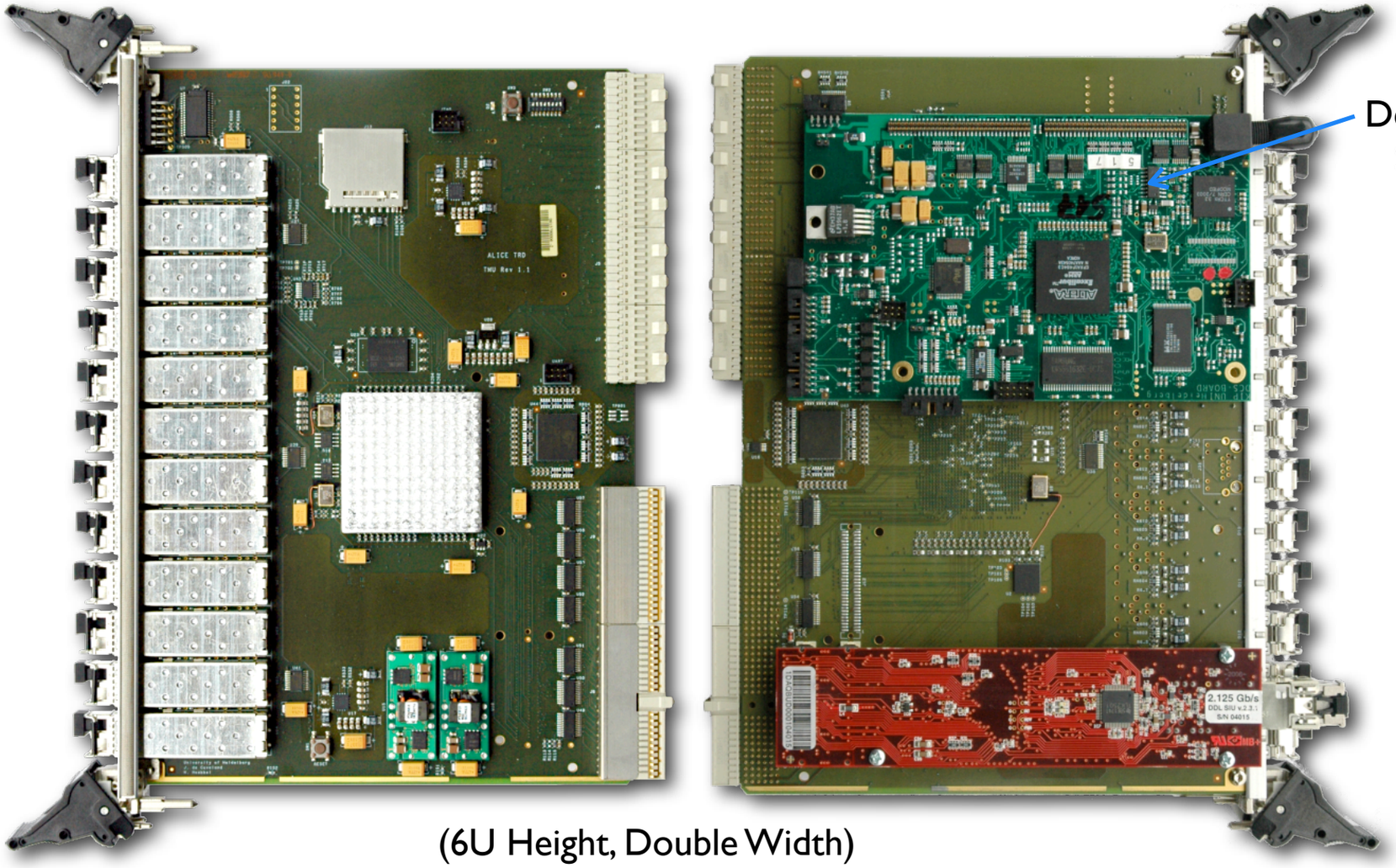
Virtex-4 FPGA: 59k LCs, 448 I/Os, 12 Internal Multi-Gigabit Serializer/ Deserializer-Units, 2 PowerPC Cores

(6U Height, Single Width)

SMU Concentrator Board



Combined TMU/SMU Board

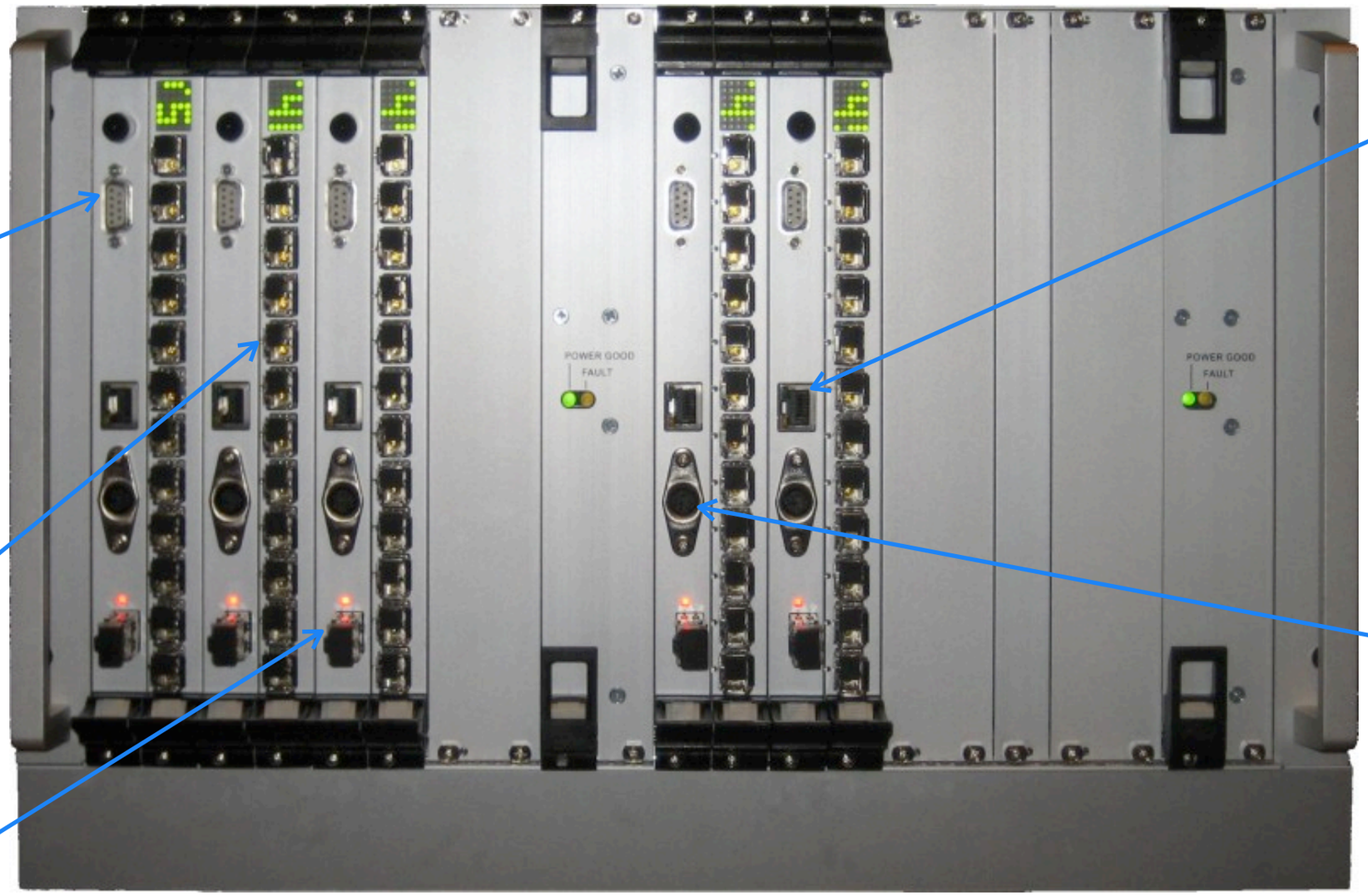


(6U Height, Double Width)

- Alternative assembly for stand-alone operation without LVDS backplane
- Used for testing with the first TRD super-module
- Modifications needed for ethernet socket, SIU mounting
- Not used in the final ALICE TRD setup

Current Intermediate GTU Setup

- **5 combined TMU/SMU boards**



Diagnostics and Debugging via Embedded PowerPC

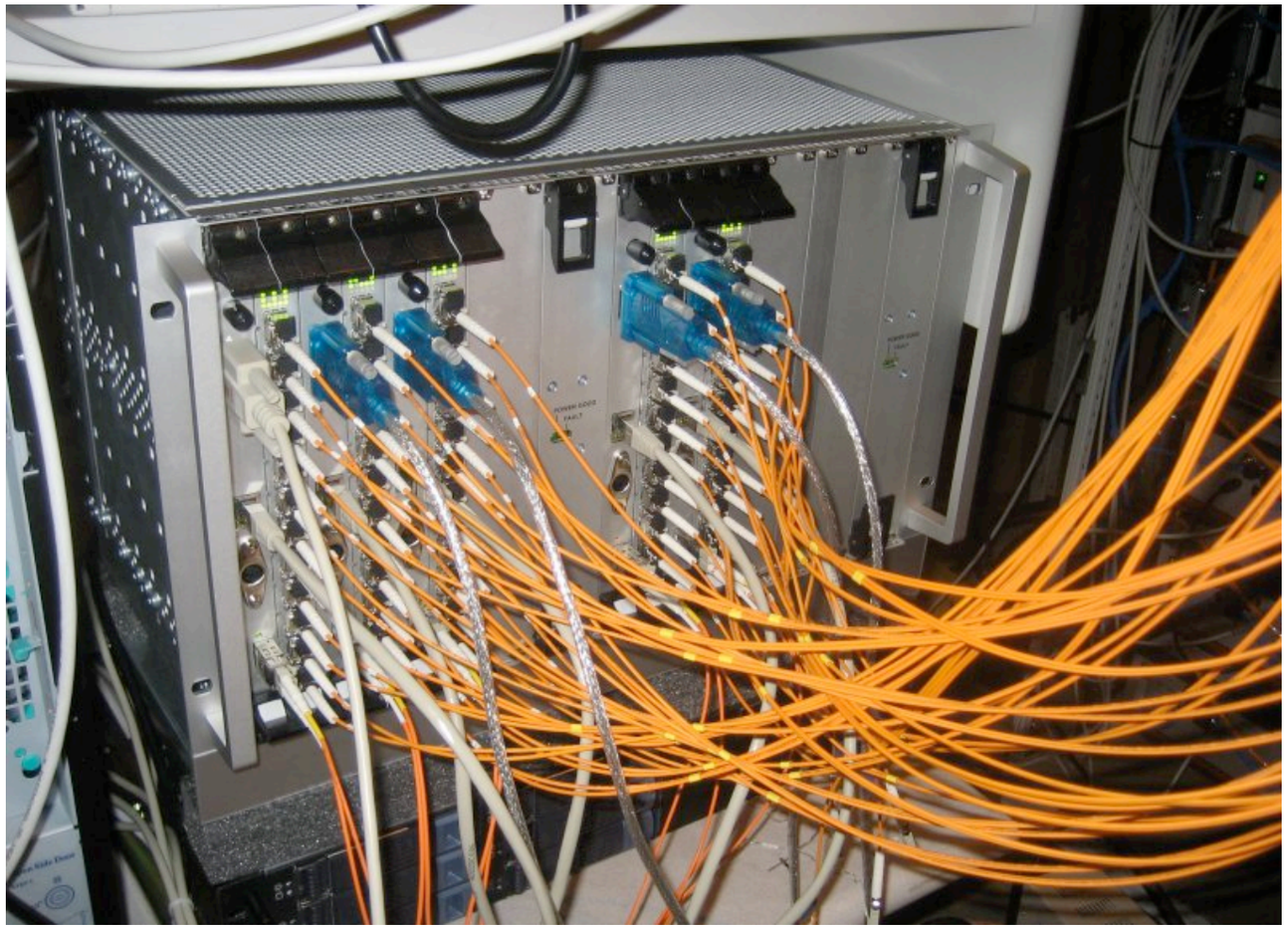
60 Fiber Optical Links

5 DDL SIUs

FPGA/PROM Programming and Control via DCS Boards (Ethernet)

JTAG Interfaces for Additional Debugging

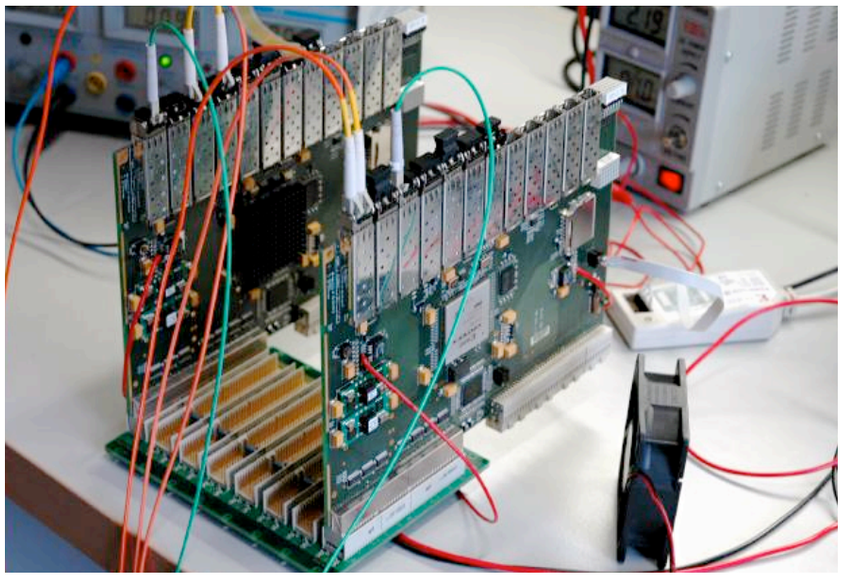
Latest Test Results



Current Test Setup

- Continuous parallel read-out of full TRD super-module via 60 links
- Successful transmission of detector raw data via DDL to DAQ PC
- Event shaper VHDL design still has timing problems (complex design running at 200 MHz) – sometimes, wrong data is transmitted
- Critical hardware components (FPGA, SFPs, MGTs, SRAM, PCI, SIU Interface, TTCrx interface on DCS board) successfully tested
- LVDS bus not yet tested
- Optical link diagnostic features via PowerPC supported detector integration
- No TMU/SMU hardware problems encountered

Status and Outlook

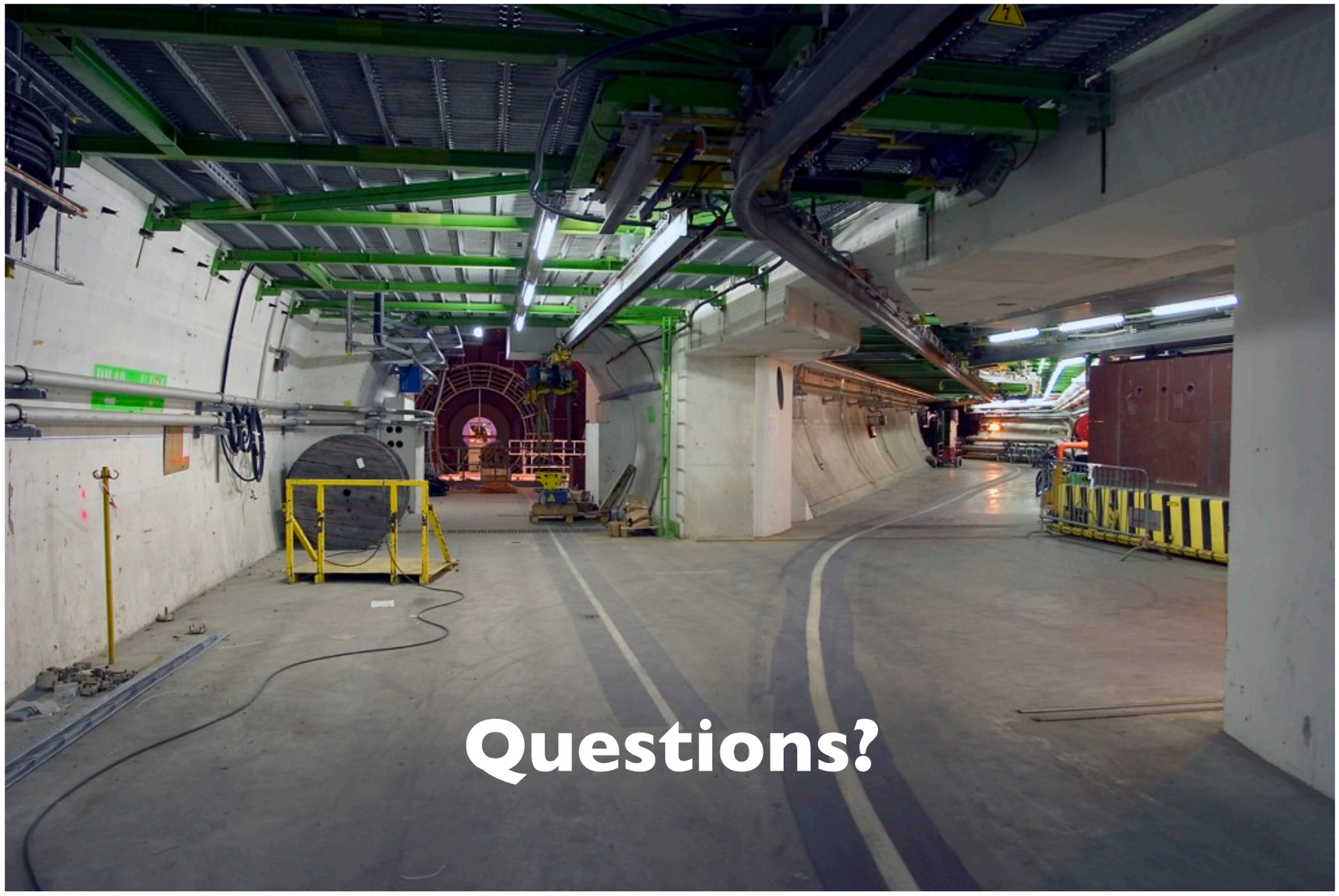


Prototype Test Setup, March 2006

Test Setup, October 2006

- TMU/SMU Hardware
  - PCB version with minor changes is in production, 130 PCBs to be delivered
- FPGA Design
  - Reconstruction and trigger algorithm implemented (in VHDL) and verified
  - Data-shipping design implemented, but needs further tuning to meet timing requirements
  - Control components are currently being implemented (TTC interfacing, backplane LVDS communication, ...)
- Next steps
  - Further testing and optimization of VHDL design, implement remaining components
  - Build final setup of 90 TMUs + 18 SMUs

Thank You for Your Attention



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