Implementation of High Precision Time to Digital Converters in FPGA Devices

Contents:

Analog methods for 'fine' measurements:

- Time stretching of the measured time interval

  The measured time interval T is stretched by a factor K by charging and discharging a capacitor before subsequent counting.

  $\longrightarrow$ Very high precision of about 10 ps.

  $\longrightarrow$ Small nonlinearities.

  $\longrightarrow$ Very long conversion time.

- Time to amplitude conversion

  The measured time interval is converted to a voltage by charging a capacitor with a constant current. The voltage is then sampled by an ADC.

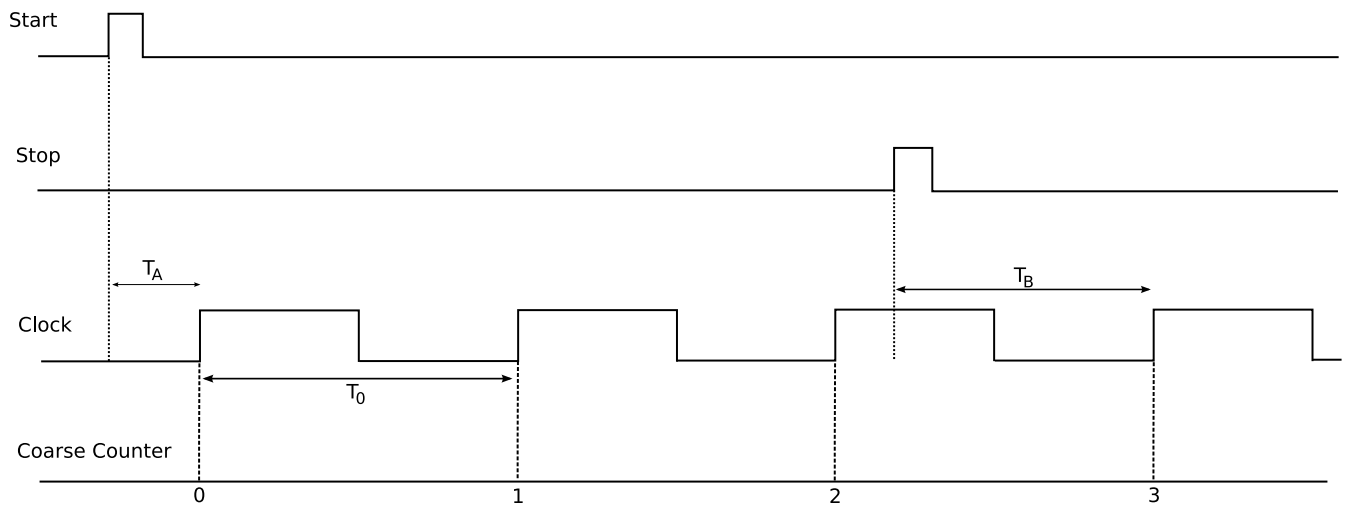
  $\longrightarrow$ Precision of 20ps possible.

  $\longrightarrow$ Shorter conversion time equal to the converstion time of the ADC.

  $\longrightarrow$ Larger nonlinearities.

Digital high resolution measurement of time intervals

Most digital TDCs use coarse and fine counters to measure a timeinterval:

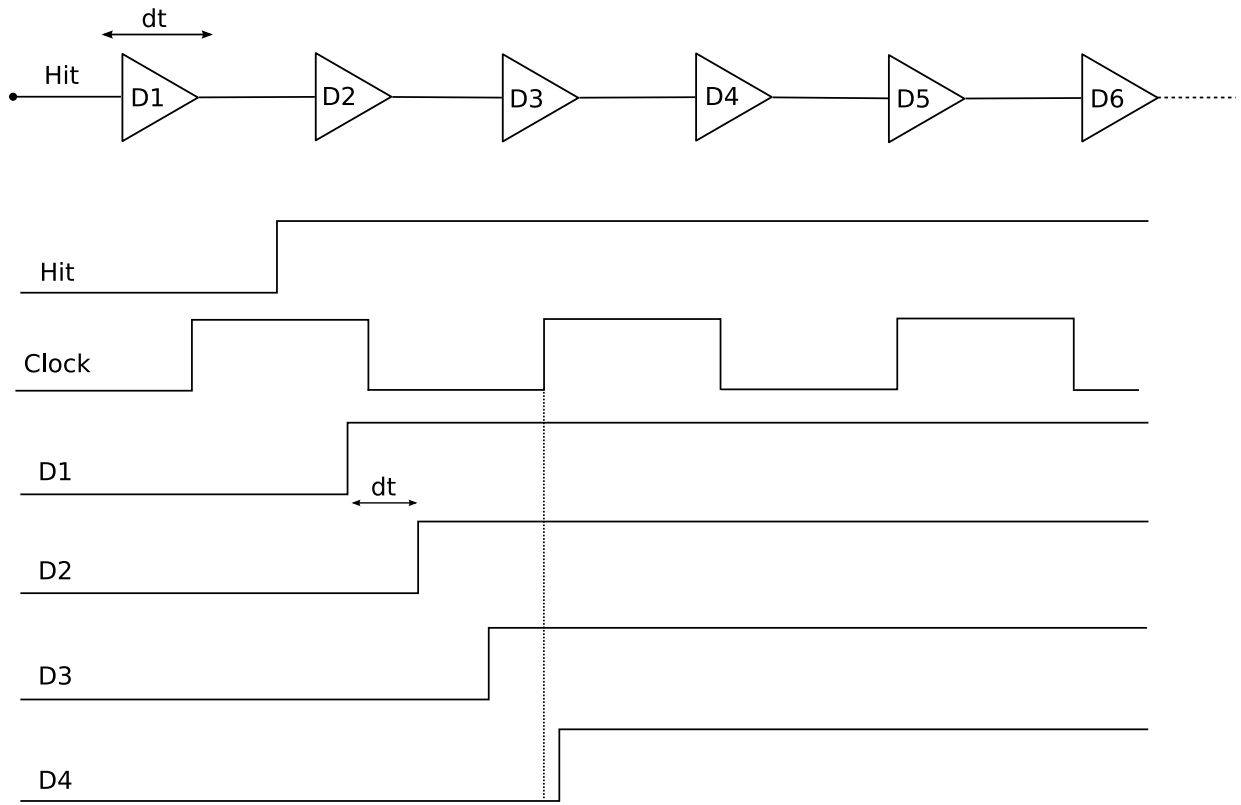


The coarse counter is driven by a reference clock providing a long measurement range.
The fine counter interpolates within one clock cycle providing a high resolution measurement of the time intervals T_A and T_B

The measured time interval T is: $T = n_c \cdot T_0 + T_A - T_B$

How to interpolate time within one clock cycle?

The common digital methods of measuring the time within one clock cycle use the propagation of the Start and Stop signal along a delay line.

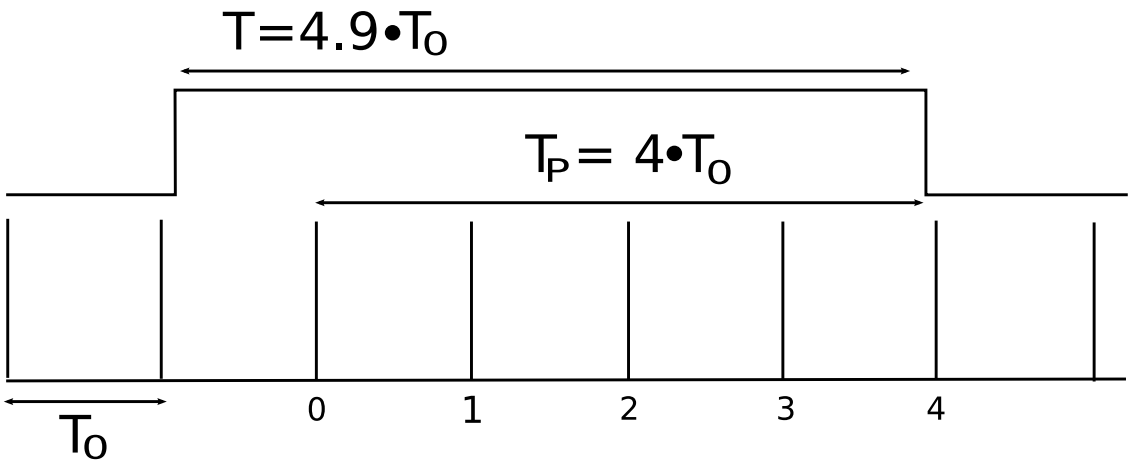


At the rising edge of the clock the state of the delay line is sampled used for the time interpolation.

Error sources limiting the precision σ_{RMS}

Quantization errors

In an ideal TDC time is measured in equal quantization steps of fixed lenght T_0.



Since neither Start nor Stop signals are correlated to the steps the maximum measurement error is $\pm T_0$.

When measuring a series of asynchronous intervals T the average error of the measurement is:

$$\sigma_{av} = \frac{T_0}{\sqrt{6}}$$

Differential and Integral non-linearity

The delay lines of TDCs, especially in FPGA devices, are not uniform resulting in bin width variations of the fine time measurement. The differential nonlinearity for the bin i of the delay chain is:

$$DNL_i = \frac{\tau_i - \tau_{\text{average}}}{\tau_{\text{average}}}$$

The integral nonlinearity for the bin j of the delay chain is then:

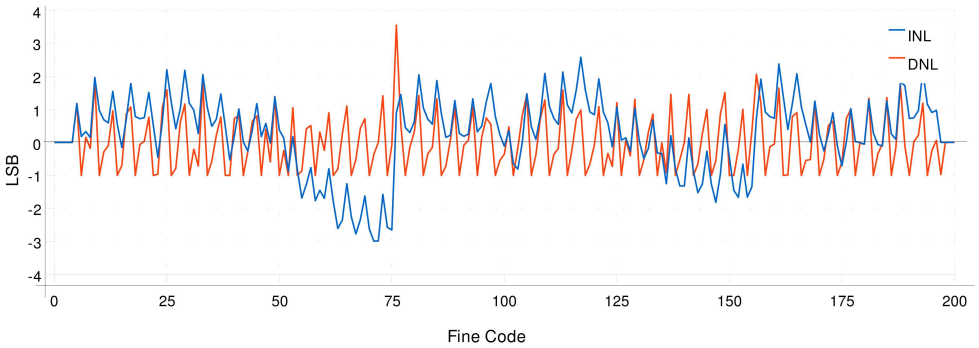
$$INL_j = \sum_{i=0}^{j} DNL_i$$

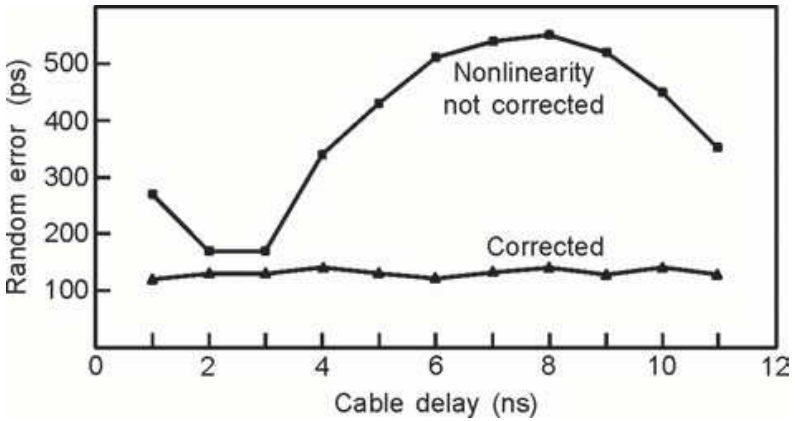
Measuring and correcting nonlinearities

Differential and integral nonlinearities can be measured using statistical methods. The code density test generates N events equally distributed over the interpolation interval with M bins. The differential nonlinearity is given by:

$$DNL_i = \frac{n_i - n_{average}}{n_{average}} \text{ with } n_{average} = \frac{N}{M}$$

Using this measurement the nonlinearities can be corrected.

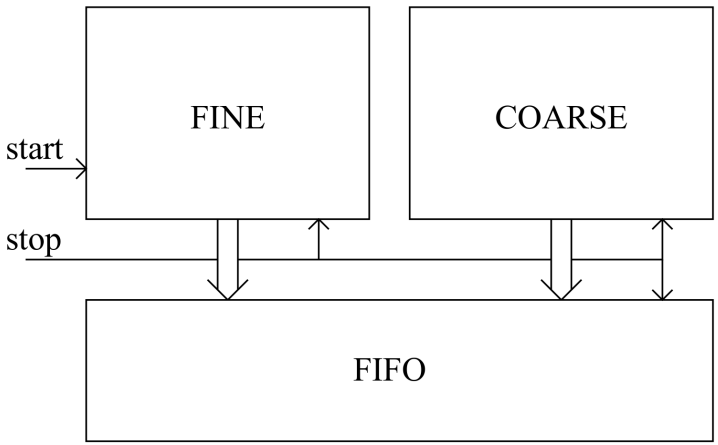




Implementations of high precision TDCs in FPGA devices

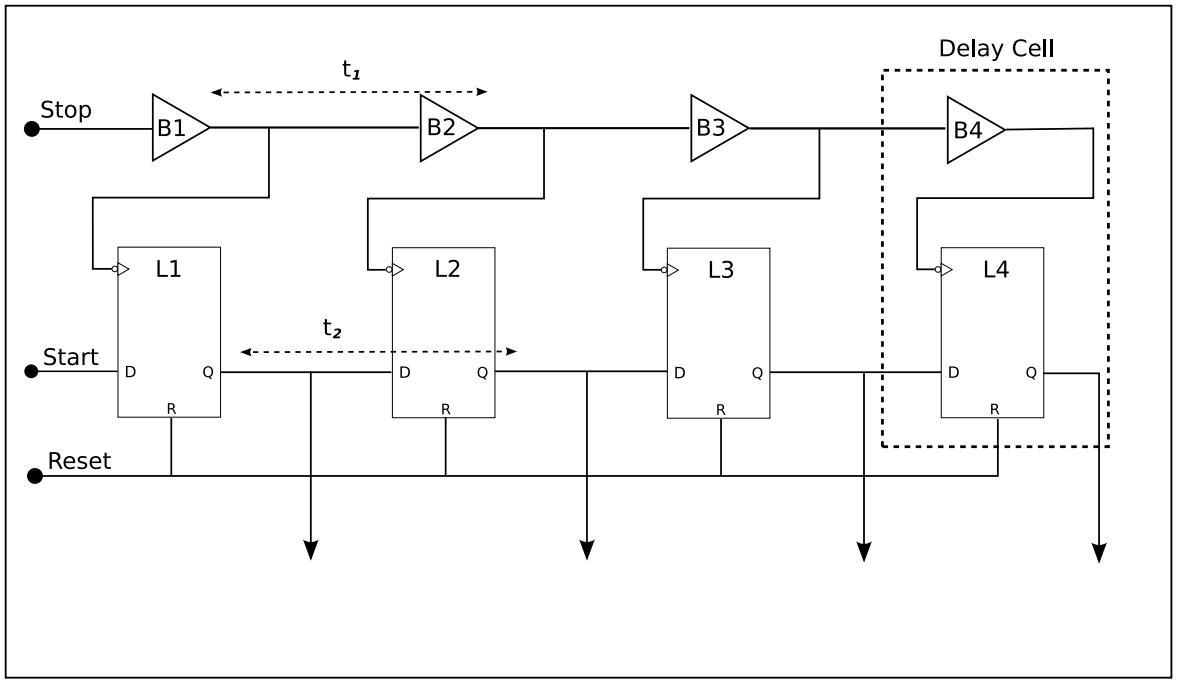
Basic architecture

High precision FPGA TDCs employ the coarse fine architecture.



The coarse counter is driven by a clock in the range of 300 MHz to 500 MHz and is designed as a free running counter in most implementations.
The TDC designs only differ in the implementation of the fine counter significantly.

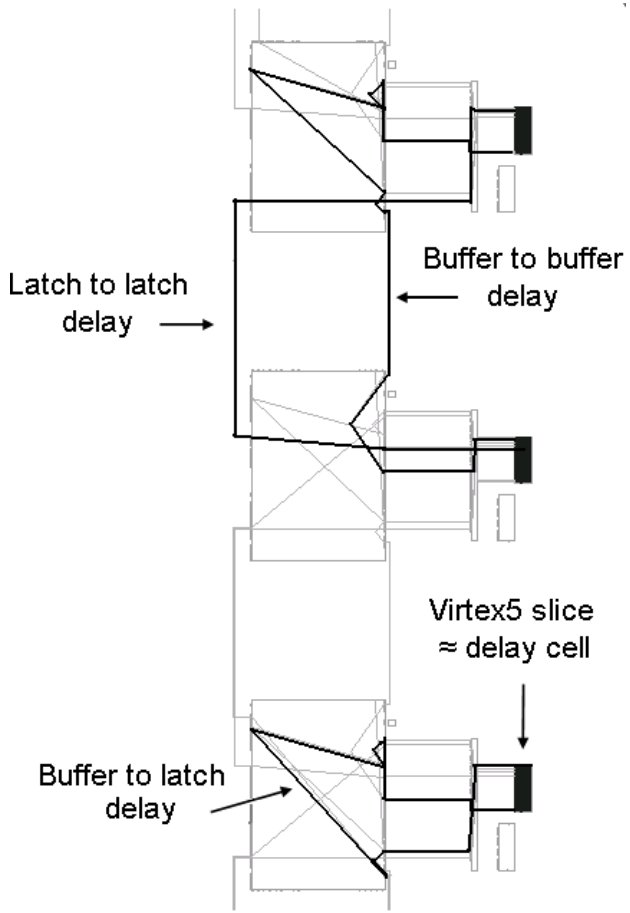
1. The vernier delay line



The Stop pulse follows the Start pulse along the line. All latches up to the cell where the Stop pulse overtakes the Start pulse are set.

The quantization step of this method is: $t_2 - t_1$.

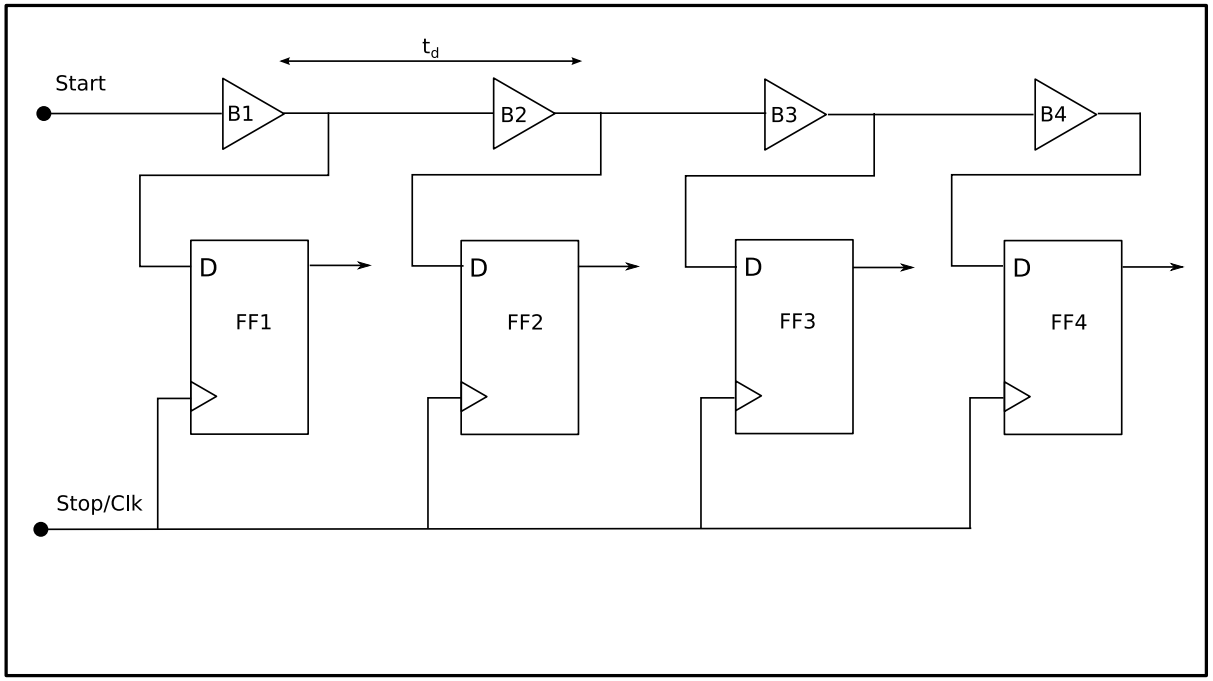
1. The vernier delay line



In FPGA devices this method introduces large differential nonlinearities especially if routed automatically.

The obtained resolution of this device was about 80ps.

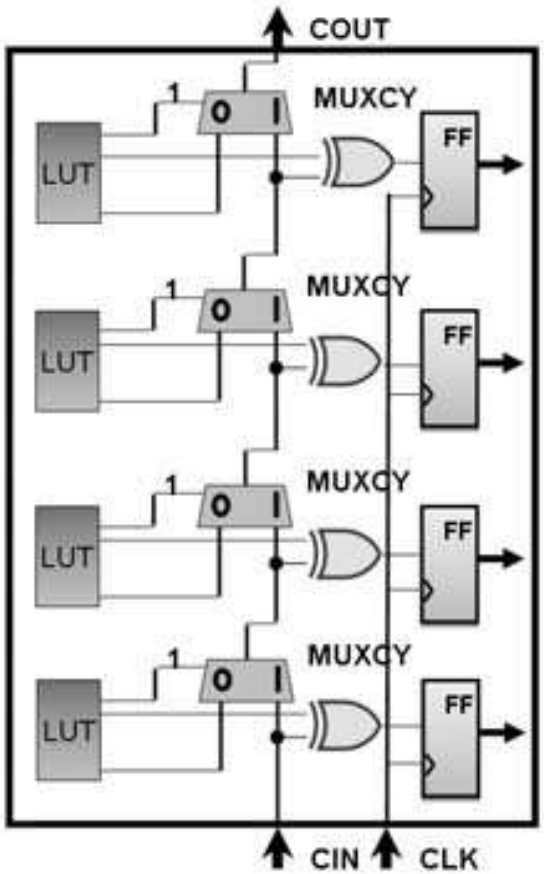
2. Tapped delay line



The state of the tapped delay line is sampled on the rising edge of the Stop signal.

The quantization step is determined by the buffer propagation delay t_d.

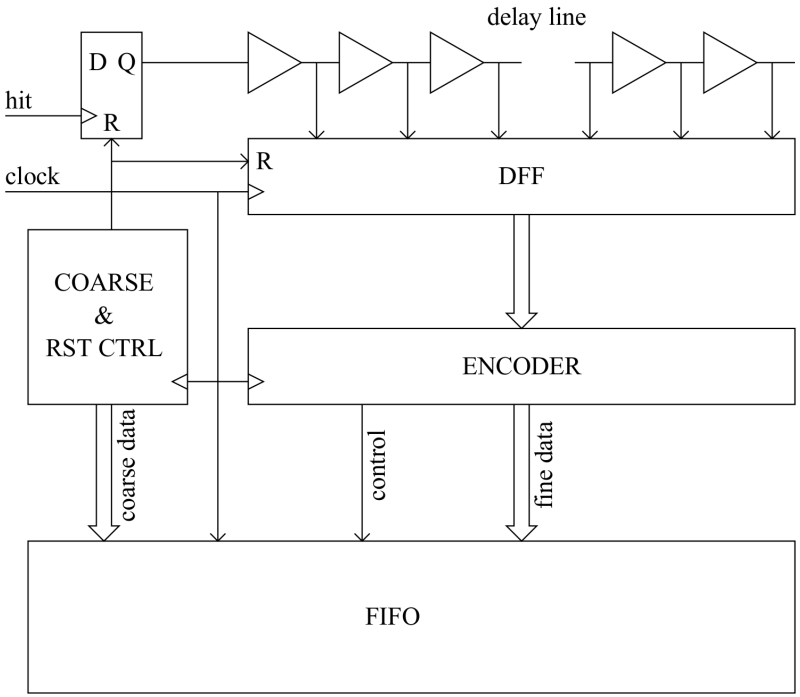
2. Tapped delay lines



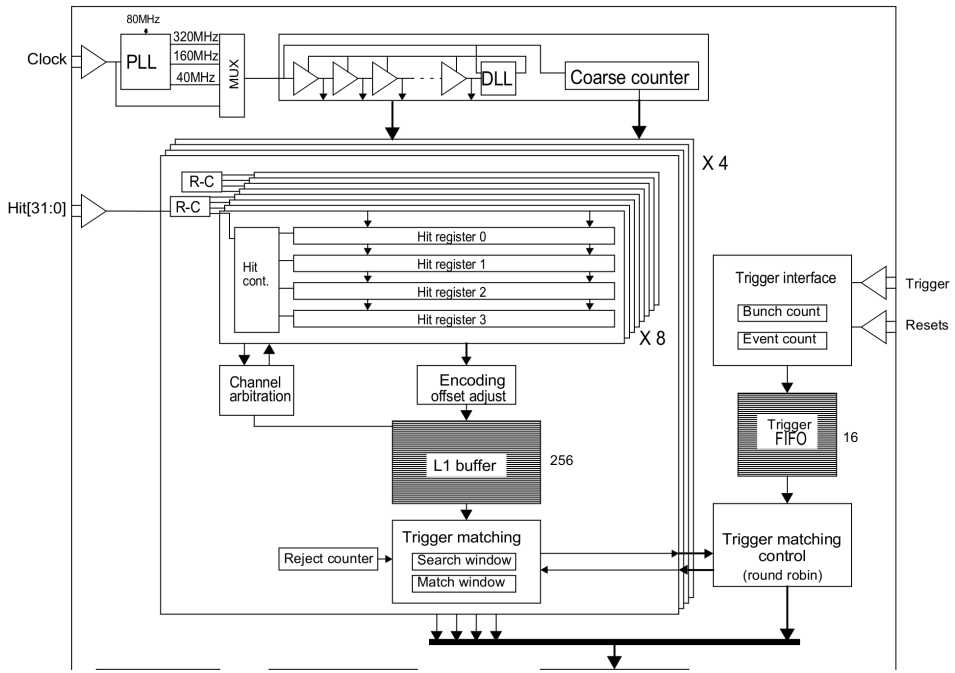
- The dedicated carry lines in FPGAs are perfectly suited for tapped delay lines.
- Uniform routing between delay elements and FlipFlops
- Delay steps from 14 ps to 34 ps.

TDCs with 25ps resolution using tapped delay lines

In a Xilinx Virtex 5 FPGA



HPTDC Chip (CERN)



Calibration of the delay line

This TDC architecture uses 2 methods for calibration of the delay line.

- Automatic Range Adjustment

  The incremental resolution of the delay line is measured on-the-fly and used to adjust the interpolation.

Coarse	fine line	N(x)
x-1	1111111111111111	0
x	1111111111111000000	6
x+1	1100000000000000000	16

$$LSB = \frac{T}{N(x+1) - N(x)}$$

- Statistical code density test

  Using this method the real bin time distribution can be calculated.

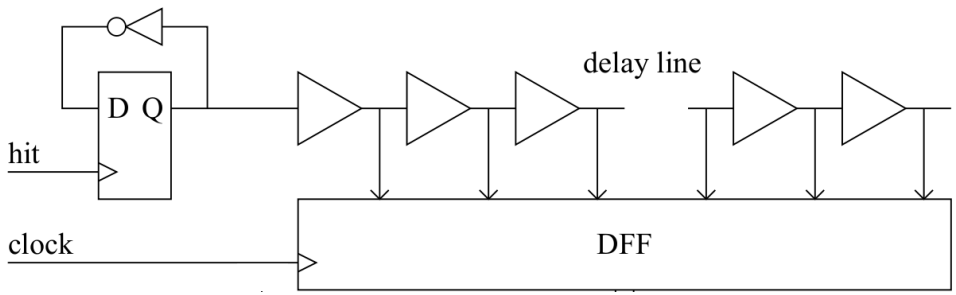
Encoding the delay line

Violations of the setup and hold times of the flipflop can create 'bubbles' in the state of the delay line.

1111111101000000

The encoder translates the state of the delay line into a binary value. It needs to be designed to be bubble proof.

Using different encoding schemes for the delay line one can improve dead time or resolution, i.e. Turbo mode of the TDC:



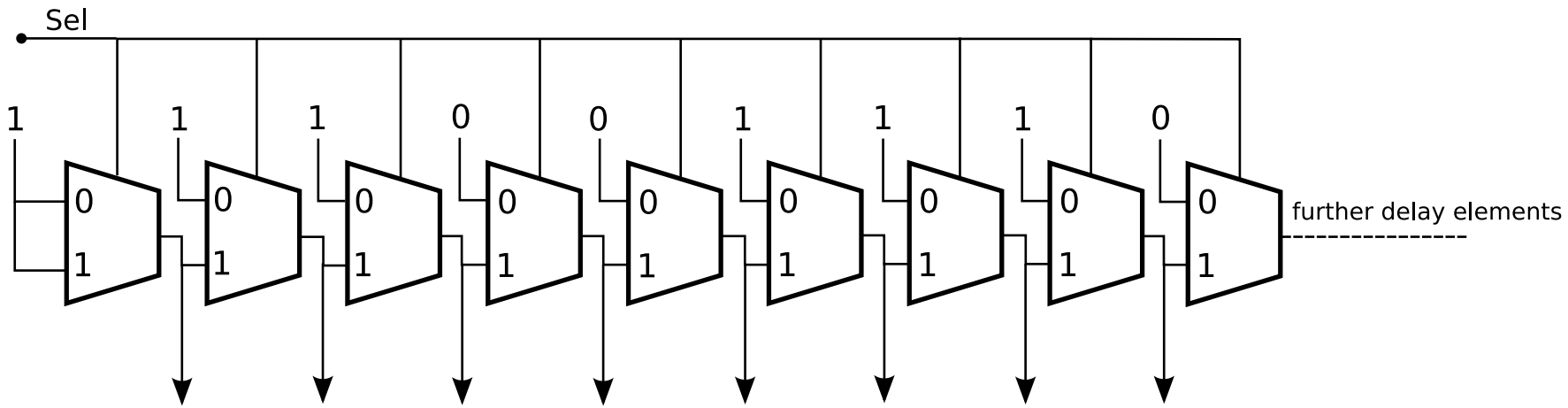
Delay line code with two hits: 0000000011111111110000

Performance summary of this TDC

	Min	Typ	Max	Unit
Clock frequency		300		MHz
Standard uncertainty	9.8		24.2	ps
Resolution		16.9		ps
DNL	-1		3.55	LSB
INL	-2.99		2.58	LSB
Normal Mode				
Measurement Range (MR)		50		ns
Dead Time (DT)	3.33		50	ns
Readout speed		20		MSample/s
Turbo Mode				
Measurement Range (MR)		53.33		ns
Dead Time (DT)	0.5		3.33	ns
Readout speed		300		MSample/s

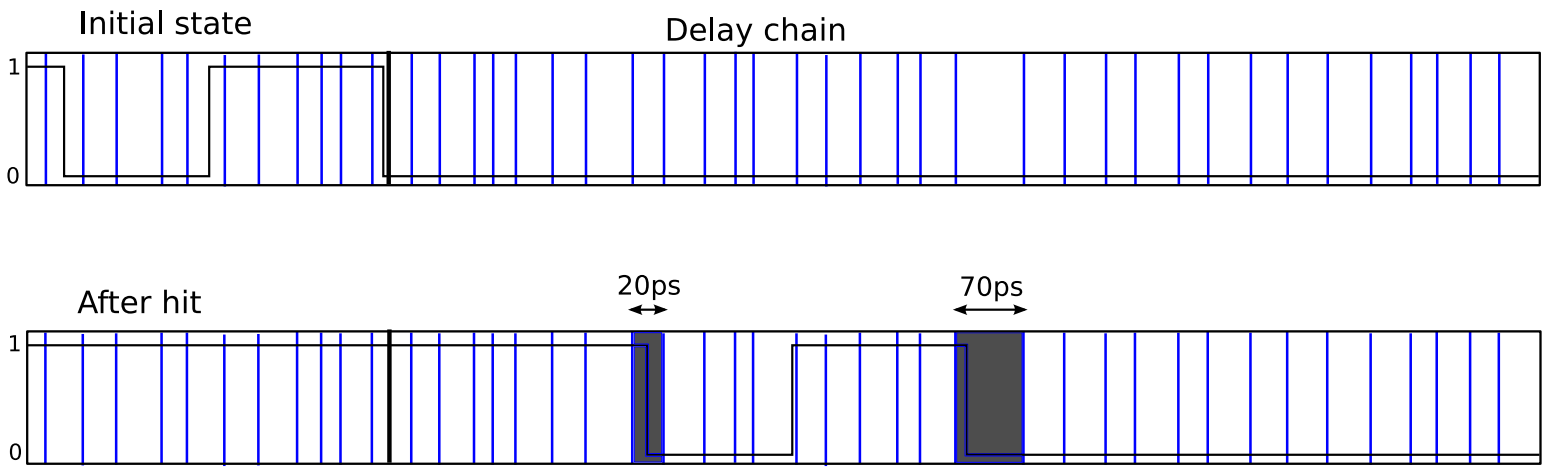
3. The Wave Union TDC

The Wave Union TDC uses the propagation of a logic pattern in a tapped delay line to reduce the nonlinearities and increase the resolution.



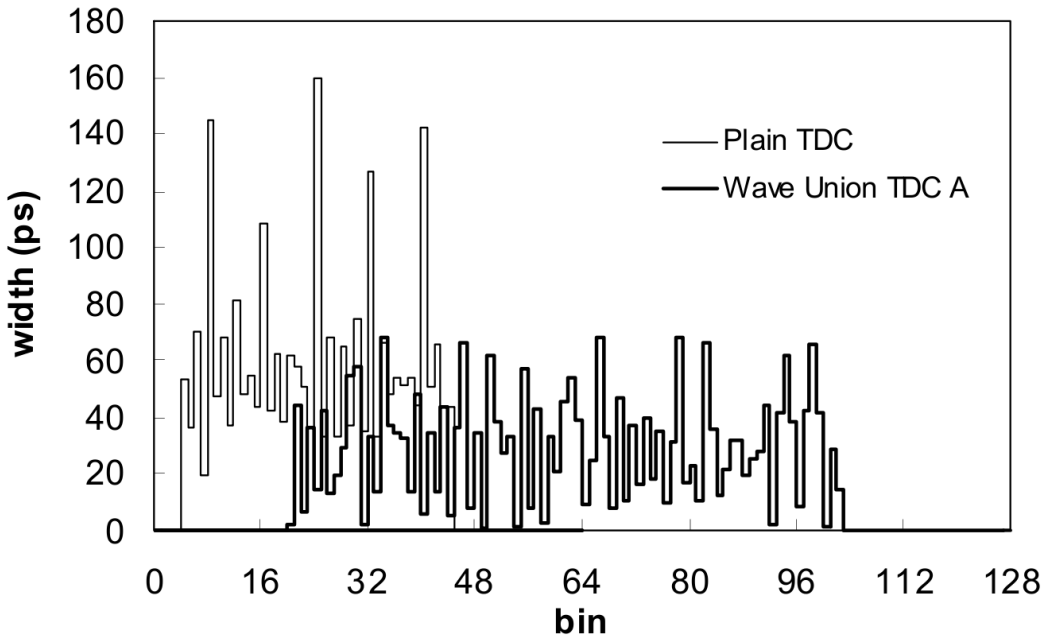
3. The Wave Union TDC

The resolution of the TDC is limited by the largest bin width of the delay chain. Multiple logic transitions in the delay chain can be used to subdivide large bins.



3. The Wave Union TDC

The improvement by using multiple transitions can be measured by performing a code density test. The 'Plain TDC' uses one logic transition and the 'Wave Union TDC A' uses two. In case of the Wave Union TDC A the sum of the bin numbers with the two transitions is used by the encoder.



Improvement by using two logic transitions

The Wave Union TDC has been implemented in an Altera Cyclone II device. The resolution of the TDC can be further improved by using an oscillator to generate 'infinite' logic transitions in the delay chain (Wave Union TDC B).

PARAMETERS OF SEVERAL TDC SCHEMES

Device: EP2C8T144C6, Price: $28 (April 2008), Operating Frequency: 400MHz, Total Logic Elements: 8256						
	Max bin width	Av bin width	ΔT RMS error	Dead Time	Delay Chain Length	Logic Element Usage
Un-calibrated TDC	165ps	60ps	58ps	2.5ns	64	1621 (20%)
Plain TDC	165ps	60ps	40ps	2.5ns		
Wave Union TDC A	65ps	30ps	25ps	5ns		
Wave Union TDC B			10ps	45ns		6851 (83%) 8 CH

Conclusion

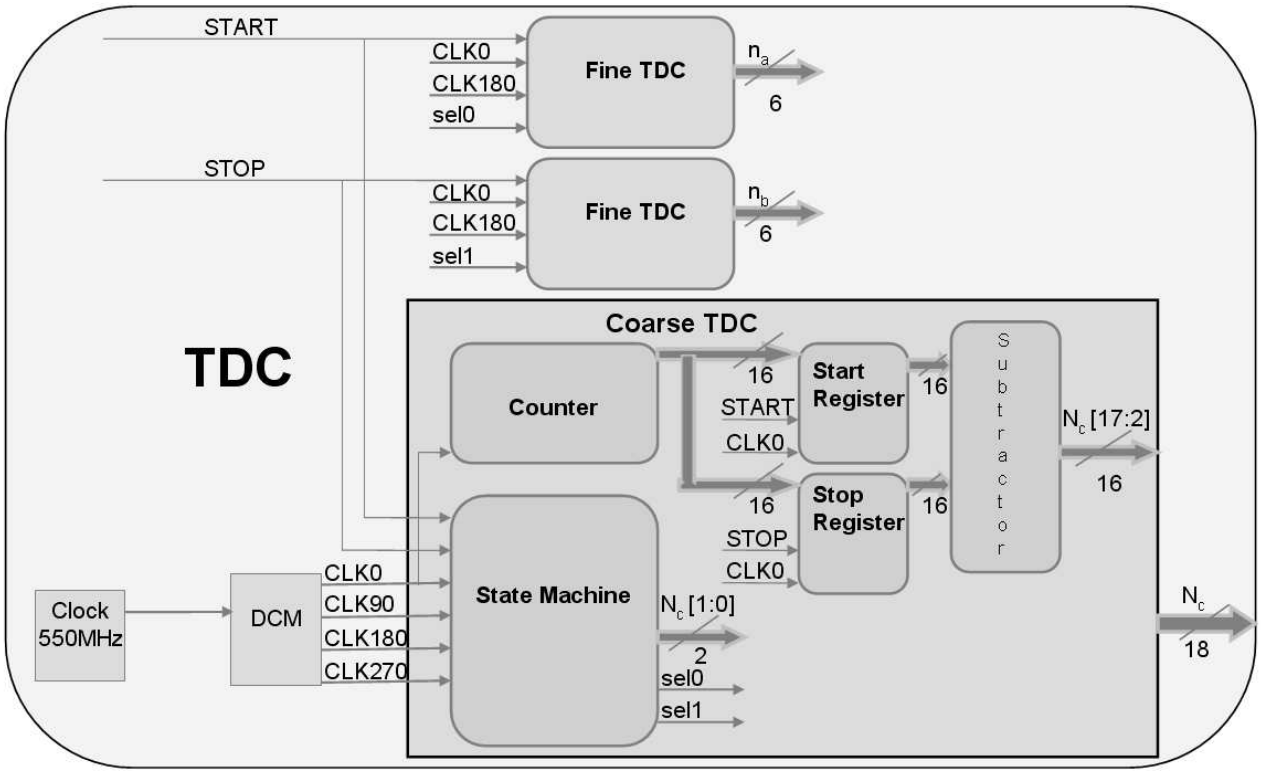
- FPGA TDC devices suffer from large differential and integral nonlinearities.
- Using dedicated carry structures to implement tapped delay lines resolutions of 25ps are possible.
- The Wave Union TDC introduces a method to improve the resolution beyond the cell delay and reduce nonlinearities.

  Using this method resolutions of 10ps can be achieved.

Backup slides

Reducing the length of the delay chain

Digital Clock Managers in FPGAs can subdivide a clock signal in 4 phases that are shifted by 90°. With the additional phase information the delay lines are only needed for interpolation within one quadrant of the clock cycle.



Quantization errors

When measuring a series of a constant and asynchronous interval T two results are obtained:

$$T_1 < T \text{ and } T_2 = T_1 + T_0 > T$$

The probability to measure T_1 or T_2 is correlated to the length of T. The average and maximum standard deviation for a measured time interval T can be calculated to:

$$\sigma_{av} = \frac{T_0}{\sqrt{6}}$$

$$\sigma_{max} = 0.5 \cdot T_0$$